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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15400
Total RAM Bits	358400
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec15e-3fn256i

LatticeECP/EC Family Data Sheet Architecture

September 2012 **Data Sheet**

Architecture Overview

The LatticeECP-DSP and LatticeEC architectures contain an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR), as shown in Figures 2-1 and 2-2. In addition, LatticeECP-DSP supports an additional row of DSP blocks, as shown in Figure 2-2.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeECP/EC architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The LatticeECP/EC devices use 1.2V as their core voltage.

Figure 2-4. Slice Diagram

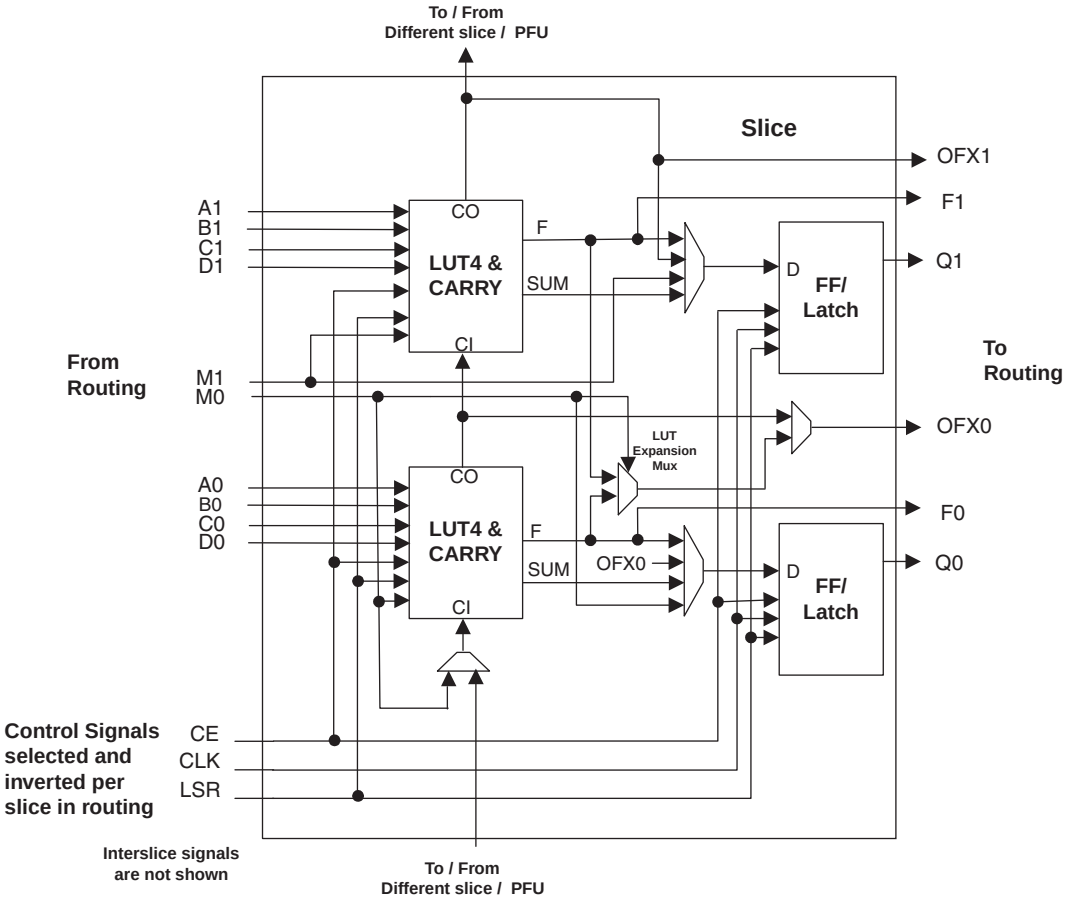


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

IPexpress™

The user can access the sysDSP block via the IPexpress configuration tool, included with the ispLEVER design tool suite. IPexpress has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
LFECP6	4	32	16	4
LFECP10	5	40	20	5
LFECP15	6	48	24	6
LFECP20	7	56	28	7
LFECP33	8	64	32	8

Table 2-10. Embedded SRAM in LatticeECP Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LFECP6	10	92
LFECP10	30	276
LFECP15	38	350
LFECP20	46	424
LFECP33	54	498

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

Table 2-11. DSP Block Performance of LatticeECP Family

Device	DSP Block	DSP Performance MMAC
LFECP6	4	3680
LFECP10	5	4600
LFECP15	6	5520
LFECP20	7	6440
LFECP33	8	7360

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP/EC devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeECP/EC sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL, BLVDS, RSDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeECP/EC devices contain two possible ports that can be used for device configuration. The test access port (TAP), which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The TAP supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins (please refer to TN1053 for more information about using the dual-use pins as general purpose I/O). There are four configuration options for LatticeECP/EC devices:

1. Industry standard SPI memories.
2. Industry standard byte wide flash and ispMACH 4000 for control/addressing.
3. Configuration from system microprocessor via the configuration bus or TAP.
4. Industry standard FPGA board memory.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next power-up sequence.

For more information about device configuration, please see the list of technical documentation at the end of this data sheet.

Internal Logic Analyzer Capability (ispTRACY)

All LatticeECP/EC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information about ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP/EC devices require a single external, 10K ohm +/- 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCIO} - 0.2V)	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	(V_{CCIO} - 0.2V) ð V_{IH} ð 3.6V	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCIO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO}.

Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Devices	Typ.[6]	Units
I_{CC}	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFECP6/LFEC6	50	mA
		LFECP10/LFEC10	60	mA
		LFECP15/LFEC15	70	mA
		LFECP20/LFEC20	150	mA
		LFECP33/LFEC33	220	mA
I_{CCAUX}	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFECP6/LFEC6	30	mA
		LFECP10/LFEC10	35	mA
		LFECP15/LFEC15	35	mA
		LFECP20/LFEC20	40	mA
		LFECP33/LFEC33	40	mA
I_{CCPLL}	PLL Power Supply Current		12	mA
I_{CCIO}	Bank Power Supply Current[7]	LFEC1	4	mA
		LFEC3	5	mA
		LFECP6/LFEC6	6	mA
		LFECP10/LFEC10	6	mA
		LFECP15/LFEC15	7	mA
		LFECP20/LFEC20	8	mA
		LFECP33/LFEC33	8	mA
I_{CCJ}	V_{CCJ} Power Supply Current		20	mA

1. Until DONE signal is active.
2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.
6. T_J=25ºC, power supplies at nominal voltage.
7. Per bank.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	5.5	ns
32-bit decoder	6.9	ns
64-bit decoder	7.1	ns
4:1 MUX	4.3	ns
8:1 MUX	4.7	ns
16:1 MUX	5.0	ns
32:1 MUX	5.5	ns

Register-to-Register Performance[1]

Function	-5 Timing	Units
Basic Functions		
16 bit decoder	410	MHz
32 bit decoder	283	MHz
64 bit decoder	272	MHz
4:1 MUX	613	MHz
8:1 MUX	565	MHz
16:1 MUX	526	MHz
32:1 MUX	442	MHz
8-bit adder	363	MHz
16-bit adder	353	MHz
64-bit adder	196	MHz
16-bit counter	414	MHz
32-bit counter	317	MHz
64-bit counter	216	MHz
64-bit accumulator	178	MHz
Embedded Memory Functions		
256x36 Single Port RAM	280	MHz
512x18 True-Dual Port RAM	280	MHz
Distributed Memory Functions		
16x2 Single Port RAM	460	MHz
64x2 Single Port RAM	375	MHz
128x4 Single Port RAM	294	MHz
32x2 Pseudo-Dual Port RAM	392	MHz
64x4 Pseudo-Dual Port RAM	332	MHz
DSP Function[2]		
9x9 Pipelined Multiply/Accumulate	242	MHz
18x18 Pipelined Multiply/Accumulate	238	MHz
36x36 Pipelined Multiply	235	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Applies to LatticeECP devices only.

Timing v.G 0.30

LatticeECP/EC External Switching Characteristics (Continued)

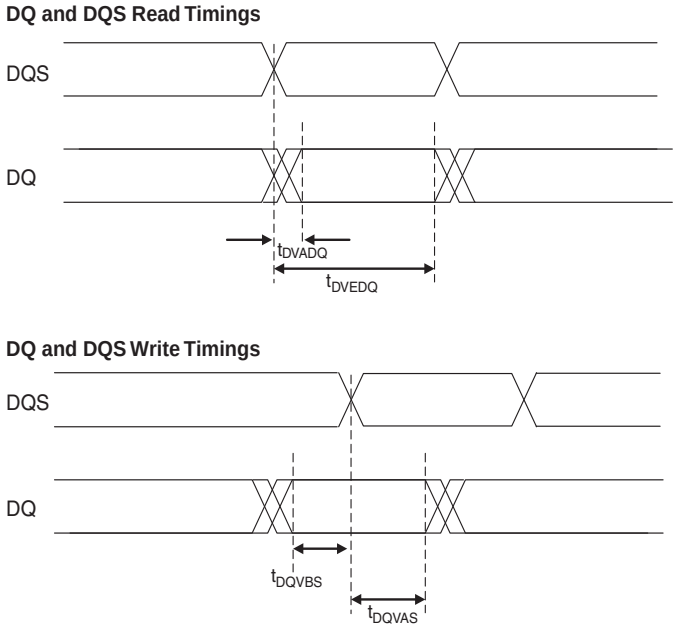
Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	200	95	166	95	133	MHz
Primary and Secondary Clock[6]									
f_{MAX_PRI}[2]	Frequency for Primary Clock Tree	All	—	420	—	378	—	340	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	All	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA. Loading of 0 pF.
2. Using LVDS I/O standard.
3. DDR timing numbers based on SSTL I/O.
4. DDR specifications are characterized but not tested.
5. UI is average bit period.
6. Based on a single primary clock.
7. These timing numbers were generated using ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.G 0.30

Figure 3-5. DDR Timings



LFEC1, LFEC3, LFECP/EC6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFEC1				LFEC3				LFECP6/EC6			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
99	VCC	-			VCC	-			VCC	-		
100	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
101	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
102	PR4B	2	C		PR8B	2	C		PR8B	2	C	
103	PR4A	2	T		PR8A	2	T		PR8A	2	T	
104	PR3B	2	C		PR7B	2	C		PR7B	2	C	
105	PR3A	2	T		PR7A	2	T		PR7A	2	T	
106	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
107	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
108	VCCIO2	2			VCCIO2	2			VCCIO2	2		
109*	GND1 GND2	-			GND1 GND2	-			GND1 GND2	-		
110	VCCIO1	1			VCCIO1	1			VCCIO1	1		
111	PT17B	1	C		PT25B	1	C		PT25B	1	C	
112	PT17A	1	T		PT25A	1	T		PT25A	1	T	
113	PT15A	1			PT23A	1			PT23A	1		
114	PT14B	1	C		PT22B	1	C		PT22B	1	C	
115	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
116	PT13B	1	C		PT21B	1	C		PT21B	1	C	
117	GND1	1			GND1	1			GND1	1		
118	PT13A	1	T		PT21A	1	T		PT21A	1	T	
119	PT12B	1	C		PT20B	1	C		PT20B	1	C	
120	PT12A	1	T		PT20A	1	T		PT20A	1	T	
121	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
122	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
123	PT10B	1	C		PT18B	1	C		PT18B	1	C	
124	PT10A	1	T		PT18A	1	T		PT18A	1	T	
125	VCCIO1	1			VCCIO1	1			VCCIO1	1		
126	VCCAUX	-			VCCAUX	-			VCCAUX	-		
127	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
128	GND0	0			GND0	0			GND0	0		
129	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
130	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
131	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
132	PT7B	0	C		PT15B	0	C		PT15B	0	C	
133	PT7A	0	T		PT15A	0	T		PT15A	0	T	
134	PT6B	0	C		PT14B	0	C		PT14B	0	C	
135	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
136	VCCIO0	0			VCCIO0	0			VCCIO0	0		
137	PT5B	0	C		PT13B	0	C		PT13B	0	C	
138	PT5A	0	T		PT13A	0	T		PT13A	0	T	
139	PT4B	0	C		PT12B	0	C		PT12B	0	C	
140	PT4A	0	T		PT12A	0	T		PT12A	0	T	
141	PT2B	0	C		PT10B	0	C		PT10B	0	C	
142	PT2A	0	T		PT10A	0	T		PT10A	0	T	
143	VCCIO0	0			VCCIO0	0			VCCIO0	0		
144*	GND0 GND7	-			GND0 GND7	-			GND0 GND7	-		

*Double bonded to the pin.

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
169	PT21A	1	T		PT29A	1	T	
170	PT20B	1	C		PT28B	1	C	
171	PT20A	1	T		PT28A	1	T	
172	PT19B	1	C	VREF2_1	PT27B	1	C	VREF2_1
173	PT19A	1	T	VREF1_1	PT27A	1	T	VREF1_1
174	PT18B	1	C		PT26B	1	C	
175	PT18A	1	T		PT26A	1	T	
176	VCCIO1	1			VCCIO1	1		
177	VCCAUX	-			VCCAUX	-		
178	PT17B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
179	GND0	0			GND0	0		
180	PT17A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
181	PT16B	0	C	VREF1_0	PT24B	0	C	VREF1_0
182	PT16A	0	T	VREF2_0	PT24A	0	T	VREF2_0
183	PT15B	0	C		PT23B	0	C	
184	PT15A	0	T		PT23A	0	T	
185	PT14B	0	C		PT22B	0	C	
186	PT14A	0	T	TDQS14	PT22A	0	T	TDQS22
187	VCCIO0	0			VCCIO0	0		
188	PT13B	0	C		PT21B	0	C	
189	GND0	0			GND0	0		
190	PT13A	0	T		PT21A	0	T	
191	PT12B	0	C		PT20B	0	C	
192	PT12A	0	T		PT20A	0	T	
193	PT11B	0	C		PT19B	0	C	
194	PT11A	0	T		PT19A	0	T	
195	PT10B	0	C		PT18B	0	C	
196	PT10A	0	T		PT18A	0	T	
197	VCCIO0	0			VCCIO0	0		
198	PT6B	0	C		PT6B	0	C	
199	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
200	PT5B	0	C		PT5B	0	C	
201	PT5A	0	T		PT5A	0	T	
202	PT4B	0	C		PT4B	0	C	
203	PT4A	0	T		PT4A	0	T	
204	PT3B	0	C		PT3B	0	C	
205	PT3A	0	T		PT3A	0	T	
206	PT2B	0	C		PT2B	0	C	
207	PT2A	0	T		PT2A	0	T	
208	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W17	NC	-			W17	NC	-			W17	PB46B	4	C	
AA20	NC	-			AA20	NC	-			AA20	PB47A	4	T	
Y19	NC	-			Y19	NC	-			Y19	PB47B	4	C	
Y18	NC	-			Y18	NC	-			Y18	PB48A	4	T	
W18	NC	-			W18	NC	-			W18	PB48B	4	C	
T17	NC	-			T17	NC	-			T17	PB49A	4	T	
U17	NC	-			U17	NC	-			U17	PB49B	4	C	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3			GND	GND3	3		
W20	PR27B	3	C	VREF2_3	W20	PR36B	3	C	VREF2_3	W20	PR44B	3	C	VREF2_3
Y20	PR27A	3	T	VREF1_3	Y20	PR36A	3	T	VREF1_3	Y20	PR44A	3	T	VREF1_3
AA21	PR26B	3	C		AA21	PR35B	3	C		AA21	PR43B	3	C	
AB21	PR26A	3	T		AB21	PR35A	3	T		AB21	PR43A	3	T	
W19	PR25B	3	C		W19	PR34B	3	C		W19	PR42B	3	C	
V19	PR25A	3	T		V19	PR34A	3	T		V19	PR42A	3	T	
Y21	PR24B	3	C		Y21	PR33B	3	C		Y21	PR41B	3	C	
AA22	PR24A	3	T	RDQS24	AA22	PR33A	3	T	RDQS33	AA22	PR41A	3	T	RDQS41
V20	PR23B	3	C	RLM0_PLLC_FB_A	V20	PR32B	3	C	RLM0_PLLC_FB_A	V20	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND	GND3	3			GND	GND3	3		
U20	PR23A	3	T	RLM0_PLLT_FB_A	U20	PR32A	3	T	RLM0_PLLT_FB_A	U20	PR40A	3	T	RLM0_PLLT_FB_A
W21	PR22B	3	C	RLM0_PLLC_IN_A	W21	PR31B	3	C	RLM0_PLLC_IN_A	W21	PR39B	3	C	RLM0_PLLC_IN_A
Y22	PR22A	3	T	RLM0_PLLT_IN_A	Y22	PR31A	3	T	RLM0_PLLT_IN_A	Y22	PR39A	3	T	RLM0_PLLT_IN_A
V21	PR21B	3	C	DI/CSSPIN	V21	PR30B	3	C	DI/CSSPIN	V21	PR38B	3	C	DI/CSSPIN
W22	PR21A	3	T	DOUT/CSON	W22	PR30A	3	T	DOUT/CSON	W22	PR38A	3	T	DOUT/CSON
U21	PR20B	3	C	BUSY/SISPI	U21	PR29B	3	C	BUSY/SISPI	U21	PR37B	3	C	BUSY/SISPI
V22	PR20A	3	T	D7/SPID0	V22	PR29A	3	T	D7/SPID0	V22	PR37A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3			R20	DONE	3		
T18	NC	-			T18	NC	-			T18	NC	-		
R17	NC	-			R17	NC	-			R17	NC	-		
R19	NC	-			R19	NC	-			R19	NC	-		
R18	NC	-			R18	NC	-			R18	NC	-		
U22	NC	-			U22	NC	-			U22	PR35B	3	C	
GND	-	-			GND	-	-			GND	GND3	3		
T22	NC	-			T22	NC	-			T22	PR35A	3	T	
R21	NC	-			R21	NC	-			R21	PR34B	3	C	
R22	NC	-			R22	NC	-			R22	PR34A	3	T	
P20	NC	-			P20	NC	-			P20	PR33B	3	C	
N20	NC	-			N20	NC	-			N20	PR33A	3	T	
P19	NC	-			P19	NC	-			P19	PR32B	3	C	
P18	NC	-			P18	NC	-			P18	PR32A	3	T	
P21	PR18B	3	C		P21	PR27B	3	C		P21	PR31B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
P22	PR18A	3	T		P22	PR27A	3	T		P22	PR31A	3	T	
N21	PR17B	3	C		N21	PR26B	3	C		N21	PR30B	3	C	

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A17	PT47A	1	T		A17	PT47A	1	T	
B15	PT46B	1	C		B15	PT46B	1	C	
A16	PT46A	1	T	TDQS46	A16	PT46A	1	T	TDQS46
A15	PT45B	1	C		A15	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
A14	PT45A	1	T		A14	PT45A	1	T	
G14	PT44B	1	C		G14	PT44B	1	C	
E15	PT44A	1	T		E15	PT44A	1	T	
D15	PT43B	1	C		D15	PT43B	1	C	
C15	PT43A	1	T		C15	PT43A	1	T	
C14	PT42B	1	C		C14	PT42B	1	C	
B14	PT42A	1	T		B14	PT42A	1	T	
A13	PT41B	1	C		A13	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
B13	PT41A	1	T		B13	PT41A	1	T	
E14	PT40B	1	C		E14	PT40B	1	C	
C13	PT40A	1	T		C13	PT40A	1	T	
F14	PT39B	1	C		F14	PT39B	1	C	
D14	PT39A	1	T		D14	PT39A	1	T	
E13	PT38B	1	C		E13	PT38B	1	C	
G13	PT38A	1	T	TDQS38	G13	PT38A	1	T	TDQS38
A12	PT37B	1	C		A12	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
B12	PT37A	1	T		B12	PT37A	1	T	
F13	PT36B	1	C		F13	PT36B	1	C	
D13	PT36A	1	T		D13	PT36A	1	T	
F12	PT35B	1	C	VREF2_1	F12	PT35B	1	C	VREF2_1
D12	PT35A	1	T	VREF1_1	D12	PT35A	1	T	VREF1_1
F11	PT34B	1	C		F11	PT34B	1	C	
C12	PT34A	1	T		C12	PT34A	1	T	
A11	PT33B	0	C	PCLKC0_0	A11	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A10	PT33A	0	T	PCLKT0_0	A10	PT33A	0	T	PCLKT0_0
E12	PT32B	0	C	VREF1_0	E12	PT32B	0	C	VREF1_0
E11	PT32A	0	T	VREF2_0	E11	PT32A	0	T	VREF2_0
B11	PT31B	0	C		B11	PT31B	0	C	
C11	PT31A	0	T		C11	PT31A	0	T	
B9	PT30B	0	C		B9	PT30B	0	C	
B10	PT30A	0	T	TDQS30	B10	PT30A	0	T	TDQS30
A9	PT29B	0	C		A9	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
A8	PT29A	0	T		A8	PT29A	0	T	
D11	PT28B	0	C		D11	PT28B	0	C	
C10	PT28A	0	T		C10	PT28A	0	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A21	PT51A	1	T		A21	PT51A	1	T	
E17	PT50B	1	C		E17	PT50B	1	C	
B17	PT50A	1	T		B17	PT50A	1	T	
C17	PT49B	1	C		C17	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
D17	PT49A	1	T		D17	PT49A	1	T	
F17	PT48B	1	C		F17	PT48B	1	C	
E20	PT48A	1	T		E20	PT48A	1	T	
G17	PT47B	1	C		G17	PT47B	1	C	
B20	PT47A	1	T		B20	PT47A	1	T	
E16	PT46B	1	C		E16	PT46B	1	C	
A20	PT46A	1	T	TDQS46	A20	PT46A	1	T	TDQS46
A19	PT45B	1	C		A19	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
B19	PT45A	1	T		B19	PT45A	1	T	
D16	PT44B	1	C		D16	PT44B	1	C	
C16	PT44A	1	T		C16	PT44A	1	T	
F16	PT43B	1	C		F16	PT43B	1	C	
A18	PT43A	1	T		A18	PT43A	1	T	
G16	PT42B	1	C		G16	PT42B	1	C	
B18	PT42A	1	T		B18	PT42A	1	T	
A17	PT41B	1	C		A17	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
A16	PT41A	1	T		A16	PT41A	1	T	
D15	PT40B	1	C		D15	PT40B	1	C	
B16	PT40A	1	T		B16	PT40A	1	T	
E15	PT39B	1	C		E15	PT39B	1	C	
C15	PT39A	1	T		C15	PT39A	1	T	
F15	PT38B	1	C		F15	PT38B	1	C	
G15	PT38A	1	T	TDQS38	G15	PT38A	1	T	TDQS38
B15	PT37B	1	C		B15	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
A15	PT37A	1	T		A15	PT37A	1	T	
E14	PT36B	1	C		E14	PT36B	1	C	
G14	PT36A	1	T		G14	PT36A	1	T	
D14	PT35B	1	C	VREF2_1	D14	PT35B	1	C	VREF2_1
E13	PT35A	1	T	VREF1_1	E13	PT35A	1	T	VREF1_1
F14	PT34B	1	C		F14	PT34B	1	C	
C14	PT34A	1	T		C14	PT34A	1	T	
B14	PT33B	0	C	PCLKC0_0	B14	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A14	PT33A	0	T	PCLKT0_0	A14	PT33A	0	T	PCLKT0_0

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A5	PT13B	0	C		A5	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
A4	PT13A	0	T		A4	PT13A	0	T	
F9	PT12B	0	C		F9	PT12B	0	C	
B6	PT12A	0	T		B6	PT12A	0	T	
E9	PT11B	0	C		E9	PT11B	0	C	
C8	PT11A	0	T		C8	PT11A	0	T	
G8	PT10B	0	C		G8	PT10B	0	C	
B5	PT10A	0	T		B5	PT10A	0	T	
A3	PT9B	0	C		A3	PT9B	0	C	
GND	GND0	0			GND	GND0	0		
A2	PT9A	0	T		A2	PT9A	0	T	
F8	PT8B	0	C		F8	PT8B	0	C	
B4	PT8A	0	T		B4	PT8A	0	T	
E8	PT7B	0	C		E8	PT7B	0	C	
B3	PT7A	0	T		B3	PT7A	0	T	
D8	PT6B	0	C		D8	PT6B	0	C	
G7	PT6A	0	T	TDQS6	G7	PT6A	0	T	TDQS6
C4	PT5B	0	C		C4	PT5B	0	C	
C5	PT5A	0	T		C5	PT5A	0	T	
E7	PT4B	0	C		E7	PT4B	0	C	
D4	PT4A	0	T		D4	PT4A	0	T	
F7	PT3B	0	C		F7	PT3B	0	C	
D6	PT3A	0	T		D6	PT3A	0	T	
D7	PT2B	0	C		D7	PT2B	0	C	
E6	PT2A	0	T		E6	PT2A	0	T	
GND	GND0	0			GND	GND0	0		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K15	GND	-			K15	GND	-		
K16	GND	-			K16	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L15	GND	-			L15	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		

LatticeECP Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFECP20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFECP20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFECP20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F672I	496	-3	fpBGA	672	IND	32.8K
LFECP33E-4F672I	496	-4	fpBGA	672	IND	32.8K
LFECP33E-3F484I	360	-3	fpBGA	484	IND	32.8K
LFECP33E-4F484I	360	-4	fpBGA	484	IND	32.8K

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFECP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFECP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFECP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFECP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFECP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFECP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFECP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFECP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFECP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFECP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFECP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFECP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFECP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC1E-3QN208I	112	-3	Lead-Free PQFP	208	IND	1.5K
LFEC1E-4QN208I	112	-4	Lead-Free PQFP	208	IND	1.5K
LFEC1E-3TN144I	97	-3	Lead-Free TQFP	144	IND	1.5K
LFEC1E-4TN144I	97	-4	Lead-Free TQFP	144	IND	1.5K
LFEC1E-3TN100I	67	-3	Lead-Free TQFP	100	IND	1.5K
LFEC1E-4TN100I	67	-4	Lead-Free TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC3E-3FN256I	160	-3	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-4FN256I	160	-4	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-3QN208I	145	-3	Lead-Free PQFP	208	IND	3.1K
LFEC3E-4QN208I	145	-4	Lead-Free PQFP	208	IND	3.1K
LFEC3E-3TN144I	97	-3	Lead-Free TQFP	144	IND	3.1K
LFEC3E-4TN144I	97	-4	Lead-Free TQFP	144	IND	3.1K
LFEC3E-3TN100I	67	-3	Lead-Free TQFP	100	IND	3.1K
LFEC3E-4TN100I	67	-4	Lead-Free TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K