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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

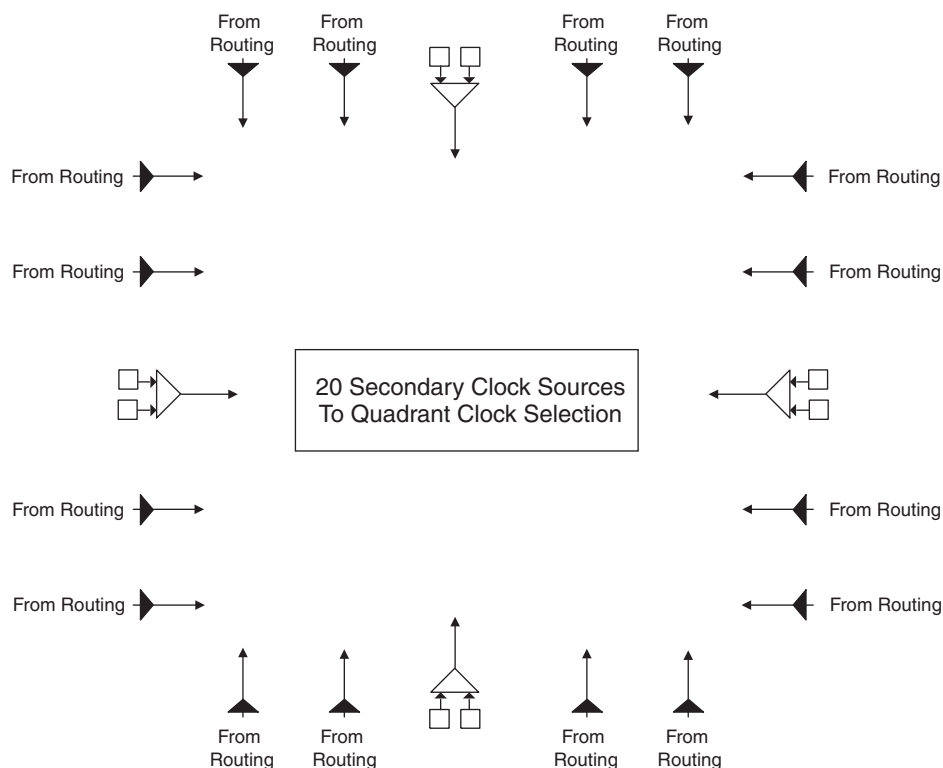
Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15400
Total RAM Bits	358400
Number of I/O	352
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec15e-3fn484i

Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

Figure 2-7. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master clock for configuration. The oscillator and the master clock run continuously. The default value of the master clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information about the use of this oscillator for configuration, please see the list of technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5*	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold		+/-100	—	—	mV
V_{CM}	Input common mode voltage	100mV δ V_{THD}	$V_{THD}/2$	1.2	1.8	V
		200mV δ V_{THD}	$V_{THD}/2$	1.2	1.9	V
		350mV δ V_{THD}	$V_{THD}/2$	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	μ A
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM})$, $R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} + V_{OM})/2$, $R_T = 100$ Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0$ V Driver outputs shorted	—	—	6	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

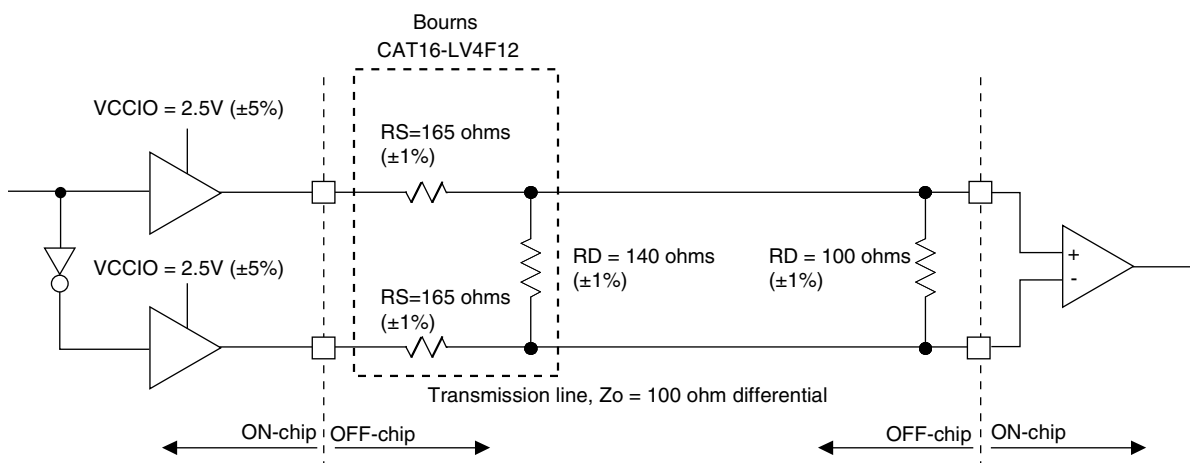


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.42	V
V_{OL}	Output low voltage	1.08	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	$\%$

LatticeECP/EC Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.25	—	0.31	—	0.36	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.40	—	0.48	—	0.56	ns
t _{LSR_PFU}	Set/Reset to Output of PFU	—	0.81	—	0.98	—	1.14	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.05	—	-0.06	—	-0.06	—	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HD_PFU}	Clock to D Input Hold time	-0.03	—	-0.03	—	-0.04	—	ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.36	—	0.44	—	0.51	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.48	—	0.58	—	0.68	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.50	—	0.60	—	0.69	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output	—	0.36	—	0.44	—	0.51	ns
t _{SUDATA_PFU}	Data Setup Time	-0.20	—	-0.24	—	-0.28	—	ns
t _{HDATA_PFU}	Data Hold Time	0.26	—	0.31	—	0.36	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.51	—	-0.62	—	-0.72	—	ns
t _{HADDR_PFU}	Address Hold Time	0.64	—	0.77	—	0.90	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.24	—	-0.29	—	-0.34	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.30	—	0.36	—	0.42	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay	—	0.56	—	0.67	—	0.78	ns
t _{OUT_PIO}	Output Buffer Delay	—	1.92	—	2.31	—	2.69	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.90	—	1.08	—	1.26	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.62	—	0.74	—	0.87	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.33	—	0.40	—	0.46	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.10	—	-0.12	—	-0.14	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.12	—	0.14	—	0.17	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.18	—	0.21	—	0.25	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.15	—	-0.18	—	-0.21	—	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data	—	3.64	—	4.37	—	5.10	ns
t _{COO_EBR}	Clock to Output from EBR output Register	—	0.74	—	0.88	—	1.03	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.18	—	-0.22	—	-0.26	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.23	—	0.28	—	0.33	—	ns

LatticeECP/EC Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUC_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.14	—	-0.17	—	-0.20	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t_{SUI_DSP}	Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HI_DSP}	Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.31	—	3.98	—	4.64	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{SUO_DSP}^4$	Output Register Setup Time	5.54	—	6.64	—	7.75	—	ns
$t_{HO_DSP}^4$	Output Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{COI_DSP}^4$	Input Register Clock to Output Time	—	7.50	—	9.00	—	10.50	ns
$t_{COP_DSP}^4$	Pipeline Register Clock to Output Time	—	4.66	—	5.60	—	6.53	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	1.47	—	1.77	—	2.06	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.

4. These parameters include the Adder Subtractor block in the path.

Timing v.G 0.30

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	210	MHz
f_{VCO}	PLL VCO Frequency		420	—	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Elected ³	45	50	55	%
t_{PH}^4	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	—	150	μs
t_{PA}	Programmable Delay Unit		100	250	450	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDL}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

Timing v.G 0.30

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data out pin used to shift data out of device using 1149.1.
V _{CCJ}	—	V _{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (Active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSO	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPIN	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes.

Pin Information Summary

		LFEC1			LFEC3				LFEC6/EC6				LFEC6/EC10		
Pin Type		100-TQFP	144-TQFP	208-PQFP	100-TQFP	144-TQFP	208-PQFP	256-fpBGA	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	208-PQFP	256-fpBGA	484-fpBGA
Single Ended User I/O		67	97	112	67	97	145	160	97	147	195	224	147	195	288
Differential Pair User I/O		29	46	56	29	46	72	80	46	72	97	112	72	97	144
Configuration	Dedicated	13	13	13	13	13	13	13	13	13	13	13	13	13	13
	Muxed	48	48	48	48	48	48	48	48	48	48	48	56	56	56
TAP		5	5	5	5	5	5	5	5	5	5	5	5	5	5
Dedicated (total without supplies)		80	110	160	80	110	160	208	110	160	208	373	160	208	373
V _{CC}		2	3	3	2	3	3	10	4	4	10	20	6	10	20
V _{CCAUX}		2	2	2	4	4	4	4	2	4	2	12	4	2	12
V _{CCPLL}		0	0	0	0	0	0	0	0	0	0	0	0	0	0
V _{CCIO}	Bank0	1	2	2	1	2	3	2	2	3	2	4	3	2	4
	Bank1	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank2	1	1	1	2	2	2	2	1	2	2	4	2	2	4
	Bank3	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank4	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank5	1	2	2	1	2	2	2	2	3	2	4	3	2	4
	Bank6	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank7	1	1	1	2	2	2	2	1	2	2	4	2	2	4
GND, GND0-GND7		8	13	13	8	13	16	20	14	18	20	44	20	20	44
NC		0	2	51	0	2	9	35	0	4	0	139	0	0	75
Single Ended/Differential I/O Pair per Bank	Bank 0	11/5	14/7	16/8	11/5	14/7	26/13	32/16	14/7	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 1	11/5	13/6	16/8	11/5	13/6	16/8	16/8	13/6	17/8	18/9	32/16	17/8	18/9	32/16
	Bank 2	3/1	8/4	8/4	3/1	8/4	14/7	16/8	8/4	14/7	16/8	16/8	14/7	16/8	32/16
	Bank 3	8/4	13/6	16/8	8/4	13/6	16/8	16/8	13/6	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 4	12/4	14/6	16/8	12/4	14/6	16/8	16/8	14/6	17/8	17/8	32/16	17/8	17/8	32/16
	Bank 5	9/4	13/6	16/8	9/4	13/6	26/13	32/16	13/6	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 6	5/2	14/7	16/8	5/2	14/7	16/8	16/8	14/7	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 7	8/4	8/4	8/4	8/4	8/4	15/7	16/8	8/4	15/7	16/8	16/8	15/7	16/8	32/16
V _{CCJ}		1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC6P/EC6, LFEC6P/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC6P/EC6				LFEC6P/EC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB18A	4	T	WRITEN	PB26A	4	T	WRITEN
87	PB18B	4	C	CS1N	PB26B	4	C	CS1N
88	PB19A	4	T	VREF1_4	PB27A	4	T	VREF1_4
89	PB19B	4	C	CSN	PB27B	4	C	CSN
90	PB20A	4	T	VREF2_4	PB28A	4	T	VREF2_4
91	PB20B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
92	PB21A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB21B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
95	PB22A	4	T	BDQS22	PB30A	4	T	BDQS30
96	PB22B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
97	PB23A	4	T		PB31A	4	T	
98	PB23B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
99	PB24A	4	T		PB32A	4	T	
100	PB24B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
101	PB25A	4	T		PB33A	4	T	
102	PB25B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
103	PB33A	4			PB41A	4		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR27B	3	C	VREF2_3	PR36B	3	C	VREF2_3
108	PR27A	3	T	VREF1_3	PR36A	3	T	VREF1_3
109	PR26B	3	C		PR35B	3	C	
110	PR26A	3	T		PR35A	3	T	
111	PR25B	3	C		PR34B	3	C	
112	PR25A	3	T		PR34A	3	T	
113	PR24B	3	C		PR33B	3	C	
114	PR24A	3	T	RDQS24	PR33A	3	T	RDQS33
115	PR23B	3	C	RLM0_PLLC_FB_A	PR32B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR23A	3	T	RLM0_PLLT_FB_A	PR32A	3	T	RLM0_PLLT_FB_A
118	PR22B	3	C	RLM0_PLLC_IN_A	PR31B	3	C	RLM0_PLLC_IN_A
119	PR22A	3	T	RLM0_PLLT_IN_A	PR31A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR21B	3	C	DI/CSSPIN	PR30B	3	C	DI/CSSPIN
122	PR21A	3	T	DOUT/CSON	PR30A	3	T	DOUT/CSON
123	PR20B	3	C	BUSY/SISPI	PR29B	3	C	BUSY/SISPI
124	PR20A	3	T	D7/SPID0	PR29A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

LFEC10/EC10 and LFEC15/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC10/LFEC10				LFEC15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
P14	PR35B	3	C		PR43B	3	C	
P15	PR35A	3	T		PR43A	3	T	
R15	PR34B	3	C		PR42B	3	C	
R16	PR34A	3	T		PR42A	3	T	
M13	PR33B	3	C		PR41B	3	C	
M14	PR33A	3	T	RDQS33	PR41A	3	T	RDQS41
P16	PR32B	3	C	RLM0_PLLC_FB_A	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		
N16	PR32A	3	T	RLM0_PLLT_FB_A	PR40A	3	T	RLM0_PLLT_FB_A
N15	PR31B	3	C	RLM0_PLLC_IN_A	PR39B	3	C	RLM0_PLLC_IN_A
M15	PR31A	3	T	RLM0_PLLT_IN_A	PR39A	3	T	RLM0_PLLT_IN_A
M16	PR30B	3	C	DI/CSSPIN	PR38B	3	C	DI/CSSPIN
L16	PR30A	3	T	DOUT/CSON	PR38A	3	T	DOUT/CSON
K16	PR29B	3	C	BUSY/SISPI	PR37B	3	C	BUSY/SISPI
J16	PR29A	3	T	D7/SPID0	PR37A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
GND	GND3	3			GND3	3		
H16	PR27B	3	C		PR31B	3	C	
-	-	-			GND3	3		
H15	PR27A	3	T		PR31A	3	T	
G16	PR26B	3	C		PR30B	3	C	
G15	PR26A	3	T		PR30A	3	T	
K12	PR25B	3	C		PR29B	3	C	
J12	PR25A	3	T		PR29A	3	T	
J14	PR24B	3	C		PR28B	3	C	
J15	PR24A	3	T	RDQS24	PR28A	3	T	RDQS28
F16	PR23B	3	C		PR27B	3	C	
GND	GND3	3			GND3	3		
F15	PR23A	3	T		PR27A	3	T	
J13	PR22B	3	C		PR26B	3	C	
H13	PR22A	3	T		PR26A	3	T	
H14	PR21B	3	C		PR25B	3	C	
G14	PR21A	3	T		PR25A	3	T	
E16	PR20B	3	C		PR24B	3	C	
E15	PR20A	3	T		PR24A	3	T	
H12	PR18B	2	C	PCLKC2_0	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND2	2		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G12	PR18A	2	T	PCLKT2_0	PR22A	2	T	PCLKT2_0
G13	PR17B	2	C		PR21B	2	C	
F13	PR17A	2	T		PR21A	2	T	
F12	PR16B	2	C		PR20B	2	C	
E13	PR16A	2	T		PR20A	2	T	
D16	PR15B	2	C		PR19B	2	C	
D15	PR15A	2	T		PR19A	2	T	RDQS19
F14	PR14B	2	C		PR18B	2	C	
GND	GND2	2			GND2	2		
E14	PR14A	2	T		PR18A	2	T	
C16	PR13B	2	C		PR17B	2	C	
B16	PR13A	2	T		PR17A	2	T	
C15	PR12B	2	C		PR16B	2	C	
C14	PR12A	2	T		PR16A	2	T	
GND	GND2	2			GND2	2		
-	-	-			GND2	2		
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
-	-	-			GND1	1		
B13	PT34B	1	C		PT34B	1	C	
C13	PT34A	1	T		PT34A	1	T	
C12	PT33B	1	C		PT33B	1	C	
GND	GND1	1			GND1	1		
D12	PT33A	1	T		PT33A	1	T	
A15	PT32B	1	C		PT32B	1	C	
B14	PT32A	1	T		PT32A	1	T	
D11	PT31B	1	C		PT31B	1	C	
C11	PT31A	1	T		PT31A	1	T	
E10	PT30B	1	C		PT30B	1	C	
E11	PT30A	1	T	TDQS30	PT30A	1	T	TDQS30
A14	PT29B	1	C		PT29B	1	C	
GND	GND1	1			GND1	1		
A13	PT29A	1	T		PT29A	1	T	
D10	PT28B	1	C		PT28B	1	C	
C10	PT28A	1	T		PT28A	1	T	
A12	PT27B	1	C	VREF2_1	PT27B	1	C	VREF2_1
B12	PT27A	1	T	VREF1_1	PT27A	1	T	VREF1_1
A11	PT26B	1	C		PT26B	1	C	
B11	PT26A	1	T		PT26A	1	T	

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR9A	2	T	RUM0_PLLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR8A	2	T	RUM0_PLLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC15/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
T11	VCCIO5	5			T11	VCCIO5	5			T11	VCCIO5	5		
M7	VCCIO6	6			M7	VCCIO6	6			M7	VCCIO6	6		
M8	VCCIO6	6			M8	VCCIO6	6			M8	VCCIO6	6		
N8	VCCIO6	6			N8	VCCIO6	6			N8	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6			P8	VCCIO6	6		
J8	VCCIO7	7			J8	VCCIO7	7			J8	VCCIO7	7		
K8	VCCIO7	7			K8	VCCIO7	7			K8	VCCIO7	7		
L7	VCCIO7	7			L7	VCCIO7	7			L7	VCCIO7	7		
L8	VCCIO7	7			L8	VCCIO7	7			L8	VCCIO7	7		
G15	VCCAUX	-			G15	VCCAUX	-			G15	VCCAUX	-		
G16	VCCAUX	-			G16	VCCAUX	-			G16	VCCAUX	-		
G7	VCCAUX	-			G7	VCCAUX	-			G7	VCCAUX	-		
G8	VCCAUX	-			G8	VCCAUX	-			G8	VCCAUX	-		
H16	VCCAUX	-			H16	VCCAUX	-			H16	VCCAUX	-		
H7	VCCAUX	-			H7	VCCAUX	-			H7	VCCAUX	-		
R16	VCCAUX	-			R16	VCCAUX	-			R16	VCCAUX	-		
R7	VCCAUX	-			R7	VCCAUX	-			R7	VCCAUX	-		
T15	VCCAUX	-			T15	VCCAUX	-			T15	VCCAUX	-		
T16	VCCAUX	-			T16	VCCAUX	-			T16	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-			T8	VCCAUX	-		
J6	VCC	-			J6	VCC	-			J6	VCC	-		
J17	VCC	-			J17	VCC	-			J17	VCC	-		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
P17	VCC	-			P17	VCC	-			P17	VCC	-		
A2	NC	-			A2	NC	-			A2	NC	-		
AB2	NC	-			AB2	NC	-			AB2	NC	-		
A21	NC	-			A21	NC	-			A21	NC	-		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
J14	VCCIO1	1			J14	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
J16	VCCIO1	1			J16	VCCIO1	1		
J17	VCCIO1	1			J17	VCCIO1	1		
K17	VCCIO2	2			K17	VCCIO2	2		
K18	VCCIO2	2			K18	VCCIO2	2		
L18	VCCIO2	2			L18	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
N18	VCCIO2	2			N18	VCCIO2	2		
N19	VCCIO2	2			N19	VCCIO2	2		
P18	VCCIO3	3			P18	VCCIO3	3		
P19	VCCIO3	3			P19	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
R19	VCCIO3	3			R19	VCCIO3	3		
T18	VCCIO3	3			T18	VCCIO3	3		
U18	VCCIO3	3			U18	VCCIO3	3		
V14	VCCIO4	4			V14	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
V16	VCCIO4	4			V16	VCCIO4	4		
V17	VCCIO4	4			V17	VCCIO4	4		
W14	VCCIO4	4			W14	VCCIO4	4		
W15	VCCIO4	4			W15	VCCIO4	4		
V10	VCCIO5	5			V10	VCCIO5	5		
V11	VCCIO5	5			V11	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
V13	VCCIO5	5			V13	VCCIO5	5		
W12	VCCIO5	5			W12	VCCIO5	5		
W13	VCCIO5	5			W13	VCCIO5	5		
P8	VCCIO6	6			P8	VCCIO6	6		
P9	VCCIO6	6			P9	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T9	VCCIO6	6			T9	VCCIO6	6		
U9	VCCIO6	6			U9	VCCIO6	6		
K9	VCCIO7	7			K9	VCCIO7	7		
L9	VCCIO7	7			L9	VCCIO7	7		
M8	VCCIO7	7			M8	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
N8	VCCIO7	7			N8	VCCIO7	7		
N9	VCCIO7	7			N9	VCCIO7	7		
G13	VCCAUX	-			G13	VCCAUX	-		
H20	VCCAUX	-			H20	VCCAUX	-		

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFEC10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFEC10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFEC10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFEC10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFEC15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFEC15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFEC15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFEC15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFEC15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFEC20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFEC20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFEC20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFEC20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFEC20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFEC33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFEC33E-5F672C	496	-5	fpBGA	672	COM	32.8K
LFEC33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFEC33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFEC33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFECP33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFECP33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3T100I	67	-3	TQFP	100	IND	1.5K
LFEC1E-4T100I	67	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256I	160	-3	fpBGA	256	IND	3.1K
LFEC3E-4F256I	160	-4	fpBGA	256	IND	3.1K
LFEC3E-3Q208I	145	-3	PQFP	208	IND	3.1K
LFEC3E-4Q208I	145	-4	PQFP	208	IND	3.1K
LFEC3E-3T144I	97	-3	TQFP	144	IND	3.1K
LFEC3E-4T144I	97	-4	TQFP	144	IND	3.1K
LFEC3E-3T100I	67	-3	TQFP	100	IND	3.1K
LFEC3E-4T100I	67	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3 P208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4 P208I	147	-4	PQFP	208	IND	10.2K

Date	Version	Section	Change Summary
December 2004	01.4	Architecture	Updated Hot Socketing Recommended Power Up Sequence section.
		Pinout Information	Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Pin Information
			Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Power Supply and NC Connections
			Added LFEC1 and LFEC3 100 TQFP Pinout
			Added LFEC1 and LFEC3 144 TQFP Pinout
			Added LFEC1, LFEC3 and LFECP/EC10 208 PQFP Pinout
			Added LFEC3, LFECP/EC10 and LFECP/EC15 256 fpBGA Pinout
			Added LFECP/EC10 and LFECP/EC15 484 fpBGA Pinout
		Ordering Information	Added Lead-Free Package Designators
			Added Lead-Free Ordering Part Numbers
		Supplemental Information	Updated list of technical notes.
April 2005	01.5	Architecture	EBR memory support section has been updated with clarification.
			Updated sysIO buffer pair section.
		DC & Switching Characteristics	Hot Socketing Specification has been updated.
			DC Electrical Characteristics table (I_{IL} , I_{IH}) has been updated.
			Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			External Switching Characteristics section has been updated.
			Removed t_{RSTW} spec. from PLL Parameter table.
			t_{RST} specifications have been updated.
			sysCONFIG Port Timing Specifications (t_{BSCL} , t_{ODISS} , t_{PRGMRJ}) have been updated.
		Pinout Information	Added LFECP/EC33 Pinout Information
			Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
			484-fpBGA logic connection has been updated (Ball # J6, J17, P6 and P17 for ECP/EC33 are now called VCCPLL).
			672-fpBGA logic connection has been updated (Ball # K19, L8, U19, U8 for ECP/EC33 are now called VCCPLL).
May 2005	01.6	Introduction	ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.
		Architecture	Table 2-10 has been updated (ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.)
			Recommended Power Up Sequence section has been removed.
		DC & Switching Characteristics	Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			Vos test condition has been updated to $(VOP+VOM)/2$.
			Register-to-Register performance table has been updated (rev. G 0.27).
			External switching characteristics have been updated (rev. G 0.27).
			Internal timing parameters have been updated (rev. G 0.27).
			Timing adders have been updated (rev. G 0.27).
			sysCONFIG port timing specifications have been updated.
		Pinout Information	Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	OPN list has been updated.