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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15400
Total RAM Bits	358400
Number of I/O	352
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec15e-4fn484i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec15e-4fn484i</a>

## Features

### ■ Extensive Density and Package Options

- 1.5K to 32.8K LUT4s
- 65 to 496 I/Os
- Density migration supported

### ■ sysDSP™ Block (LatticeECP™ Versions)

- High performance multiply and accumulate
- 4 to 8 blocks
  - 4 to 8 36x36 multipliers or
  - 16 to 32 18x18 multipliers or
  - 32 to 64 9x9 multipliers

### ■ Embedded and Distributed Memory

- 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
- Up to 131 Kbits distributed RAM
- Flexible memory resources:
  - Distributed and block memory

### ■ Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:

- LVCMOS 3.3/2.5/1.8/1.5/1.2
- LVTTTL
- SSTL 3/2 Class I, II, SSTL18 Class I
- HSTL 18 Class I, II, III, HSTL15 Class I, III
- PCI
- LVDS, Bus-LVDS, LVPECL, RSDS

### ■ Dedicated DDR Memory Support

- Implements interface up to DDR400 (200MHz)

### ■ sysCLOCK™ PLLs

- Up to four analog PLLs per device
- Clock multiply, divide and phase shifting

### ■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- SPI boot flash interface
- 1.2V power supply

### ■ Low Cost FPGA

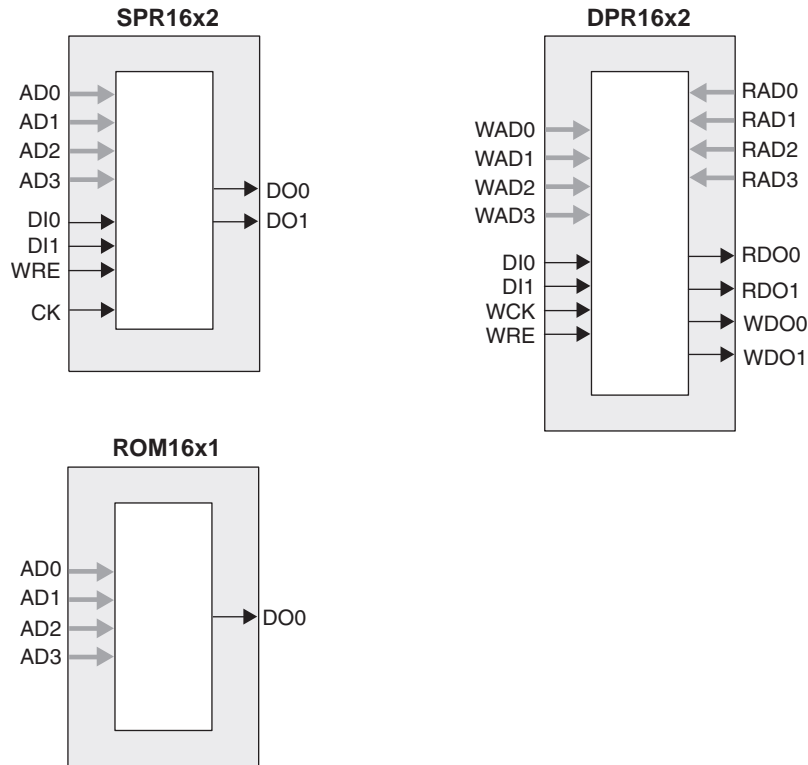
- Features optimized for mainstream applications
- Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFCEP6	LFEC10/ LFCEP10	LFEC15/ LFCEP15	LFEC20/ LFCEP20	LFEC33/ LFCEP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks <sup>1</sup>	—	—	4	5	6	7	8
18x18 Multipliers <sup>1</sup>	—	—	16	20	24	28	32
V <sub>CC</sub> Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
<b>Packages and I/O Combinations:</b>							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Figure 2-5. Distributed Memory Primitives



**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM <sup>1</sup>	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

**Table 2-5. PLL Signal Descriptions**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

## Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

**Figure 2-13. DCS Block Primitive**

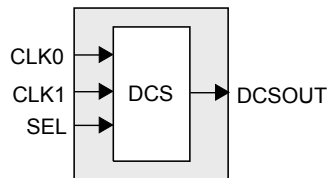
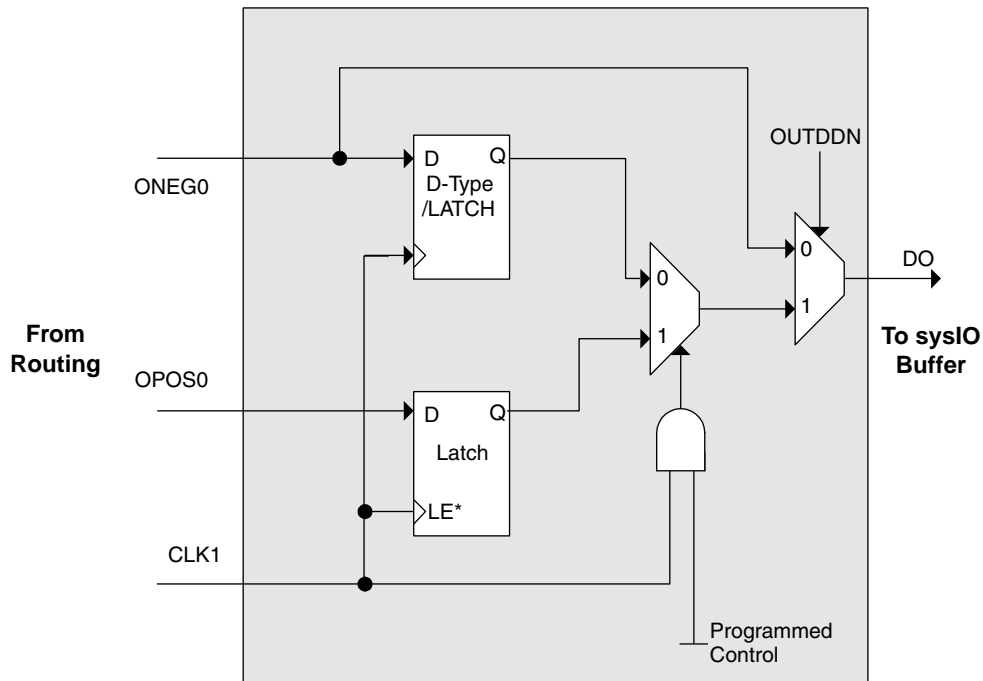


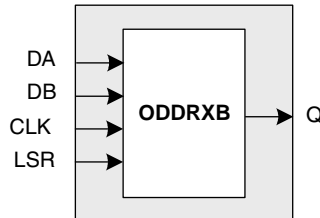
Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Figure 2-29. Output Register Block



\*Latch is transparent when input is low.

Figure 2-30. ODDRXB Primitive



**Tristate Register Block**

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

Supply Voltage $V_{CC}$ . . . . .	-0.5 to 1.32V
Supply Voltage $V_{CCAUX}$ . . . . .	-0.5 to 3.75V
Supply Voltage $V_{CCJ}$ . . . . .	-0.5 to 3.75V
Output Supply Voltage $V_{CCIO}$ . . . . .	-0.5 to 3.75V
Dedicated Input Voltage Applied <sup>4</sup> . . . . .	-0.5 to 4.25V
I/O Tristate Voltage Applied <sup>4</sup> . . . . .	-0.5 to 3.75V
Storage Temperature (Ambient) . . . . .	-65 to 150°C
Junction Temp. (Tj) . . . . .	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ( $V_{IHMAX} + 2$ ) volts is permitted for a duration of <20ns.

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^3$	Auxiliary Supply Voltage	3.135	3.465	V
$V_{CCPLL}$	PLL Supply Voltage for ECP/EC33	1.14	1.26	V
$V_{CCIO}^{1,2}$	I/O Driver Supply Voltage	1.140	3.465	V
$V_{CCJ}^1$	Supply Voltage for IEEE 1149.1 Test Access Port	1.140	3.465	V
$t_{JCOM}$	Junction Commercial Operation	0	85	°C
$t_{JIND}$	Junction Industrial Operation	-40	100	°C

1. If  $V_{CCIO}$  or  $V_{CCJ}$  is set to 1.2V, they must be connected to the same power supply as  $V_{CC}$ . If  $V_{CCIO}$  or  $V_{CCJ}$  is set to 3.3V, they must be connected to the same power supply as  $V_{CCAUX}$ .
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCAUX}$  ramp rate must not exceed 3mV/ $\mu$ s for commercial and 0.6 mV/ $\mu$ s for industrial device operations during power up when transitioning between 0.8V and 1.8V.

### Hot Socketing Specifications<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>Top and Bottom General Purpose sysI/Os (Banks 0, 1, 4 and 5), JTAG and Dedicated sysCONFIG Pins</b>						
$I_{DK\_TB}$	Input or I/O Leakage Current	$0 \delta V_{IN} \delta V_{IH} (MAX.)$	—	—	+/-1000	$\mu$ A
<b>Left and Right General Purpose sysI/Os (Banks 2, 3, 6 and 7)</b>						
$I_{DK\_LR}$	Input or I/O Leakage Current	$V_{IN} \delta V_{CCIO}$	—	—	+/-1000	$\mu$ A
		$V_{IN} > V_{CCIO}$	—	35	—	mA

1. Insensitive to sequence of  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ .
2.  $0 \delta V_{CC} \delta V_{CC} (MAX)$ ,  $0 \delta V_{CCIO} \delta V_{CCIO} (MAX)$  or  $0 \delta V_{CCAUX} \delta V_{CCAUX} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ .
4. LVCMOS and LVTTTL only.

**sysI/O Single-Ended DC Electrical Characteristics**

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}^1$ (mA)	$I_{OH}^1$ (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
SSTL18 class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
HSTL15 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL15 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8
HSTL18 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	9.6	-9.6
HSTL18 class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL18 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed  $n * 8\text{mA}$ . Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

## Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics ( $\Theta_{JA}$ ), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables:  $T_J$  °C.

**Table 3-5. Delay Derating Table for Internal Blocks**

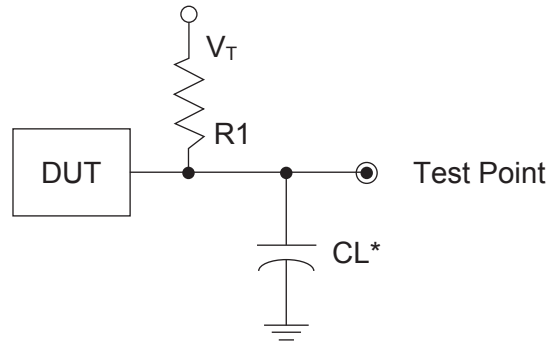
$T_J$ °C Commercial	$T_J$ °C Industrial	Power Supply Voltage		
		1.14V	1.2V	1.26V
—	-40	0.82	0.77	0.71
—	-25	0.82	0.76	0.71
0	20	0.89	0.83	0.78
25	45	0.93	0.87	0.81
85	105	1.00	0.94	0.89



## Switching Test Conditions

Figure 3-21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

**Figure 3-21. Output Test Load, LVTTTL and LVCMOS Standards**



\*CL Includes Test Fixture and Probe Capacitance

**Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> H)	188 <sup>3/4</sup>	0pF	V <sub>CCIO</sub> /2	V <sub>OL</sub>
LVCMOS 2.5 I/O (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVCMOS 2.5 I/O (H -> Z)			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVCMOS 2.5 I/O (L -> Z)			V <sub>OL</sub> + 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

**Power Supply and NC Connections (Cont.)**

Signals	484 fpBGA	672 fpBGA
VCC	J16, J7, K16, K17, K6, K7, L17, L6, M17, M6, N16, N17, N6, N7, P16, P7, J6, J17, P6, P17	H10, H11, H16, H17, H18, H19, H8, H9, J18, J9, K8, L19, M19, N7, R20, R7, T19, V18, V8, V9, W10, W11, W16, W17, W18, W19, W8, W9, K19, L8, U19, U8
VCCIO0	G11, H10, H11, H9	H12, H13, J10, J11, J12, J13
VCCIO1	G12, H12, H13, H14	H14, H15, J14, J15, J16, J17
VCCIO2	J15, K15, L15, L16	K17, K18, L18, M18, N18, N19
VCCIO3	M15, M16, N15, P15	P18, P19, R18, R19, T18, U18
VCCIO4	R12, R13, R14, T12	V14, V15, V16, V17, W14, W15
VCCIO5	R10, R11, R9, T11	V10, V11, V12, V13, W12, W13
VCCIO6	M7, M8, N8, P8	P8, P9, R8, R9, T9, U9
VCCIO7	J8, K8, L7, L8	K9, L9, M8, M9, N8, N9
VCCJ	U2	U6
VCCAUX	G15, G16, G7, G8, H16, H7, R16, R7, T15, T16, T7, T8	G13, H20, H7, J19, J8, K7, L20, M20, M7, N20, P20, P7, T20, T7, T8, V19, V7, W20, Y13, Y7
VCCPLL	<b>ECP/EC20:</b> None <b>ECP/EC33:</b> J6, J17, P6, P17	<b>ECP/EC20:</b> None <b>ECP/EC33:</b> K19, L8, U19, U8
GND, GND0-GND7	A1, A22, AB1, AB22, H15, H8, J10, J11, J12, J13, J14, J9, K10, K11, K12, K13, K14, K9, L10, L11, L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R15, R8	K10, K11, K12, K13, K14, K15, K16, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17
NC	<b>ECP/EC6:</b> C3, B2, E5, F5, D3, C2, F4, G4, E3, D2, B1, C1, F3, E2, G5, H6, G3, H4, J5, H5, F2, F1, E1, D1, R6, P5, P3, P4, R1, R2, R5, R4, T1, T2, R3, T3, V7, T6, V8, U7, W5, U6, AA3, AB3, Y6, V6, AA5, W6, Y5, Y4, AA4, AB4, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, E21, D22, G21, G20, J18, H19, J19, H20, H17, H18, D21, C22, G19, G18, F20, F19, E20, D20, C21, C20, F18, E18, B22, B21, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A4, B4, C4, C5, D6, B5, E6, C6, A3, B3, F6, D5, F7, E8, G6, E7, A2, AB2, A21 <b>ECP/EC10:</b> G5, H6, G3, H4, J5, H5, F2, F1, R6, P5, P3, P4, R2, R1, R5, R4, T1, T2, R3, T3, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, G21, G20, J18, H19, J19, H20, H17, H18, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A2, AB2, A21 <b>ECP/EC15:</b> T1, T2, R3, T3, T18, R17, R19, R18, A2, AB2, A21 <b>ECP/EC20:</b> A2, AB2, A21 <b>ECP/EC33:</b> A2, AB2, A21	<b>ECP/EC20:</b> E5, D5, F4, F5, C3, D3, C2, B2, H6, J7, G5, H5, H3, J3, H2, J2, AA2, AA3, W5, Y5, Y6, W7, AA4, AB3, AC2, AC3, AA5, AB5, AD3, AD2, AE1, AD1, AD19, AD20, AC19, AB19, AD21, AC20, AF25, AE25, AB21, AB20, AE24, AD23, AD22, AC21, AC22, AB22, AD24, AD25, AE26, AD26, Y20, Y19, AA23, AA22, AB23, AB24, Y21, AA21, Y23, Y22, AA24, Y24, J21, J22, J23, H22, G26, F26, E26, E25, F24, F23, E24, D24, E22, F22, E21, D22, G20, F20, D21, C21, C23, C22, B23, C24, D20, E19, B25, B24, B26, A25, C20, C19 <b>ECP/EC33:</b> None

**LFEC1, LFEC3 Logic Signal Connections: 100 TQFP**

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	PL3A	7	T		PL7A	7	T	
6	PL3B	7	C		PL7B	7	C	
7	PL4A	7	T		PL8A	7	T	
8	PL4B	7	C		PL8B	7	C	
9	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
10	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
11	XRES	6			XRES	6		
12	VCC	-			VCC	-		
13	TCK	6			TCK	6		
14	GND	-			GND	-		
15	TDI	6			TDI	6		
16	TMS	6			TMS	6		
17	TDO	6			TDO	6		
18	VCCJ	6			VCCJ	6		
19	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LUM0_PLLT_IN_A
20	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LUM0_PLLC_IN_A
21	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LUM0_PLLT_FB_A
22	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LUM0_PLLC_FB_A
23	PL14A	6		VREF1_6	PL18A	6		VREF1_6
24	VCCIO6	6			VCCIO6	6		
25*	GND5 GND6	-			GND5 GND6	-		
26	VCCIO5	5			VCCIO5	5		
27	PB2A	5	T		PB10A	5	T	
28	PB2B	5	C		PB10B	5	C	
29	PB3A	5	T		PB11A	5	T	
30	PB3B	5	C		PB11B	5	C	
31	PB6A	5		BDQS6	PB14A	5		BDQS14
32	PB8A	5	T	VREF2_5	PB16A	5	T	VREF2_5
33	PB8B	5	C	VREF1_5	PB16B	5	C	VREF1_5
34	PB9A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
35	GND5	5			GND5	5		
36	PB9B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
37	VCCAUX	-			VCCAUX	-		
38	VCCIO4	4			VCCIO4	4		
39	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN
40	PB10B	4	C	CS1N	PB18B	4	C	CS1N

**LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN
87	PB10B	4	C	CS1N	PB18B	4	C	CS1N
88	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
89	PB11B	4	C	CSN	PB19B	4	C	CSN
90	PB12A	4	T	VREF2_4	PB20A	4	T	VREF2_4
91	PB12B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
92	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
95	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
96	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
97	PB15A	4	T		PB23A	4	T	
98	PB15B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
99	PB16A	4	T		PB24A	4	T	
100	PB16B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
101	PB17A	4	T		PB25A	4	T	
102	PB17B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
103	NC	-			NC	-		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR14B	3	C	VREF2_3	PR18B	3	C	VREF2_3
108	PR14A	3	T	VREF1_3	PR18A	3	T	VREF1_3
109	PR13B	3	C		PR17B	3	C	
110	PR13A	3	T		PR17A	3	T	
111	PR12B	3	C		PR16B	3	C	
112	PR12A	3	T		PR16A	3	T	
113	PR11B	3	C		PR15B	3	C	
114	PR11A	3	T	RDQS11	PR15A	3	T	RDQS15
115	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
118	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
119	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
122	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
123	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
124	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

**LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)**

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

**LFCEP/EC20 and LFCEP/EC33 Logic Signal Connections: 484 fpBGA**

LFCEP20/LFCEP20					LFCEP/LFCEP33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
GND	-	-			GND	GND7	7		
C3	PL3A	7	T		C3	PL10A	7	T	
B2	PL3B	7	C		B2	PL10B	7	C	
E5	PL4A	7	T		E5	PL11A	7	T	
F5	PL4B	7	C		F5	PL11B	7	C	
D3	PL5A	7	T		D3	PL12A	7	T	
C2	PL5B	7	C		C2	PL12B	7	C	
GND	-	-			GND	GND7	7		
F4	PL6A	7	T	LDQS6	F4	PL14A	7	T	LDQS14
G4	PL6B	7	C		G4	PL14B	7	C	
E3	PL7A	7	T		E3	PL15A	7	T	
D2	PL7B	7	C		D2	PL15B	7	C	
B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL16A	7	T	LUM0_PLLT_IN_A
C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL16B	7	C	LUM0_PLLC_IN_A
F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL17B	7	C	LUM0_PLLC_FB_A
GND	-	-			GND	GND7	7		
G5	PL11A	7	T		G5	PL23A	7	T	LDQS23
H6	PL11B	7	C		H6	PL23B	7	C	
G3	PL12A	7	T		G3	PL24A	7	T	
H4	PL12B	7	C		H4	PL24B	7	C	
J5	PL13A	7	T		J5	PL25A	7	T	
H5	PL13B	7	C		H5	PL25B	7	C	
F2	PL14A	7	T		F2	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
F1	PL14B	7	C		F1	PL26B	7	C	
E1	PL15A	7	T		E1	PL27A	7	T	
D1	PL15B	7	C		D1	PL27B	7	C	
H3	PL16A	7	T		H3	PL28A	7	T	
G2	PL16B	7	C		G2	PL28B	7	C	
H2	PL17A	7	T		H2	PL29A	7	T	
G1	PL17B	7	C		G1	PL29B	7	C	
J4	PL18A	7	T		J4	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
J3	PL18B	7	C		J3	PL30B	7	C	
J2	PL19A	7	T	LDQS19	J2	PL31A	7	T	LDQS31
H1	PL19B	7	C		H1	PL31B	7	C	
K4	PL20A	7	T		K4	PL32A	7	T	
K5	PL20B	7	C		K5	PL32B	7	C	

**LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)**

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
V2	PL41B	6	C	LLM0_PLLC_IN_A	V2	PL53B	6	C	LLM0_PLLC_IN_A
U3	PL42A	6	T	LLM0_PLLT_FB_A	U3	PL54A	6	T	LLM0_PLLT_FB_A
V3	PL42B	6	C	LLM0_PLLC_FB_A	V3	PL54B	6	C	LLM0_PLLC_FB_A
U4	PL43A	6	T		U4	PL55A	6	T	
V5	PL43B	6	C		V5	PL55B	6	C	
W1	PL44A	6	T		W1	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W2	PL44B	6	C		W2	PL56B	6	C	
Y1	PL45A	6	T	LDQS45	Y1	PL57A	6	T	LDQS57
Y2	PL45B	6	C		Y2	PL57B	6	C	
AA1	PL46A	6	T		AA1	PL58A	6	T	
AA2	PL46B	6	C		AA2	PL58B	6	C	
W4	PL47A	6	T		W4	PL59A	6	T	
V4	PL47B	6	C		V4	PL59B	6	C	
W3	PL48A	6	T	VREF1_6	W3	PL68A	6	T	VREF1_6
Y3	PL48B	6	C	VREF2_6	Y3	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND6	6		
GND	-				GND	GND6	6		
GND	-				GND	GND5	5		
GND	GND5	5			GND	GND5	5		
V7	PB10A	5	T		V7	PB10A	5	T	
T6	PB10B	5	C		T6	PB10B	5	C	
V8	PB11A	5	T		V8	PB11A	5	T	
U7	PB11B	5	C		U7	PB11B	5	C	
W5	PB12A	5	T		W5	PB12A	5	T	
U6	PB12B	5	C		U6	PB12B	5	C	
AA3	PB13A	5	T		AA3	PB13A	5	T	
GND	GND5	5			GND	GND5	5		
AB3	PB13B	5	C		AB3	PB13B	5	C	
Y6	PB14A	5	T	BDQS14	Y6	PB14A	5	T	BDQS14
V6	PB14B	5	C		V6	PB14B	5	C	
AA5	PB15A	5	T		AA5	PB15A	5	T	
W6	PB15B	5	C		W6	PB15B	5	C	
Y5	PB16A	5	T		Y5	PB16A	5	T	
Y4	PB16B	5	C		Y4	PB16B	5	C	
AA4	PB17A	5	T		AA4	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AB4	PB17B	5	C		AB4	PB17B	5	C	
Y7	PB18A	5	T		Y7	PB18A	5	T	
W8	PB18B	5	C		W8	PB18B	5	C	
W7	PB19A	5	T		W7	PB19A	5	T	
U8	PB19B	5	C		U8	PB19B	5	C	
W9	PB20A	5	T		W9	PB20A	5	T	

**LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)**

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	



**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7		
E3	PL2A	7	T	VREF2_7	E3	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
E5	NC	-			E5	PL6A	7	T	LDQS6
D5	NC	-			D5	PL6B	7	C	
F4	NC	-			F4	PL7A	7	T	
F5	NC	-			F5	PL7B	7	C	
C3	NC	-			C3	PL8A	7	T	
D3	NC	-			D3	PL8B	7	C	
C2	NC	-			C2	PL9A	7	T	
-	-	-			GND	GND7	7		
B2	NC	-			B2	PL9B	7	C	
B1	PL3A	7	T		B1	PL10A	7	T	
C1	PL3B	7	C		C1	PL10B	7	C	
F3	PL4A	7	T		F3	PL11A	7	T	
G3	PL4B	7	C		G3	PL11B	7	C	
D2	PL5A	7	T		D2	PL12A	7	T	
E2	PL5B	7	C		E2	PL12B	7	C	
-	-	-			GND	GND7	7		
D1	PL6A	7	T	LDQS6	D1	PL14A	7	T	LDQS14
E1	PL6B	7	C		E1	PL14B	7	C	
F2	PL7A	7	T		F2	PL15A	7	T	
G2	PL7B	7	C		G2	PL15B	7	C	
F6	PL8A	7	T	LUM0_PLLT_IN_A	F6	PL16A	7	T	LUM0_PLLT_IN_A
G6	PL8B	7	C	LUM0_PLLC_IN_A	G6	PL16B	7	C	LUM0_PLLC_IN_A
H4	PL9A	7	T	LUM0_PLLT_FB_A	H4	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
G4	PL9B	7	C	LUM0_PLLC_FB_A	G4	PL17B	7	C	LUM0_PLLC_FB_A
H6	NC	-			H6	PL19A	7	T	
J7	NC	-			J7	PL19B	7	C	
G5	NC	-			G5	PL20A	7	T	
H5	NC	-			H5	PL20B	7	C	
H3	NC	-			H3	PL21A	7	T	
J3	NC	-			J3	PL21B	7	C	
H2	NC	-			H2	PL22A	7	T	
-	-	-			GND	GND7	7		
J2	NC	-			J2	PL22B	7	C	
J4	PL11A	7	T		J4	PL23A	7	T	LDQS23
J5	PL11B	7	C		J5	PL23B	7	C	
K4	PL12A	7	T		K4	PL24A	7	T	
K5	PL12B	7	C		K5	PL24B	7	C	
J6	PL13A	7	T		J6	PL25A	7	T	

**LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AC13	PB32B	5	C	VREF1_5	AC13	PB32B	5	C	VREF1_5
AF14	PB33A	5	T	PCLKT5_0	AF14	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AE14	PB33B	5	C	PCLKC5_0	AE14	PB33B	5	C	PCLKC5_0
AA13	PB34A	4	T	WRITEN	AA13	PB34A	4	T	WRITEN
AB13	PB34B	4	C	CS1N	AB13	PB34B	4	C	CS1N
AD14	PB35A	4	T	VREF1_4	AD14	PB35A	4	T	VREF1_4
AA14	PB35B	4	C	CSN	AA14	PB35B	4	C	CSN
AC14	PB36A	4	T	VREF2_4	AC14	PB36A	4	T	VREF2_4
AB14	PB36B	4	C	D0/SPID7	AB14	PB36B	4	C	D0/SPID7
AF15	PB37A	4	T	D2/SPID5	AF15	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AE15	PB37B	4	C	D1/SPID6	AE15	PB37B	4	C	D1/SPID6
AD15	PB38A	4	T	BDQS38	AD15	PB38A	4	T	BDQS38
AC15	PB38B	4	C	D3/SPID4	AC15	PB38B	4	C	D3/SPID4
AF16	PB39A	4	T		AF16	PB39A	4	T	
Y14	PB39B	4	C	D4/SPID3	Y14	PB39B	4	C	D4/SPID3
AE16	PB40A	4	T		AE16	PB40A	4	T	
AB15	PB40B	4	C	D5/SPID2	AB15	PB40B	4	C	D5/SPID2
AF17	PB41A	4	T		AF17	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AE17	PB41B	4	C	D6/SPID1	AE17	PB41B	4	C	D6/SPID1
Y15	PB42A	4	T		Y15	PB42A	4	T	
AA15	PB42B	4	C		AA15	PB42B	4	C	
AD17	PB43A	4	T		AD17	PB43A	4	T	
Y16	PB43B	4	C		Y16	PB43B	4	C	
AD18	PB44A	4	T		AD18	PB44A	4	T	
AC16	PB44B	4	C		AC16	PB44B	4	C	
AE18	PB45A	4	T		AE18	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AF18	PB45B	4	C		AF18	PB45B	4	C	
AD16	PB46A	4	T	BDQS46	AD16	PB46A	4	T	BDQS46
AB16	PB46B	4	C		AB16	PB46B	4	C	
AF19	PB47A	4	T		AF19	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AA17	PB48A	4	T		AA17	PB48A	4	T	
Y17	PB48B	4	C		Y17	PB48B	4	C	
AF21	PB49A	4	T		AF21	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AF20	PB49B	4	C		AF20	PB49B	4	C	
AE21	PB50A	4	T		AE21	PB50A	4	T	
AC17	PB50B	4	C		AC17	PB50B	4	C	

**LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

**LatticeEC Industrial (Continued)**

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672I	400	-3	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-4FN672I	400	-4	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-3FN484I	400	-3	Lead-Free fpBGA	484	IND	19.7K
LFEC20E-4FN484I	400	-4	Lead-Free fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672I	496	-3	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-4FN672I	496	-4	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-3FN484I	360	-3	Lead-Free fpBGA	484	IND	32.8K
LFEC33E-4FN484I	360	-4	Lead-Free fpBGA	484	IND	32.8K

**LatticeECP Industrial**

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K

## For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at [www.latticesemi.com](http://www.latticesemi.com).

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): [www.jedec.org](http://www.jedec.org)
- PCI: [www.pcisig.com](http://www.pcisig.com)