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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	112
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-3qn208i

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (EConomy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (EConomy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (EConomy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

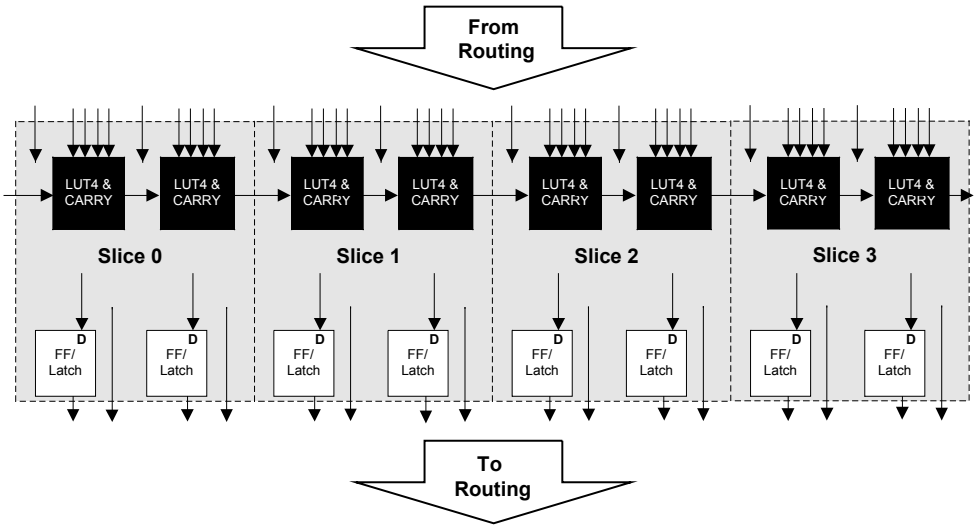
Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, the routing of both short and long connections between PFUs.

The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

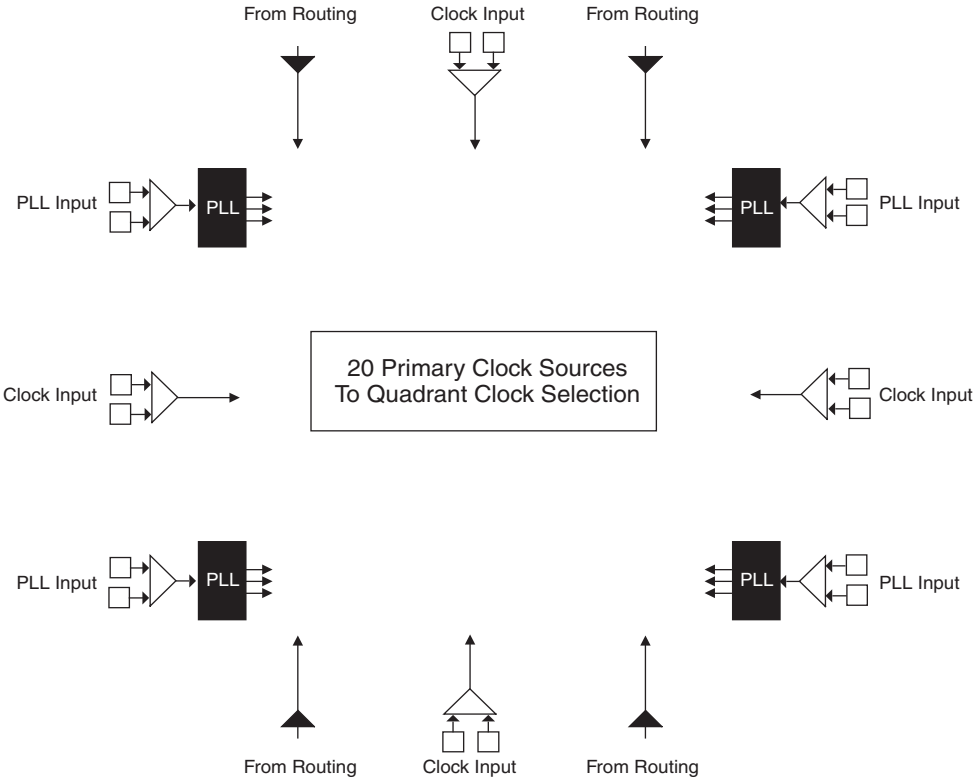
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Primary Clock Sources



Note: Smaller devices have two PLLs.

grammed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-11. PLL Diagram

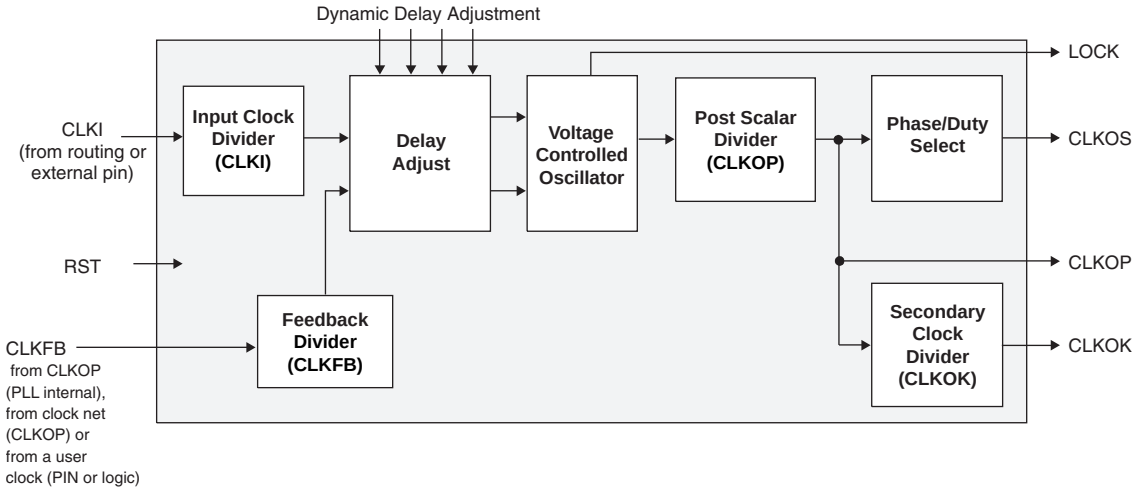
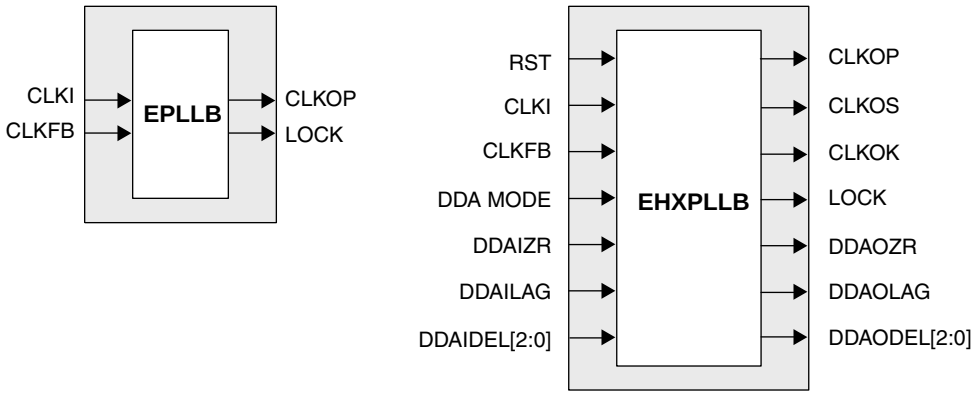


Figure 2-12 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

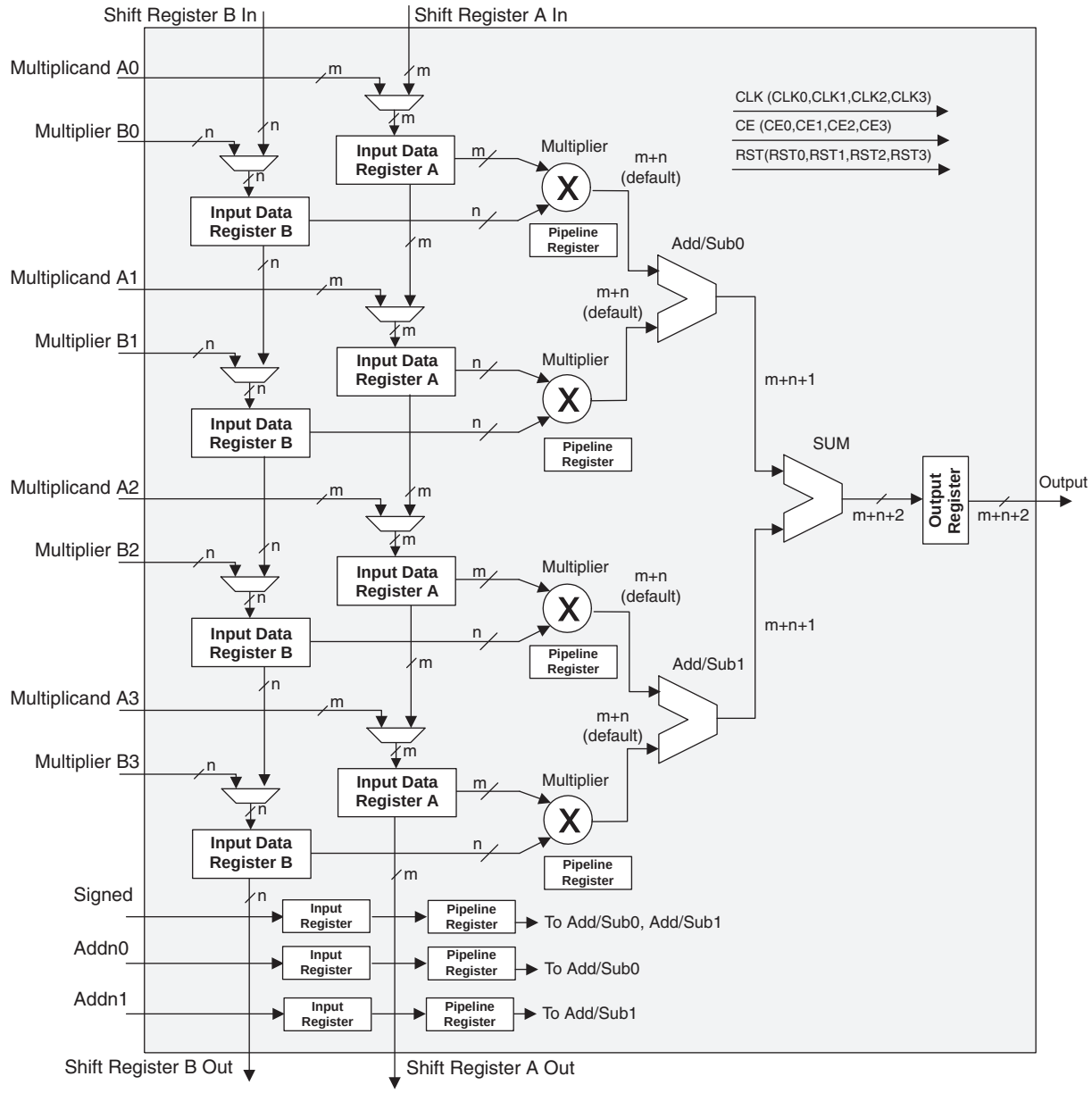
Figure 2-12. PLL Primitive



MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUM sysDSP element.

Figure 2-22. MULTADDSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Figure 2-32. DQS Local Bus.

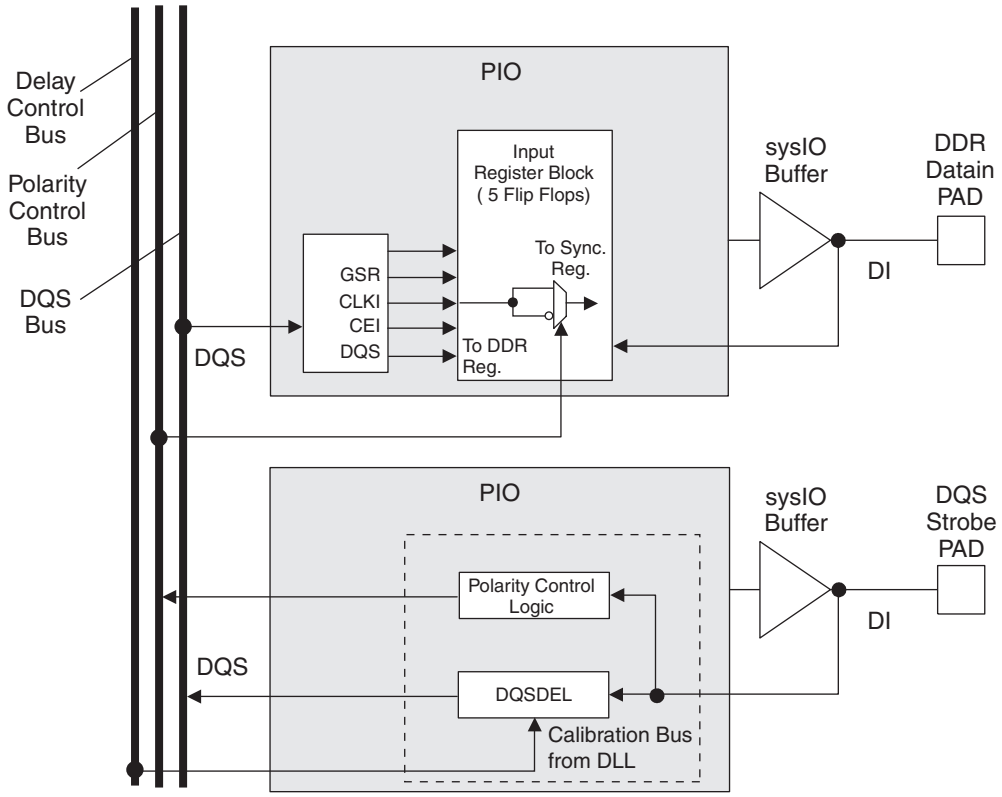
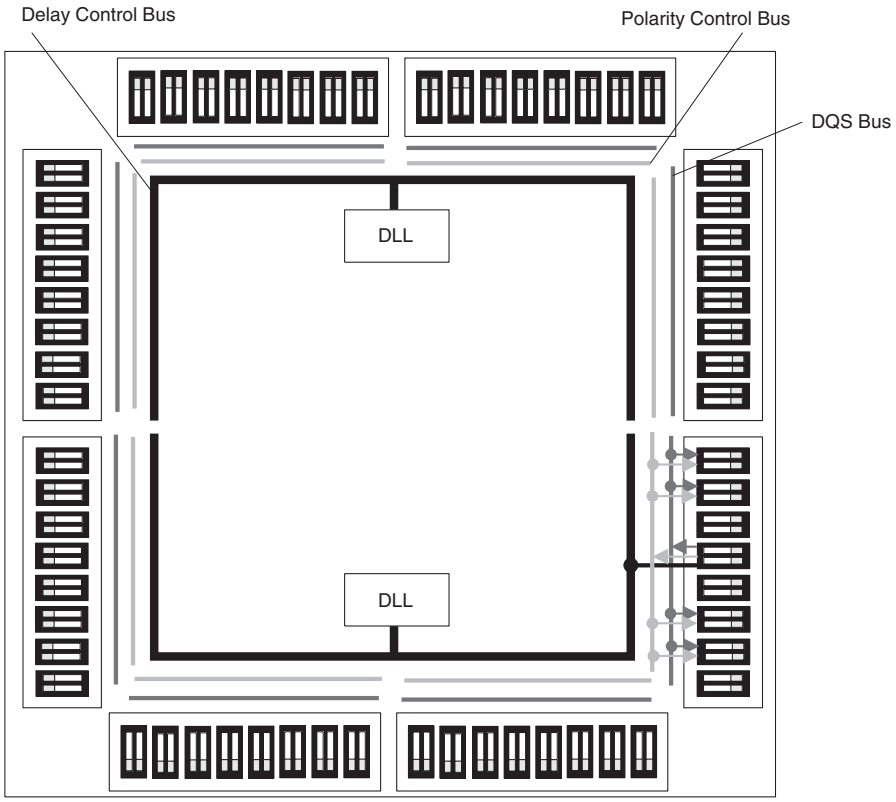


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution



DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCIO} - 0.2V)	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	(V_{CCIO} - 0.2V) ð V_{IH} ð 3.6V	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCIO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO}.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

LatticeECP/EC Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.25	—	0.31	—	0.36	ns
t_{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.40	—	0.48	—	0.56	ns
t_{LSR_PFU}	Set/Reset to Output of PFU	—	0.81	—	0.98	—	1.14	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.05	—	-0.06	—	-0.06	—	ns
t_{SUD_PFU}	Clock to D Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t_{HD_PFU}	Clock to D Input Hold time	-0.03	—	-0.03	—	-0.04	—	ns
t_{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.36	—	0.44	—	0.51	ns
t_{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.48	—	0.58	—	0.68	ns
t_{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.50	—	0.60	—	0.69	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.36	—	0.44	—	0.51	ns
t_{SUDATA_PFU}	Data Setup Time	-0.20	—	-0.24	—	-0.28	—	ns
t_{HDATA_PFU}	Data Hold Time	0.26	—	0.31	—	0.36	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.51	—	-0.62	—	-0.72	—	ns
t_{HADDR_PFU}	Address Hold Time	0.64	—	0.77	—	0.90	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.24	—	-0.29	—	-0.34	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.30	—	0.36	—	0.42	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—	0.56	—	0.67	—	0.78	ns
t_{OUT_PIO}	Output Buffer Delay	—	1.92	—	2.31	—	2.69	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.90	—	1.08	—	1.26	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	0.62	—	0.74	—	0.87	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.33	—	0.40	—	0.46	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.10	—	-0.12	—	-0.14	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	0.12	—	0.14	—	0.17	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.18	—	0.21	—	0.25	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.15	—	-0.18	—	-0.21	—	ns
EBR Timing								
t_{CO_EBR}	Clock to Output from Address or Data	—	3.64	—	4.37	—	5.10	ns
t_{COO_EBR}	Clock to Output from EBR output Register	—	0.74	—	0.88	—	1.03	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.18	—	-0.22	—	-0.26	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.23	—	0.28	—	0.33	—	ns

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from tICFG to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			NC	-		
6	NC	-			NC	-		
7	NC	-			PL3B	7		
8	NC	-			PL4A	7	T	
9	NC	-			PL4B	7	C	
10	NC	-			PL5A	7	T	
11	NC	-			PL5B	7	C	
12	NC	-			PL6A	7	T	LDQS6
13	NC	-			VCCIO7	7		
14	NC	-			PL6B	7	C	
15	PL3A	7	T		PL7A	7	T	
16	PL3B	7	C		PL7B	7	C	
17	PL4A	7	T		PL8A	7	T	
18	NC	-			NC	-		
19	PL4B	7	C		PL8B	7	C	
20	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
21	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
22	NC	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	NC	-			NC	-		
25	NC	-			NC	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LLM0_PLLT_IN_A
34	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LLM0_PLLC_IN_A
35	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LLM0_PLLT_FB_A
36	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL9A	6	T		PL13A	6	T	
39	PL9B	6	C		PL13B	6	C	
40	PL10A	6	T		PL14A	6	T	
41	GND6	6			GND6	6		
42	PL10B	6	C		PL14B	6	C	

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A4	NC	-			A4	PT9B	0	C		A4	PT9B	0	C	
B4	NC	-			B4	PT9A	0	T		B4	PT9A	0	T	
C4	NC	-			C4	PT8B	0	C		C4	PT8B	0	C	
C5	NC	-			C5	PT8A	0	T		C5	PT8A	0	T	
D6	NC	-			D6	PT7B	0	C		D6	PT7B	0	C	
B5	NC	-			B5	PT7A	0	T		B5	PT7A	0	T	
E6	NC	-			E6	PT6B	0	C		E6	PT6B	0	C	
C6	NC	-			C6	PT6A	0	T	TDQS6	C6	PT6A	0	T	TDQS6
A3	NC	-			A3	PT5B	0	C		A3	PT5B	0	C	
B3	NC	-			B3	PT5A	0	T		B3	PT5A	0	T	
F6	NC	-			F6	PT4B	0	C		F6	PT4B	0	C	
D5	NC	-			D5	PT4A	0	T		D5	PT4A	0	T	
F7	NC	-			F7	PT3B	0	C		F7	PT3B	0	C	
E8	NC	-			E8	PT3A	0	T		E8	PT3A	0	T	
G6	NC	-			G6	PT2B	0	C		G6	PT2B	0	C	
E7	NC	-			E7	PT2A	0	T		E7	PT2A	0	T	
GND	-	-			GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-			A22	GND	-		
AB1	GND	-			AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-			N12	GND	-		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
T11	VCCIO5	5			T11	VCCIO5	5			T11	VCCIO5	5		
M7	VCCIO6	6			M7	VCCIO6	6			M7	VCCIO6	6		
M8	VCCIO6	6			M8	VCCIO6	6			M8	VCCIO6	6		
N8	VCCIO6	6			N8	VCCIO6	6			N8	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6			P8	VCCIO6	6		
J8	VCCIO7	7			J8	VCCIO7	7			J8	VCCIO7	7		
K8	VCCIO7	7			K8	VCCIO7	7			K8	VCCIO7	7		
L7	VCCIO7	7			L7	VCCIO7	7			L7	VCCIO7	7		
L8	VCCIO7	7			L8	VCCIO7	7			L8	VCCIO7	7		
G15	VCCAUX	-			G15	VCCAUX	-			G15	VCCAUX	-		
G16	VCCAUX	-			G16	VCCAUX	-			G16	VCCAUX	-		
G7	VCCAUX	-			G7	VCCAUX	-			G7	VCCAUX	-		
G8	VCCAUX	-			G8	VCCAUX	-			G8	VCCAUX	-		
H16	VCCAUX	-			H16	VCCAUX	-			H16	VCCAUX	-		
H7	VCCAUX	-			H7	VCCAUX	-			H7	VCCAUX	-		
R16	VCCAUX	-			R16	VCCAUX	-			R16	VCCAUX	-		
R7	VCCAUX	-			R7	VCCAUX	-			R7	VCCAUX	-		
T15	VCCAUX	-			T15	VCCAUX	-			T15	VCCAUX	-		
T16	VCCAUX	-			T16	VCCAUX	-			T16	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-			T8	VCCAUX	-		
J6	VCC	-			J6	VCC	-			J6	VCC	-		
J17	VCC	-			J17	VCC	-			J17	VCC	-		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
P17	VCC	-			P17	VCC	-			P17	VCC	-		
A2	NC	-			A2	NC	-			A2	NC	-		
AB2	NC	-			AB2	NC	-			AB2	NC	-		
A21	NC	-			A21	NC	-			A21	NC	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF22	PB51A	4	T		AF22	PB51A	4	T	
AB17	PB51B	4	C		AB17	PB51B	4	C	
AE22	PB52A	4	T		AE22	PB52A	4	T	
AA18	PB52B	4	C		AA18	PB52B	4	C	
AE19	PB53A	4	T		AE19	PB53A	4	T	
GND	GND4	4			GND	GND4	4		
AE20	PB53B	4	C		AE20	PB53B	4	C	
AA19	PB54A	4	T	BDQS54	AA19	PB54A	4	T	BDQS54
Y18	PB54B	4	C		Y18	PB54B	4	C	
AF23	PB55A	4	T		AF23	PB55A	4	T	
AA20	PB55B	4	C		AA20	PB55B	4	C	
AC18	PB56A	4	T		AC18	PB56A	4	T	
AB18	PB56B	4	C		AB18	PB56B	4	C	
AF24	PB57A	4	T		AF24	PB57A	4	T	
-	-	-			GND	GND4	4		
AE23	PB57B	4	C		AE23	PB57B	4	C	
AD19	NC	-			AD19	PB58A	4	T	
AD20	NC	-			AD20	PB58B	4	C	
AC19	NC	-			AC19	PB59A	4	T	
AB19	NC	-			AB19	PB59B	4	C	
AD21	NC	-			AD21	PB60A	4	T	
AC20	NC	-			AC20	PB60B	4	C	
AF25	NC	-			AF25	PB61A	4	T	
-	-	-			GND	GND4	4		
AE25	NC	-			AE25	PB61B	4	C	
AB21	NC	-			AB21	PB62A	4	T	BDQS62
AB20	NC	-			AB20	PB62B	4	C	
AE24	NC	-			AE24	PB63A	4	T	
AD23	NC	-			AD23	PB63B	4	C	
AD22	NC	-			AD22	PB64A	4	T	
AC21	NC	-			AC21	PB64B	4	C	
AC22	NC	-			AC22	PB65A	4	T	
AB22	NC	-			AB22	PB65B	4	C	
GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3		
AC23	PR48B	3	C	VREF2_3	AC23	PR68B	3	C	VREF2_3
AC24	PR48A	3	T	VREF1_3	AC24	PR68A	3	T	VREF1_3
AD24	NC	-			AD24	PR67B	3	C	
AD25	NC	-			AD25	PR67A	3	T	
AE26	NC	-			AE26	PR66B	3	C	
AD26	NC	-			AD26	PR66A	3	T	
Y20	NC	-			Y20	PR65B	3	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
H7	VCCAUX	-			H7	VCCAUX	-		
J19	VCCAUX	-			J19	VCCAUX	-		
J8	VCCAUX	-			J8	VCCAUX	-		
K7	VCCAUX	-			K7	VCCAUX	-		
L20	VCCAUX	-			L20	VCCAUX	-		
M20	VCCAUX	-			M20	VCCAUX	-		
M7	VCCAUX	-			M7	VCCAUX	-		
N20	VCCAUX	-			N20	VCCAUX	-		
P20	VCCAUX	-			P20	VCCAUX	-		
P7	VCCAUX	-			P7	VCCAUX	-		
T20	VCCAUX	-			T20	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
V19	VCCAUX	-			V19	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
W20	VCCAUX	-			W20	VCCAUX	-		
Y13	VCCAUX	-			Y13	VCCAUX	-		
Y7	VCCAUX	-			Y7	VCCAUX	-		
K19	VCC[1]	-			K19	VCCPLL	-		
L8	VCC[1]	-			L8	VCCPLL	-		
U19	VCC[1]	-			U19	VCCPLL	-		
U8	VCC[1]	-			U8	VCCPLL	-		

1. Tied to V_{CCPLL}.

LatticeECP/EC Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com