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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	67
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-3tn100i

Architecture Overview

The LatticeECP-DSP and LatticeEC architectures contain an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR), as shown in Figures 2-1 and 2-2. In addition, LatticeECP-DSP supports an additional row of DSP blocks, as shown in Figure 2-2.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

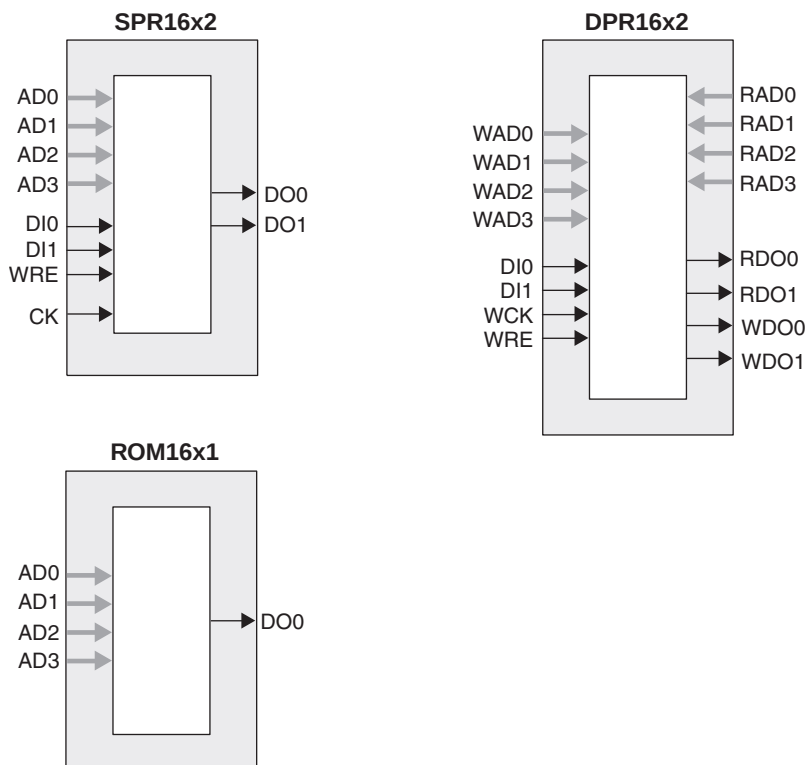
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeECP/EC architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The LatticeECP/EC devices use 1.2V as their core voltage.

Figure 2-5. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM ¹	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Figure 2-8. Per Quadrant Primary Clock Selection

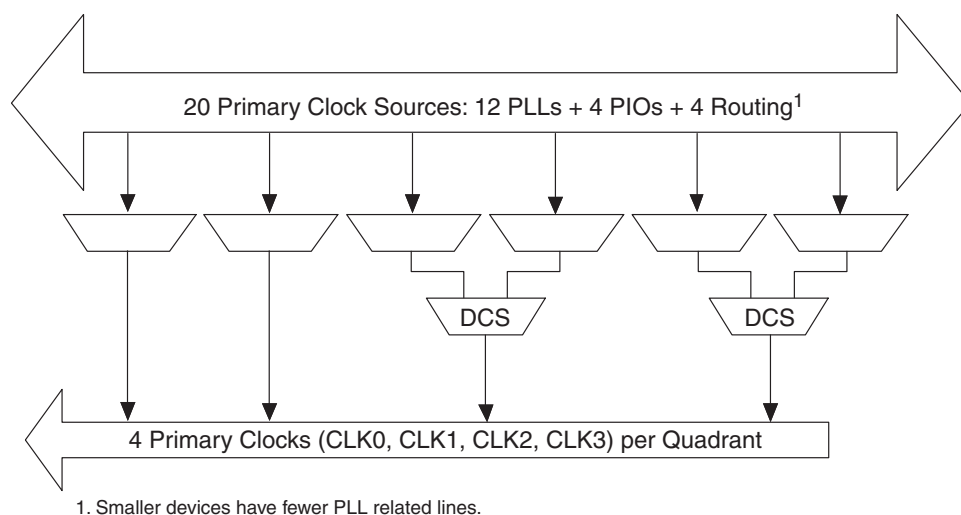


Figure 2-9. Per Quadrant Secondary Clock Selection

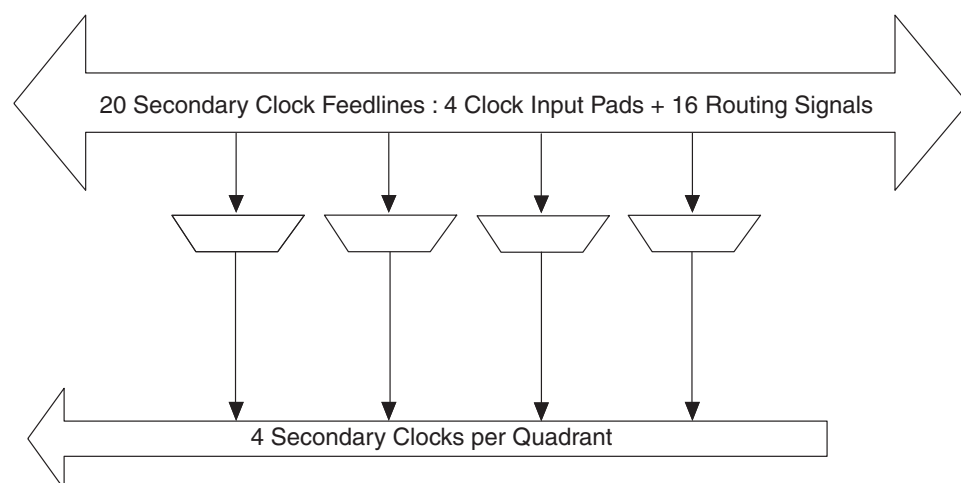
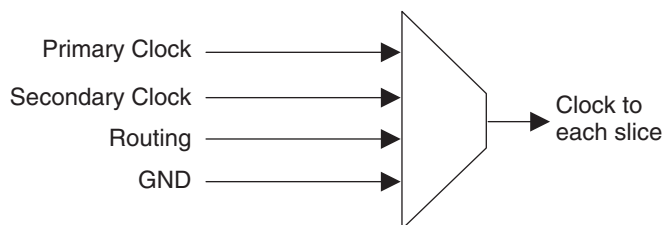


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Table 2-14. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3
RSDS ¹	N/A	2.5

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

LatticeECP/EC Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.25	—	0.31	—	0.36	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.40	—	0.48	—	0.56	ns
t _{LSR_PFU}	Set/Reset to Output of PFU	—	0.81	—	0.98	—	1.14	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.05	—	-0.06	—	-0.06	—	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HD_PFU}	Clock to D Input Hold time	-0.03	—	-0.03	—	-0.04	—	ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.36	—	0.44	—	0.51	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.48	—	0.58	—	0.68	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.50	—	0.60	—	0.69	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output	—	0.36	—	0.44	—	0.51	ns
t _{SUDATA_PFU}	Data Setup Time	-0.20	—	-0.24	—	-0.28	—	ns
t _{HDATA_PFU}	Data Hold Time	0.26	—	0.31	—	0.36	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.51	—	-0.62	—	-0.72	—	ns
t _{HADDR_PFU}	Address Hold Time	0.64	—	0.77	—	0.90	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.24	—	-0.29	—	-0.34	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.30	—	0.36	—	0.42	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay	—	0.56	—	0.67	—	0.78	ns
t _{OUT_PIO}	Output Buffer Delay	—	1.92	—	2.31	—	2.69	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.90	—	1.08	—	1.26	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.62	—	0.74	—	0.87	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.33	—	0.40	—	0.46	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.10	—	-0.12	—	-0.14	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.12	—	0.14	—	0.17	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.18	—	0.21	—	0.25	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.15	—	-0.18	—	-0.21	—	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data	—	3.64	—	4.37	—	5.10	ns
t _{COO_EBR}	Clock to Output from EBR output Register	—	0.74	—	0.88	—	1.03	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.18	—	-0.22	—	-0.26	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.23	—	0.28	—	0.33	—	ns

LatticeECP/EC Family Timing Adders^{1, 2, 3}

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25	LVDS	0.41	0.50	0.58	ns
BLVDS25	BLVDS	0.41	0.50	0.58	ns
LVPECL33	LVPECL	0.50	0.60	0.70	ns
HSTL18_I	HSTL_18 class I	0.41	0.49	0.57	ns
HSTL18_II	HSTL_18 class II	0.41	0.49	0.57	ns
HSTL18_III	HSTL_18 class III	0.41	0.49	0.57	ns
HSTL18D_I	Differential HSTL 18 class I	0.37	0.44	0.52	ns
HSTL18D_II	Differential HSTL 18 class II	0.37	0.44	0.52	ns
HSTL18D_III	Differential HSTL 18 class III	0.37	0.44	0.52	ns
HSTL15_I	HSTL_15 class I	0.40	0.48	0.56	ns
HSTL15_III	HSTL_15 class III	0.40	0.48	0.56	ns
HSTL15D_I	Differential HSTL 15 class I	0.37	0.44	0.51	ns
HSTL15D_III	Differential HSTL 15 class III	0.37	0.44	0.51	ns
SSTL33_I	SSTL_3 class I	0.46	0.55	0.64	ns
SSTL33_II	SSTL_3 class II	0.46	0.55	0.64	ns
SSTL33D_I	Differential SSTL_3 class I	0.39	0.47	0.55	ns
SSTL33D_II	Differential SSTL_3 class II	0.39	0.47	0.55	ns
SSTL25_I	SSTL_2 class I	0.43	0.51	0.60	ns
SSTL25_II	SSTL_2 class II	0.43	0.51	0.60	ns
SSTL25D_I	Differential SSTL_2 class I	0.38	0.45	0.53	ns
SSTL25D_II	Differential SSTL_2 class II	0.38	0.45	0.53	ns
SSTL18_I	SSTL_18 class I	0.40	0.48	0.56	ns
SSTL18D_I	Differential SSTL_18 class I	0.37	0.44	0.51	ns
LVTTL33	LVTTL	0.07	0.09	0.10	ns
LVC MOS33	LVC MOS 3.3	0.07	0.09	0.10	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	0.07	0.09	0.10	ns
LVC MOS15	LVC MOS 1.5	0.24	0.29	0.33	ns
LVC MOS12	LVC MOS 1.2	1.27	1.52	1.77	ns
PCI33	PCI	0.07	0.09	0.10	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	0.12	0.14	0.17	ns
LVDS25	LVDS 2.5	-0.44	-0.53	-0.62	ns
BLVDS25	BLVDS 2.5	0.33	0.40	0.46	ns
LVPECL33	LVPECL 3.3	0.20	0.24	0.28	ns
HSTL18_I	HSTL_18 class I	-0.10	-0.12	-0.14	ns
HSTL18_II	HSTL_18 class II	0.06	0.07	0.08	ns
HSTL18_III	HSTL_18 class III	0.15	0.19	0.22	ns
HSTL18D_I	Differential HSTL 18 class I	-0.10	-0.12	-0.14	ns
HSTL18D_II	Differential HSTL 18 class II	0.06	0.07	0.08	ns
HSTL18D_III	Differential HSTL 18 class III	0.15	0.19	0.22	ns
HSTL15_I	HSTL_15 class I	0.08	0.10	0.11	ns

LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30



LatticeECP/EC Family Data Sheet

Pinout Information

September 2012

Data Sheet

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins.
V _{CCIOx}	—	Power supply pins for I/O bank x. Dedicated pins.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES	—	10K ohm +/-1% resistor must be connected between this pad and ground.
V _{CCPLL}	—	Power supply pin for PLL. Applicable to ECP/EC33 device.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	I	Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_PLL[T, C]_FB_A	I	Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.

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LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
K2	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
K1	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
L2	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
L1	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
M2	PL13A	6	T		PL22A	6	T	
M1	PL13B	6	C		PL22B	6	C	
N1	PL14A	6	T		PL23A	6	T	
GND	GND6	6			GND6	6		
N2	PL14B	6	C		PL23B	6	C	
M4	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
M3	PL15B	6	C		PL24B	6	C	
P1	PL16A	6	T		PL25A	6	T	
R1	PL16B	6	C		PL25B	6	C	
P2	PL17A	6	T		PL26A	6	T	
P3	PL17B	6	C		PL26B	6	C	
N3	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
N4	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
P4	PB2A	5	T		PB2A	5	T	
N5	PB2B	5	C		PB2B	5	C	
P5	PB3A	5	T		PB3A	5	T	
P6	PB3B	5	C		PB3B	5	C	
R4	PB4A	5	T		PB4A	5	T	
R3	PB4B	5	C		PB4B	5	C	
T2	PB5A	5	T		PB5A	5	T	
T3	PB5B	5	C		PB5B	5	C	
R5	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
R6	PB6B	5	C		PB6B	5	C	
T4	PB7A	5	T		PB7A	5	T	
T5	PB7B	5	C		PB7B	5	C	
N6	PB8A	5	T		PB8A	5	T	
M6	PB8B	5	C		PB8B	5	C	
T6	PB9A	5	T		PB9A	5	T	
GND	GND5	5			GND5	5		
T7	PB9B	5	C		PB9B	5	C	
P7	PB10A	5	T		PB10A	5	T	
N7	PB10B	5	C		PB10B	5	C	
R7	PB11A	5	T		PB11A	5	T	
R8	PB11B	5	C		PB11B	5	C	
M7	PB12A	5	T		PB12A	5	T	
M8	PB12B	5	C		PB12B	5	C	
T8	PB13A	5	T		PB13A	5	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N16	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
N15	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
M15	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
M16	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
L16	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
K16	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
J16	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
	-	-			GND3	3		
H16	NC	-			PR18B	3	C	
H15	NC	-			PR18A	3	T	
G16	NC	-			PR17B	3	C	
G15	NC	-			PR17A	3	T	
K12	NC	-			PR16B	3	C	
J12	NC	-			PR16A	3	T	
J14	NC	-			PR15B	3	C	
J15	NC	-			PR15A	3	T	RDQS15
F16	NC	-			PR14B	3	C	
-	-	-			GND3	3		
F15	NC	-			PR14A	3	T	
J13	NC	-			PR13B	3	C	
H13	NC	-			PR13A	3	T	
H14	NC	-			PR12B	3	C	
G14	NC	-			PR12A	3	T	
E16	NC	-			PR11B	3	C	
E15	NC	-			PR11A	3	T	
H12	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
GND	GND2	2			GND2			
G12	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
G13	PR8B	2	C		PR8B	2	C	
F13	PR8A	2	T		PR8A	2	T	
F12	PR7B	2	C		PR7B	2	C	
E13	PR7A	2	T		PR7A	2	T	
D16	PR6B	2	C		PR6B	2	C	
D15	PR6A	2	T	RDQS6	PR6A	2	T	RDQS6
F14	PR5B	2	C		PR5B	2	C	
E14	PR5A	2	T		PR5A	2	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFEC/EC10 and LFEC/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFEC/EC10				LFEC/EC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND	GND5	5			GND	GND5	5		
V7	NC	-			V7	PB2A	5	T		V7	PB2A	5	T	
T6	NC	-			T6	PB2B	5	C		T6	PB2B	5	C	
V8	NC	-			V8	PB3A	5	T		V8	PB3A	5	T	
U7	NC	-			U7	PB3B	5	C		U7	PB3B	5	C	
W5	NC	-			W5	PB4A	5	T		W5	PB4A	5	T	
U6	NC	-			U6	PB4B	5	C		U6	PB4B	5	C	
AA3	NC	-			AA3	PB5A	5	T		AA3	PB5A	5	T	
AB3	NC	-			AB3	PB5B	5	C		AB3	PB5B	5	C	
Y6	NC	-			Y6	PB6A	5	T	BDQS6	Y6	PB6A	5	T	BDQS6
V6	NC	-			V6	PB6B	5	C		V6	PB6B	5	C	
AA5	NC	-			AA5	PB7A	5	T		AA5	PB7A	5	T	
W6	NC	-			W6	PB7B	5	C		W6	PB7B	5	C	
Y5	NC	-			Y5	PB8A	5	T		Y5	PB8A	5	T	
Y4	NC	-			Y4	PB8B	5	C		Y4	PB8B	5	C	
AA4	NC	-			AA4	PB9A	5	T		AA4	PB9A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
AB4	NC	-			AB4	PB9B	5	C		AB4	PB9B	5	C	
Y7	PB2A	5	T		Y7	PB10A	5	T		Y7	PB10A	5	T	
W8	PB2B	5	C		W8	PB10B	5	C		W8	PB10B	5	C	
W7	PB3A	5	T		W7	PB11A	5	T		W7	PB11A	5	T	
U8	PB3B	5	C		U8	PB11B	5	C		U8	PB11B	5	C	
W9	PB4A	5	T		W9	PB12A	5	T		W9	PB12A	5	T	
U9	PB4B	5	C		U9	PB12B	5	C		U9	PB12B	5	C	
Y8	PB5A	5	T		Y8	PB13A	5	T		Y8	PB13A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
Y9	PB5B	5	C		Y9	PB13B	5	C		Y9	PB13B	5	C	
V9	PB6A	5	T	BDQS6	V9	PB14A	5	T	BDQS14	V9	PB14A	5	T	BDQS14
T9	PB6B	5	C		T9	PB14B	5	C		T9	PB14B	5	C	
W10	PB7A	5	T		W10	PB15A	5	T		W10	PB15A	5	T	
U10	PB7B	5	C		U10	PB15B	5	C		U10	PB15B	5	C	
V10	PB8A	5	T		V10	PB16A	5	T		V10	PB16A	5	T	
T10	PB8B	5	C		T10	PB16B	5	C		T10	PB16B	5	C	
AA6	PB9A	5	T		AA6	PB17A	5	T		AA6	PB17A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB5	PB9B	5	C		AB5	PB17B	5	C		AB5	PB17B	5	C	
AA8	PB10A	5	T		AA8	PB18A	5	T		AA8	PB18A	5	T	
AA7	PB10B	5	C		AA7	PB18B	5	C		AA7	PB18B	5	C	
AB6	PB11A	5	T		AB6	PB19A	5	T		AB6	PB19A	5	T	
AB7	PB11B	5	C		AB7	PB19B	5	C		AB7	PB19B	5	C	
Y10	PB12A	5	T		Y10	PB20A	5	T		Y10	PB20A	5	T	
W11	PB12B	5	C		W11	PB20B	5	C		W11	PB20B	5	C	
AB8	PB13A	5	T		AB8	PB21A	5	T		AB8	PB21A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB9	PB13B	5	C		AB9	PB21B	5	C		AB9	PB21B	5	C	
AA10	PB14A	5	T	BDQS14	AA10	PB22A	5	T	BDQS22	AA10	PB22A	5	T	BDQS22
AA9	PB14B	5	C		AA9	PB22B	5	C		AA9	PB22B	5	C	
Y11	PB15A	5	T		Y11	PB23A	5	T		Y11	PB23A	5	T	
AA11	PB15B	5	C		AA11	PB23B	5	C		AA11	PB23B	5	C	
V11	PB16A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
L7	VCCIO7	7			L7	VCCIO7	7		
L8	VCCIO7	7			L8	VCCIO7	7		
G15	VCCAUX	-			G15	VCCAUX	-		
G16	VCCAUX	-			G16	VCCAUX	-		
G7	VCCAUX	-			G7	VCCAUX	-		
G8	VCCAUX	-			G8	VCCAUX	-		
H16	VCCAUX	-			H16	VCCAUX	-		
H7	VCCAUX	-			H7	VCCAUX	-		
R16	VCCAUX	-			R16	VCCAUX	-		
R7	VCCAUX	-			R7	VCCAUX	-		
T15	VCCAUX	-			T15	VCCAUX	-		
T16	VCCAUX	-			T16	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
J6	VCC ¹	-			J6	VCCPLL	-		
J17	VCC ¹	-			J17	VCCPLL	-		
P6	VCC ¹	-			P6	VCCPLL	-		
P17	VCC ¹	-			P17	VCCPLL	-		
A2	NC	-			A2	NC	-		
AB2	NC	-			AB2	NC	-		
A21	NC	-			A21	NC	-		

 1. Tied to V_{CCPLL}.

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M15	GND	-			M15	GND	-		
M16	GND	-			M16	GND	-		
M17	GND	-			M17	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N16	GND	-			N16	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P16	GND	-			P16	GND	-		
P17	GND	-			P17	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
R15	GND	-			R15	GND	-		
R16	GND	-			R16	GND	-		
R17	GND	-			R17	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T12	GND	-			T12	GND	-		
T13	GND	-			T13	GND	-		
T14	GND	-			T14	GND	-		
T15	GND	-			T15	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
J14	VCCIO1	1			J14	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
J16	VCCIO1	1			J16	VCCIO1	1		
J17	VCCIO1	1			J17	VCCIO1	1		
K17	VCCIO2	2			K17	VCCIO2	2		
K18	VCCIO2	2			K18	VCCIO2	2		
L18	VCCIO2	2			L18	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
N18	VCCIO2	2			N18	VCCIO2	2		
N19	VCCIO2	2			N19	VCCIO2	2		
P18	VCCIO3	3			P18	VCCIO3	3		
P19	VCCIO3	3			P19	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
R19	VCCIO3	3			R19	VCCIO3	3		
T18	VCCIO3	3			T18	VCCIO3	3		
U18	VCCIO3	3			U18	VCCIO3	3		
V14	VCCIO4	4			V14	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
V16	VCCIO4	4			V16	VCCIO4	4		
V17	VCCIO4	4			V17	VCCIO4	4		
W14	VCCIO4	4			W14	VCCIO4	4		
W15	VCCIO4	4			W15	VCCIO4	4		
V10	VCCIO5	5			V10	VCCIO5	5		
V11	VCCIO5	5			V11	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
V13	VCCIO5	5			V13	VCCIO5	5		
W12	VCCIO5	5			W12	VCCIO5	5		
W13	VCCIO5	5			W13	VCCIO5	5		
P8	VCCIO6	6			P8	VCCIO6	6		
P9	VCCIO6	6			P9	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T9	VCCIO6	6			T9	VCCIO6	6		
U9	VCCIO6	6			U9	VCCIO6	6		
K9	VCCIO7	7			K9	VCCIO7	7		
L9	VCCIO7	7			L9	VCCIO7	7		
M8	VCCIO7	7			M8	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
N8	VCCIO7	7			N8	VCCIO7	7		
N9	VCCIO7	7			N9	VCCIO7	7		
G13	VCCAUX	-			G13	VCCAUX	-		
H20	VCCAUX	-			H20	VCCAUX	-		

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software