Lattice Semiconductor Corporation - LFEC1E-3TN144I Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	97
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-3tn144i

LatticeECP/EC Family Data Sheet Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR16x2	ROM16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information about using RAM in LatticeECP/EC devices, please see the list of technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of slices	1	2

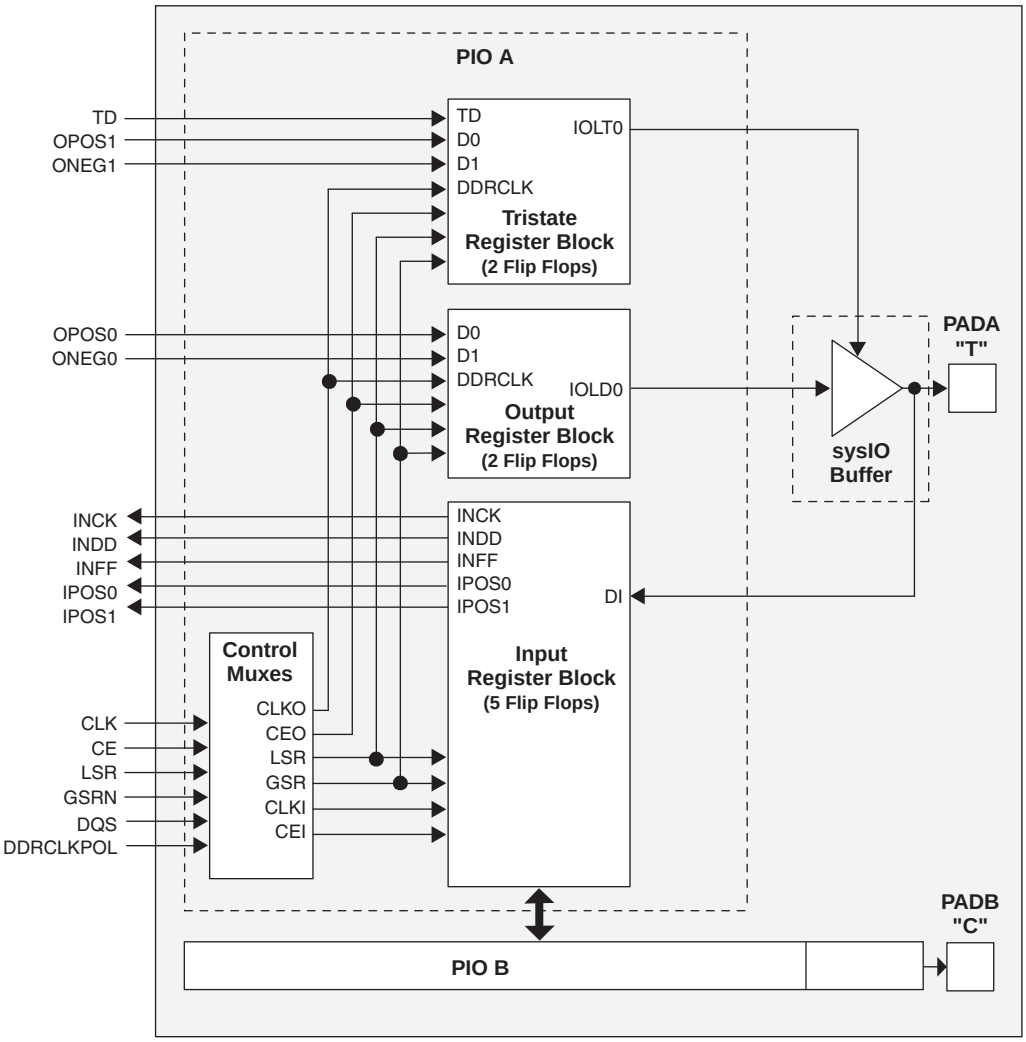
Note: SPR = Single Port RAM, DPR = Dual Port RAM

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP/EC devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeECP/EC sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL, BLVDS, RSDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

sysI/O Single-Ended DC Electrical Characteristics

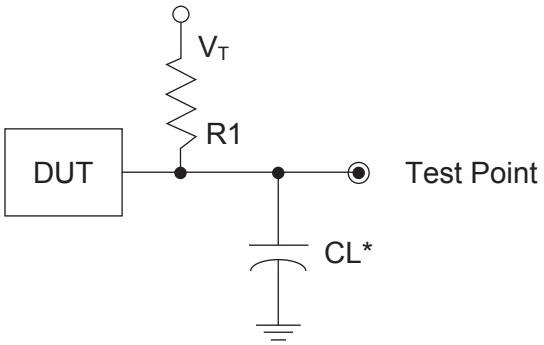
Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Switching Test Conditions

Figure 3-21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-21. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188¾	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LFEC1, LFEC3, LFECP/EC6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFEC1				LFEC3				LFECP6/EC6			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
99	VCC	-			VCC	-			VCC	-		
100	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
101	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
102	PR4B	2	C		PR8B	2	C		PR8B	2	C	
103	PR4A	2	T		PR8A	2	T		PR8A	2	T	
104	PR3B	2	C		PR7B	2	C		PR7B	2	C	
105	PR3A	2	T		PR7A	2	T		PR7A	2	T	
106	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
107	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
108	VCCIO2	2			VCCIO2	2			VCCIO2	2		
109*	GND1 GND2	-			GND1 GND2	-			GND1 GND2	-		
110	VCCIO1	1			VCCIO1	1			VCCIO1	1		
111	PT17B	1	C		PT25B	1	C		PT25B	1	C	
112	PT17A	1	T		PT25A	1	T		PT25A	1	T	
113	PT15A	1			PT23A	1			PT23A	1		
114	PT14B	1	C		PT22B	1	C		PT22B	1	C	
115	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
116	PT13B	1	C		PT21B	1	C		PT21B	1	C	
117	GND1	1			GND1	1			GND1	1		
118	PT13A	1	T		PT21A	1	T		PT21A	1	T	
119	PT12B	1	C		PT20B	1	C		PT20B	1	C	
120	PT12A	1	T		PT20A	1	T		PT20A	1	T	
121	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
122	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
123	PT10B	1	C		PT18B	1	C		PT18B	1	C	
124	PT10A	1	T		PT18A	1	T		PT18A	1	T	
125	VCCIO1	1			VCCIO1	1			VCCIO1	1		
126	VCCAUX	-			VCCAUX	-			VCCAUX	-		
127	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
128	GND0	0			GND0	0			GND0	0		
129	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
130	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
131	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
132	PT7B	0	C		PT15B	0	C		PT15B	0	C	
133	PT7A	0	T		PT15A	0	T		PT15A	0	T	
134	PT6B	0	C		PT14B	0	C		PT14B	0	C	
135	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
136	VCCIO0	0			VCCIO0	0			VCCIO0	0		
137	PT5B	0	C		PT13B	0	C		PT13B	0	C	
138	PT5A	0	T		PT13A	0	T		PT13A	0	T	
139	PT4B	0	C		PT12B	0	C		PT12B	0	C	
140	PT4A	0	T		PT12A	0	T		PT12A	0	T	
141	PT2B	0	C		PT10B	0	C		PT10B	0	C	
142	PT2A	0	T		PT10A	0	T		PT10A	0	T	
143	VCCIO0	0			VCCIO0	0			VCCIO0	0		
144*	GND0 GND7	-			GND0 GND7	-			GND0 GND7	-		

*Double bonded to the pin.

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	VCCAUX	-			VCCAUX	-		
137	PR9B	2	C	PCLKC2_0	PR18B	2	C	PCLKC2_0
138	GND2	2			GND2	2		
139	PR9A	2	T	PCLKT2_0	PR18A	2	T	PCLKT2_0
140	PR8B	2	C		PR17B	2	C	
141	PR8A	2	T		PR17A	2	T	
142	PR7B	2	C		PR16B	2	C	
143	PR7A	2	T		PR16A	2	T	
144	PR6B	2	C		PR15B	2	C	
145	VCCIO2	2			VCCIO2	2		
146	PR6A	2	T	RDQS6	PR15A	2	T	RDQS15
147	PR5B	2	C		PR14B	2	C	
148	PR5A	2	T		PR14A	2	T	
149	PR4B	2	C		PR13B	2	C	
150	PR4A	2	T		PR13A	2	T	
151	NC	-			GND	-		
152	NC	-			VCC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	PT33A	1			PT41A	1		
159	PT25B	1	C		PT33B	1	C	
160	PT25A	1	T		PT33A	1	T	
161	PT24B	1	C		PT32B	1	C	
162	PT24A	1	T		PT32A	1	T	
163	PT23B	1	C		PT31B	1	C	
164	PT23A	1	T		PT31A	1	T	
165	PT22B	1	C		PT30B	1	C	
166	PT22A	1	T	TDQS22	PT30A	1	T	TDQS30
167	PT21B	1	C		PT29B	1	C	
168	GND1	1			GND1	1		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
K2	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
K1	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
L2	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
L1	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
M2	PL13A	6	T		PL22A	6	T	
M1	PL13B	6	C		PL22B	6	C	
N1	PL14A	6	T		PL23A	6	T	
GND	GND6	6			GND6	6		
N2	PL14B	6	C		PL23B	6	C	
M4	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
M3	PL15B	6	C		PL24B	6	C	
P1	PL16A	6	T		PL25A	6	T	
R1	PL16B	6	C		PL25B	6	C	
P2	PL17A	6	T		PL26A	6	T	
P3	PL17B	6	C		PL26B	6	C	
N3	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
N4	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
P4	PB2A	5	T		PB2A	5	T	
N5	PB2B	5	C		PB2B	5	C	
P5	PB3A	5	T		PB3A	5	T	
P6	PB3B	5	C		PB3B	5	C	
R4	PB4A	5	T		PB4A	5	T	
R3	PB4B	5	C		PB4B	5	C	
T2	PB5A	5	T		PB5A	5	T	
T3	PB5B	5	C		PB5B	5	C	
R5	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
R6	PB6B	5	C		PB6B	5	C	
T4	PB7A	5	T		PB7A	5	T	
T5	PB7B	5	C		PB7B	5	C	
N6	PB8A	5	T		PB8A	5	T	
M6	PB8B	5	C		PB8B	5	C	
T6	PB9A	5	T		PB9A	5	T	
GND	GND5	5			GND5	5		
T7	PB9B	5	C		PB9B	5	C	
P7	PB10A	5	T		PB10A	5	T	
N7	PB10B	5	C		PB10B	5	C	
R7	PB11A	5	T		PB11A	5	T	
R8	PB11B	5	C		PB11B	5	C	
M7	PB12A	5	T		PB12A	5	T	
M8	PB12B	5	C		PB12B	5	C	
T8	PB13A	5	T		PB13A	5	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
P14	PR35B	3	C		PR43B	3	C	
P15	PR35A	3	T		PR43A	3	T	
R15	PR34B	3	C		PR42B	3	C	
R16	PR34A	3	T		PR42A	3	T	
M13	PR33B	3	C		PR41B	3	C	
M14	PR33A	3	T	RDQS33	PR41A	3	T	RDQS41
P16	PR32B	3	C	RLM0_PLLC_FB_A	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		
N16	PR32A	3	T	RLM0_PLLT_FB_A	PR40A	3	T	RLM0_PLLT_FB_A
N15	PR31B	3	C	RLM0_PLLC_IN_A	PR39B	3	C	RLM0_PLLC_IN_A
M15	PR31A	3	T	RLM0_PLLT_IN_A	PR39A	3	T	RLM0_PLLT_IN_A
M16	PR30B	3	C	DI/CSSPIN	PR38B	3	C	DI/CSSPIN
L16	PR30A	3	T	DOUT/CSON	PR38A	3	T	DOUT/CSON
K16	PR29B	3	C	BUSY/SISPI	PR37B	3	C	BUSY/SISPI
J16	PR29A	3	T	D7/SPID0	PR37A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
GND	GND3	3			GND3	3		
H16	PR27B	3	C		PR31B	3	C	
-	-	-			GND3	3		
H15	PR27A	3	T		PR31A	3	T	
G16	PR26B	3	C		PR30B	3	C	
G15	PR26A	3	T		PR30A	3	T	
K12	PR25B	3	C		PR29B	3	C	
J12	PR25A	3	T		PR29A	3	T	
J14	PR24B	3	C		PR28B	3	C	
J15	PR24A	3	T	RDQS24	PR28A	3	T	RDQS28
F16	PR23B	3	C		PR27B	3	C	
GND	GND3	3			GND3	3		
F15	PR23A	3	T		PR27A	3	T	
J13	PR22B	3	C		PR26B	3	C	
H13	PR22A	3	T		PR26A	3	T	
H14	PR21B	3	C		PR25B	3	C	
G14	PR21A	3	T		PR25A	3	T	
E16	PR20B	3	C		PR24B	3	C	
E15	PR20A	3	T		PR24A	3	T	
H12	PR18B	2	C	PCLKC2_0	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND2	2		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
E24	NC	-			E24	PR8B	2	C	
D24	NC	-			D24	PR8A	2	T	
E22	NC	-			E22	PR7B	2	C	
F22	NC	-			F22	PR7A	2	T	
E21	NC	-			E21	PR6B	2	C	
D22	NC	-			D22	PR6A	2	T	RDQS6
E23	PR2B	2	C	VREF1_2	E23	PR2B	2	C	VREF1_2
D23	PR2A	2	T	VREF2_2	D23	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
G20	NC	-			G20	PT65B	1	C	
F20	NC	-			F20	PT65A	1	T	
D21	NC	-			D21	PT64B	1	C	
C21	NC	-			C21	PT64A	1	T	
C23	NC	-			C23	PT63B	1	C	
C22	NC	-			C22	PT63A	1	T	
B23	NC	-			B23	PT62B	1	C	
C24	NC	-			C24	PT62A	1	T	TDQS62
D20	NC	-			D20	PT61B	1	C	
-	-	-			GND	GND1	1		
E19	NC	-			E19	PT61A	1	T	
B25	NC	-			B25	PT60B	1	C	
B24	NC	-			B24	PT60A	1	T	
B26	NC	-			B26	PT59B	1	C	
A25	NC	-			A25	PT59A	1	T	
C20	NC	-			C20	PT58B	1	C	
C19	NC	-			C19	PT58A	1	T	
A24	PT57B	1	C		A24	PT57B	1	C	
-	-	-			GND	GND1	1		
A23	PT57A	1	T		A23	PT57A	1	T	
E18	PT56B	1	C		E18	PT56B	1	C	
D19	PT56A	1	T		D19	PT56A	1	T	
F19	PT55B	1	C		F19	PT55B	1	C	
B22	PT55A	1	T		B22	PT55A	1	T	
G19	PT54B	1	C		G19	PT54B	1	C	
B21	PT54A	1	T	TDQS54	B21	PT54A	1	T	TDQS54
D18	PT53B	1	C		D18	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
C18	PT53A	1	T		C18	PT53A	1	T	
F18	PT52B	1	C		F18	PT52B	1	C	
A22	PT52A	1	T		A22	PT52A	1	T	
G18	PT51B	1	C		G18	PT51B	1	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A5	PT13B	0	C		A5	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
A4	PT13A	0	T		A4	PT13A	0	T	
F9	PT12B	0	C		F9	PT12B	0	C	
B6	PT12A	0	T		B6	PT12A	0	T	
E9	PT11B	0	C		E9	PT11B	0	C	
C8	PT11A	0	T		C8	PT11A	0	T	
G8	PT10B	0	C		G8	PT10B	0	C	
B5	PT10A	0	T		B5	PT10A	0	T	
A3	PT9B	0	C		A3	PT9B	0	C	
GND	GND0	0			GND	GND0	0		
A2	PT9A	0	T		A2	PT9A	0	T	
F8	PT8B	0	C		F8	PT8B	0	C	
B4	PT8A	0	T		B4	PT8A	0	T	
E8	PT7B	0	C		E8	PT7B	0	C	
B3	PT7A	0	T		B3	PT7A	0	T	
D8	PT6B	0	C		D8	PT6B	0	C	
G7	PT6A	0	T	TDQS6	G7	PT6A	0	T	TDQS6
C4	PT5B	0	C		C4	PT5B	0	C	
C5	PT5A	0	T		C5	PT5A	0	T	
E7	PT4B	0	C		E7	PT4B	0	C	
D4	PT4A	0	T		D4	PT4A	0	T	
F7	PT3B	0	C		F7	PT3B	0	C	
D6	PT3A	0	T		D6	PT3A	0	T	
D7	PT2B	0	C		D7	PT2B	0	C	
E6	PT2A	0	T		E6	PT2A	0	T	
GND	GND0	0			GND	GND0	0		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K15	GND	-			K15	GND	-		
K16	GND	-			K16	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L15	GND	-			L15	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M15	GND	-			M15	GND	-		
M16	GND	-			M16	GND	-		
M17	GND	-			M17	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N16	GND	-			N16	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P16	GND	-			P16	GND	-		
P17	GND	-			P17	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
R15	GND	-			R15	GND	-		
R16	GND	-			R16	GND	-		
R17	GND	-			R17	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T12	GND	-			T12	GND	-		
T13	GND	-			T13	GND	-		
T14	GND	-			T14	GND	-		
T15	GND	-			T15	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
H7	VCCAUX	-			H7	VCCAUX	-		
J19	VCCAUX	-			J19	VCCAUX	-		
J8	VCCAUX	-			J8	VCCAUX	-		
K7	VCCAUX	-			K7	VCCAUX	-		
L20	VCCAUX	-			L20	VCCAUX	-		
M20	VCCAUX	-			M20	VCCAUX	-		
M7	VCCAUX	-			M7	VCCAUX	-		
N20	VCCAUX	-			N20	VCCAUX	-		
P20	VCCAUX	-			P20	VCCAUX	-		
P7	VCCAUX	-			P7	VCCAUX	-		
T20	VCCAUX	-			T20	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
V19	VCCAUX	-			V19	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
W20	VCCAUX	-			W20	VCCAUX	-		
Y13	VCCAUX	-			Y13	VCCAUX	-		
Y7	VCCAUX	-			Y7	VCCAUX	-		
K19	VCC[1]	-			K19	VCCPLL	-		
L8	VCC[1]	-			L8	VCCPLL	-		
U19	VCC[1]	-			U19	VCCPLL	-		
U8	VCC[1]	-			U8	VCCPLL	-		

1. Tied to V_{CCPLL}.

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFECP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFECP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFECP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFECP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFECP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFECP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFECP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFECP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFECP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFECP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFECP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFECP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFECP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFECP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFECP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFECP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFECP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFECP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFECP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K

LatticeECP/EC Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com