



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	112
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (Tj)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-4qn208c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-4qn208c</a>

## Introduction

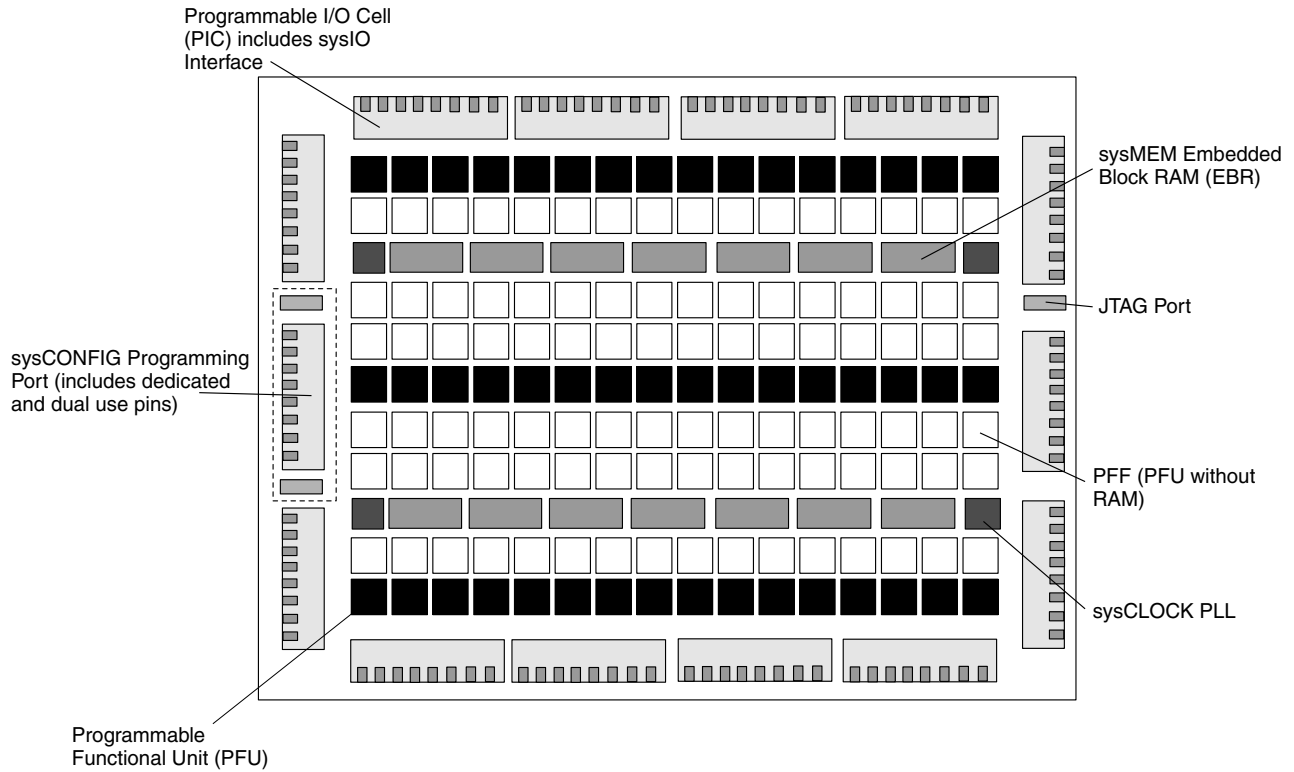
The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

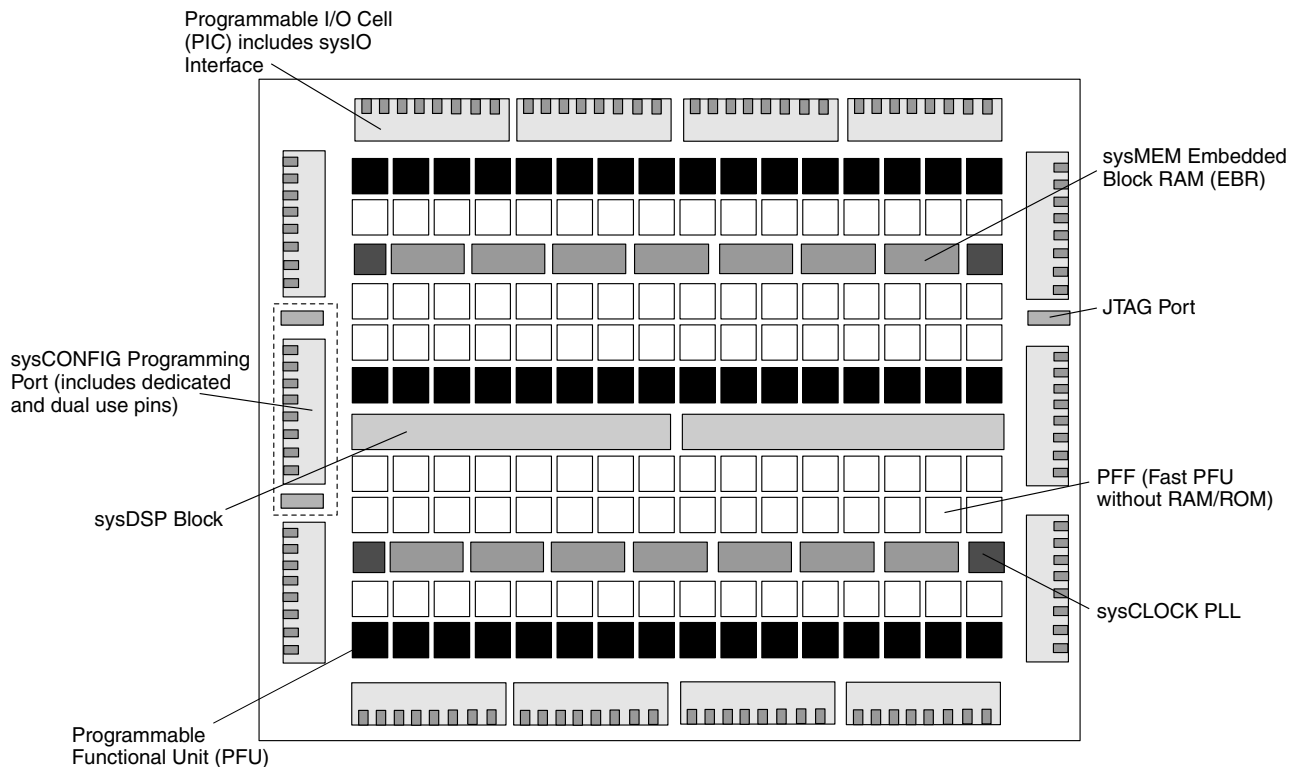
The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

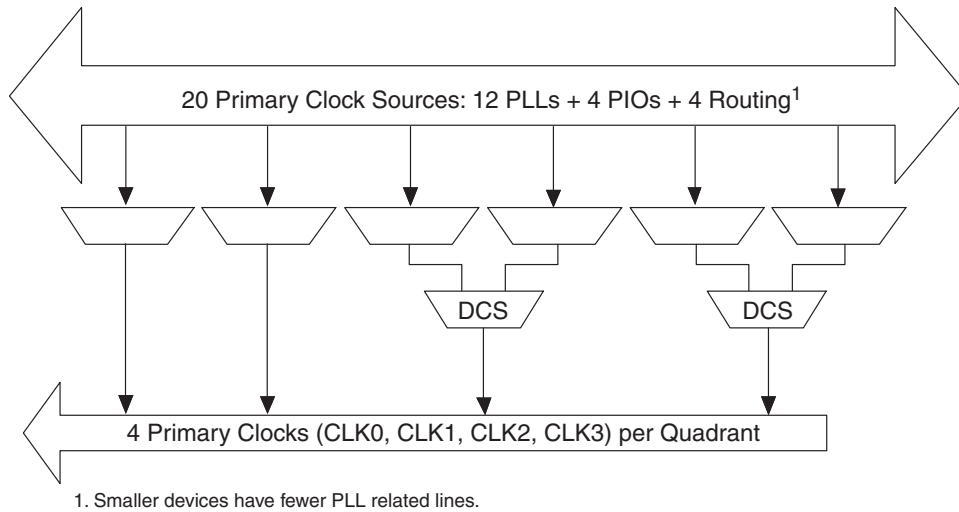
**Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)**



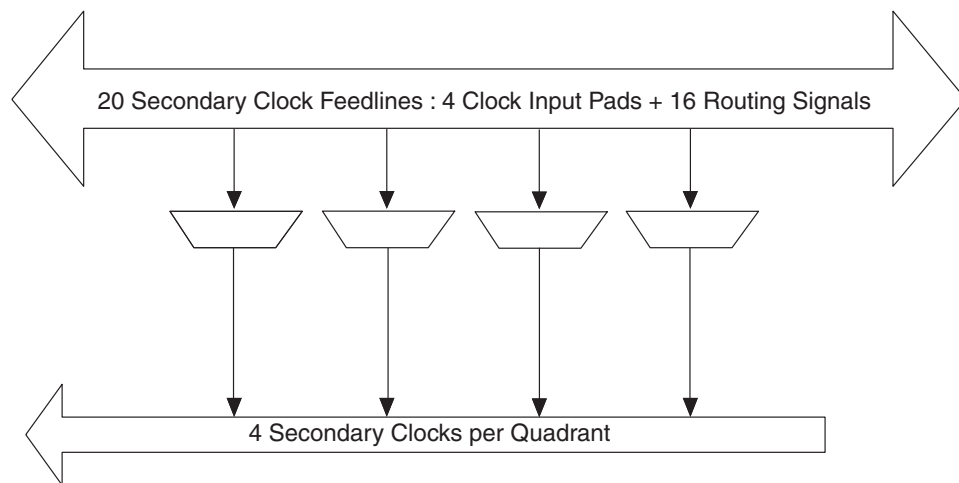
**Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)**



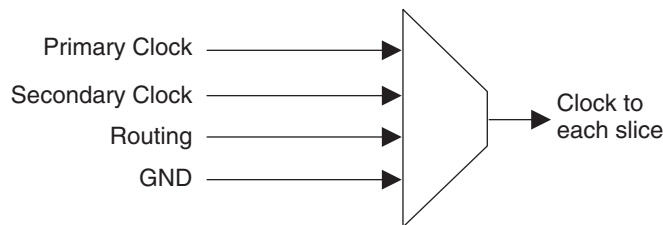
**Figure 2-8. Per Quadrant Primary Clock Selection**



**Figure 2-9. Per Quadrant Secondary Clock Selection**



**Figure 2-10. Slice Clock Selection**



### sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL\_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

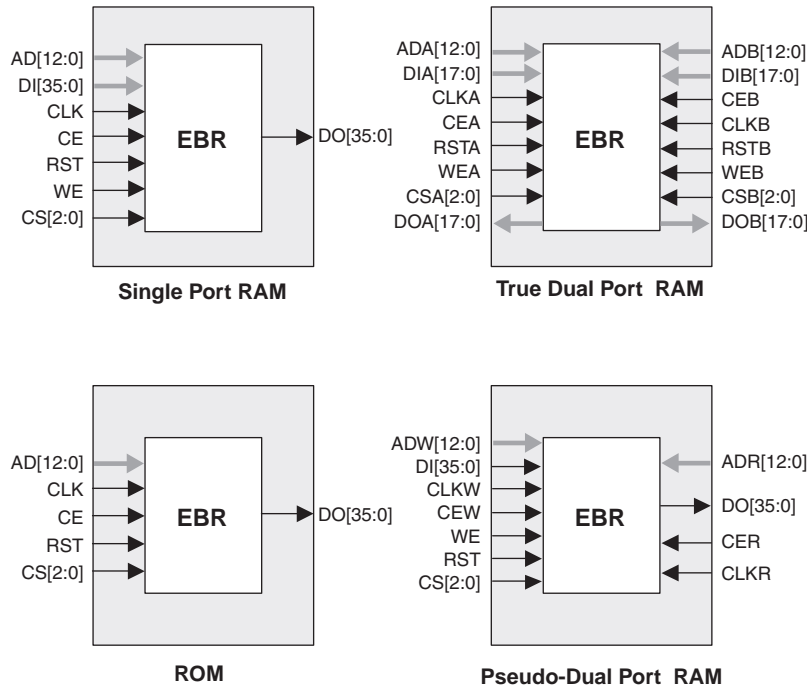
## Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

**Figure 2-15. sysMEM EBR Primitives**



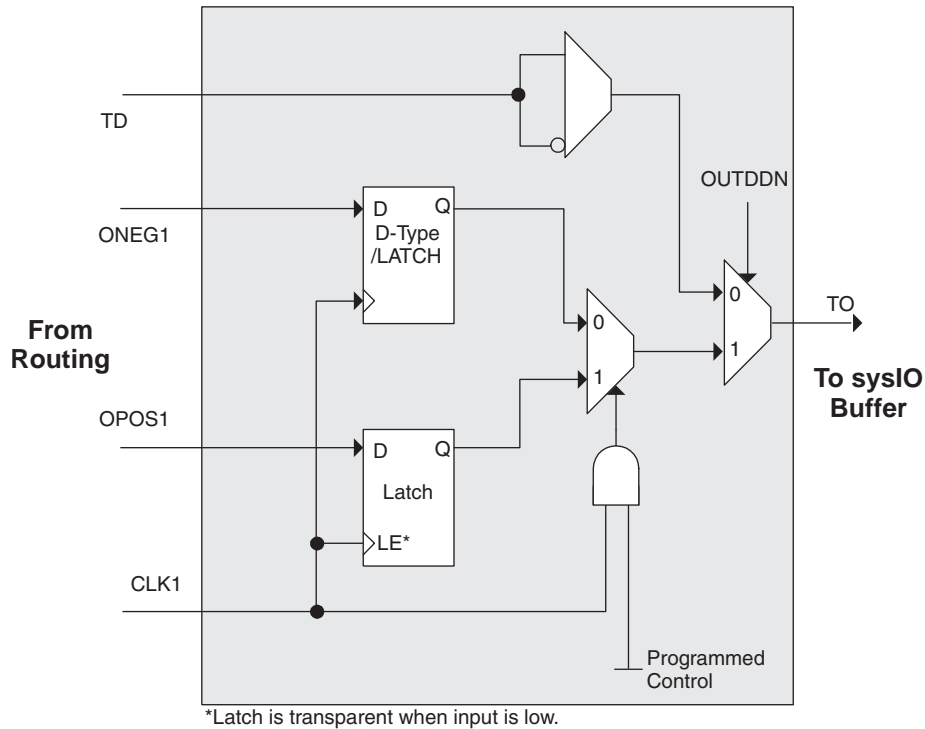
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-31. Tristate Register Block



### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

### DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

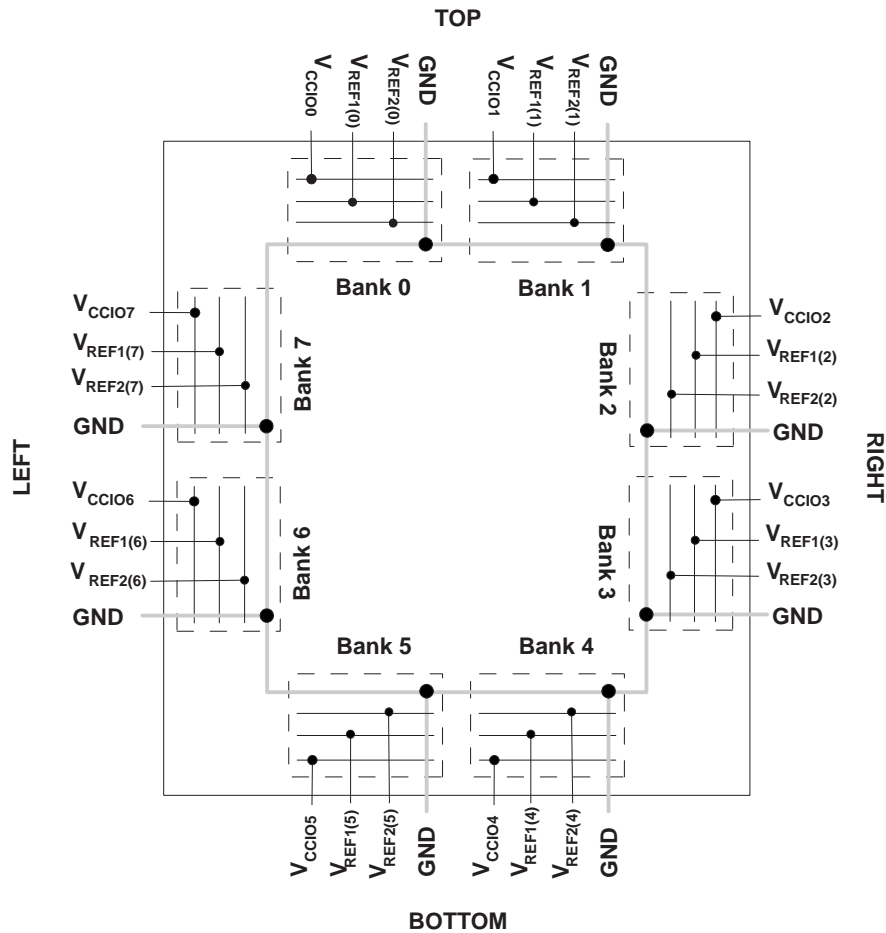
### DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-34. LatticeECP/EC Banks



LatticeECP/EC devices contain two types of sysI/O buffer pairs.

1. **Top and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)**

The sysI/O buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps. These I/O banks also support hot socketing with I<sub>DK</sub> less than 1mA. Note that the PCI clamp is enabled after V<sub>CC</sub>, V<sub>CCAUX</sub> and V<sub>CCIO</sub> are at valid operating levels and the device has been configured.

2. **Left and Right sysI/O Buffer Pairs (Differential and Single-Ended Outputs)**

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Only the left and right banks have LVDS differential output drivers. See the I<sub>DK</sub> specification for I/O leakage current during power-up.

## sysI/O Differential Electrical Characteristics

### LVDS

#### Over Recommended Operating Conditions

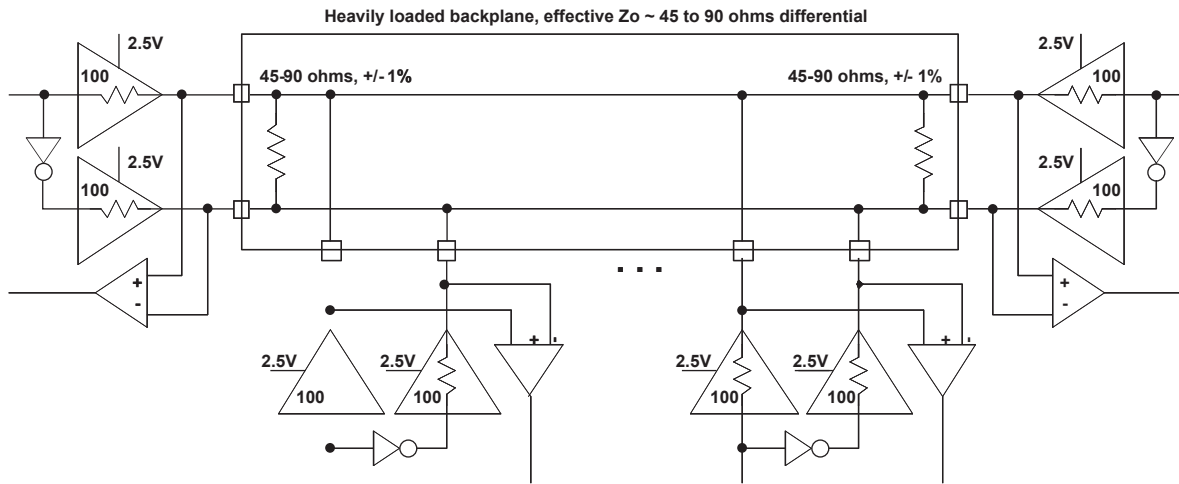
Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}, V_{INM}$	Input voltage		0	—	2.4	V
$V_{THD}$	Differential input threshold		+/-100	—	—	mV
$V_{CM}$	Input common mode voltage	100mV $\delta V_{THD}$	$V_{THD}/2$	1.2	1.8	V
		200mV $\delta V_{THD}$	$V_{THD}/2$	1.2	1.9	V
		350mV $\delta V_{THD}$	$V_{THD}/2$	1.2	2.0	V
$I_{IN}$	Input current	Power on or power off	—	—	+/-10	$\mu$ A
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	—	1.38	1.60	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	0.9V	1.03	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100$ Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} + V_{OM})/2, R_T = 100$ Ohm	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0V$ Driver outputs shorted	—	—	6	mA



**BLVDS**

The LatticeECP/EC devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

**Figure 3-2. BLVDS Multi-point Output Example**



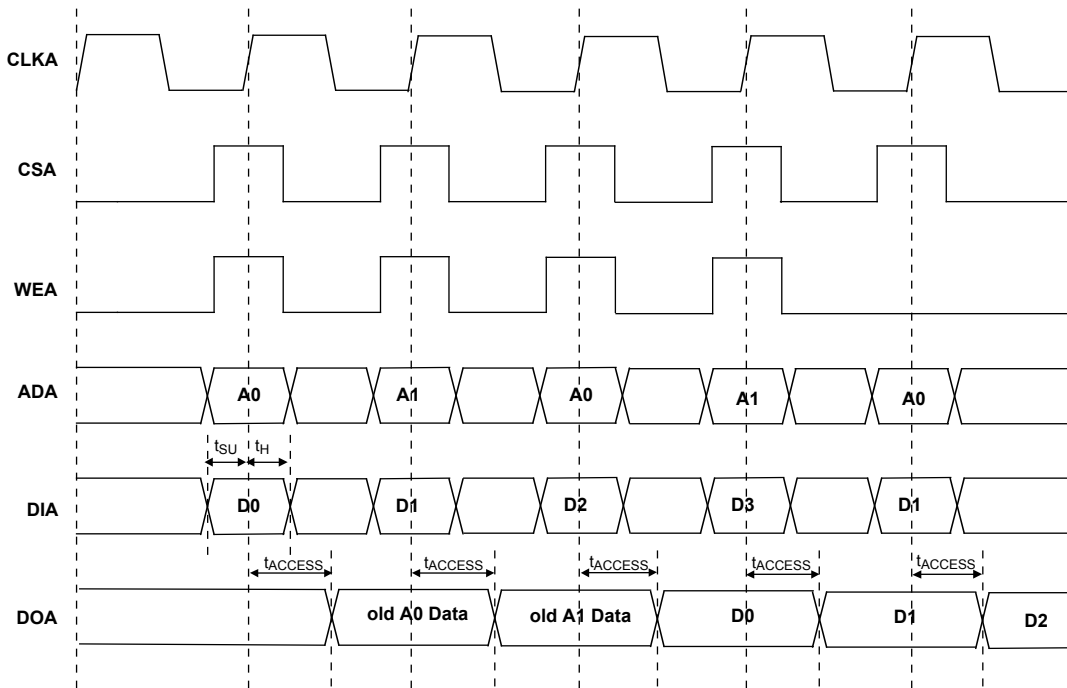
**Table 3-2. BLVDS DC Conditions<sup>1</sup>**

**Over Recommended Operating Conditions**

Parameter	Description	Typical		Units
		Zo = 45	Zo = 90	
Z <sub>OUT</sub>	Output impedance	100	100	ohm
R <sub>TLEFT</sub>	Left end termination	45	90	ohm
R <sub>TRIGHT</sub>	Right end termination	45	90	ohm
V <sub>OH</sub>	Output high voltage	1.375	1.48	V
V <sub>OL</sub>	Output low voltage	1.125	1.02	V
V <sub>OD</sub>	Output differential voltage	0.25	0.46	V
V <sub>CM</sub>	Output common mode voltage	1.25	1.25	V
I <sub>DC</sub>	DC output current	11.2	10.2	mA

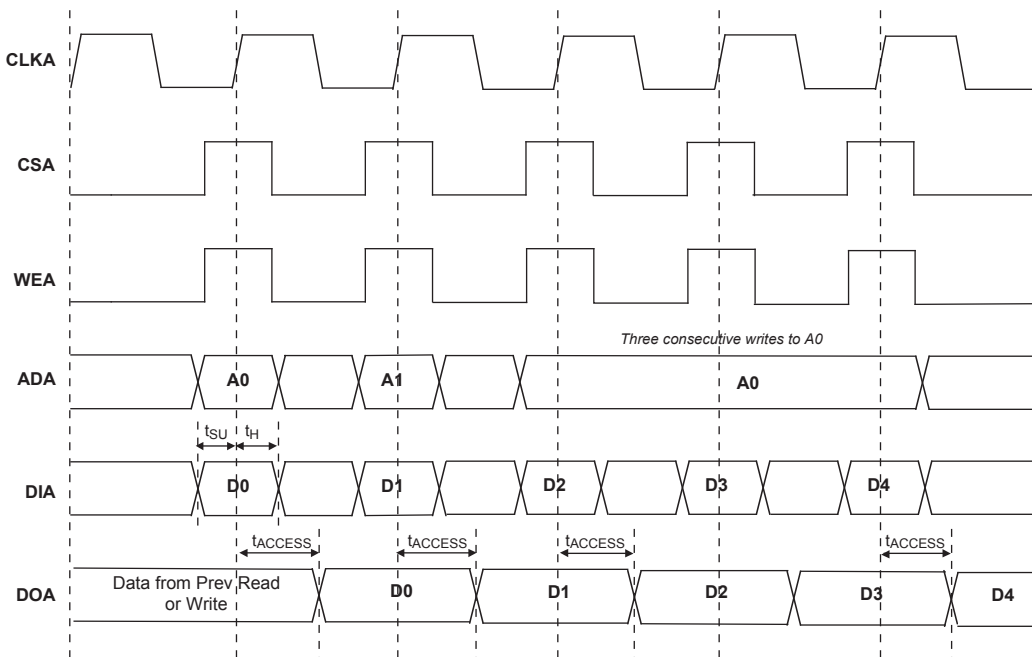
1. For input buffer, see LVDS table.

**Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)**



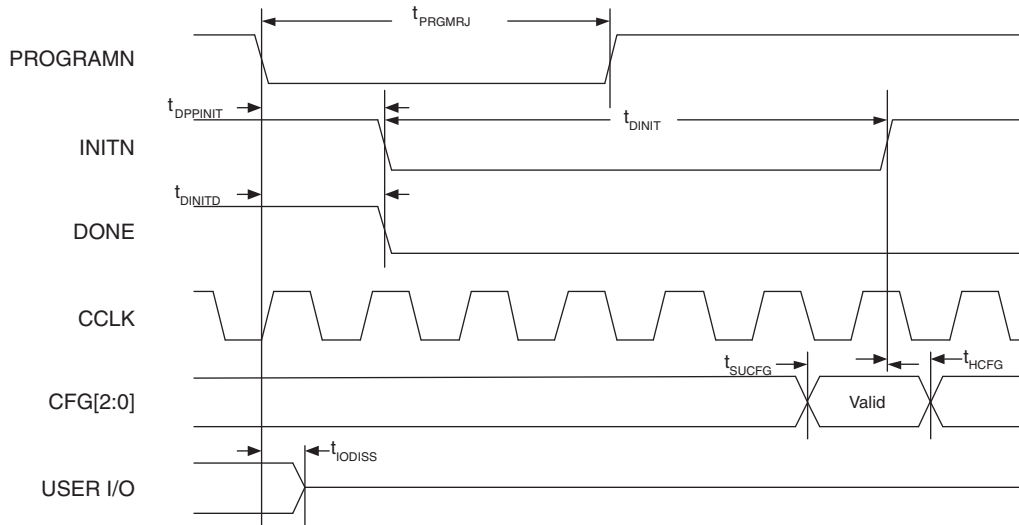
Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

**Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)**



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-17. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-18. Wake-Up Timing

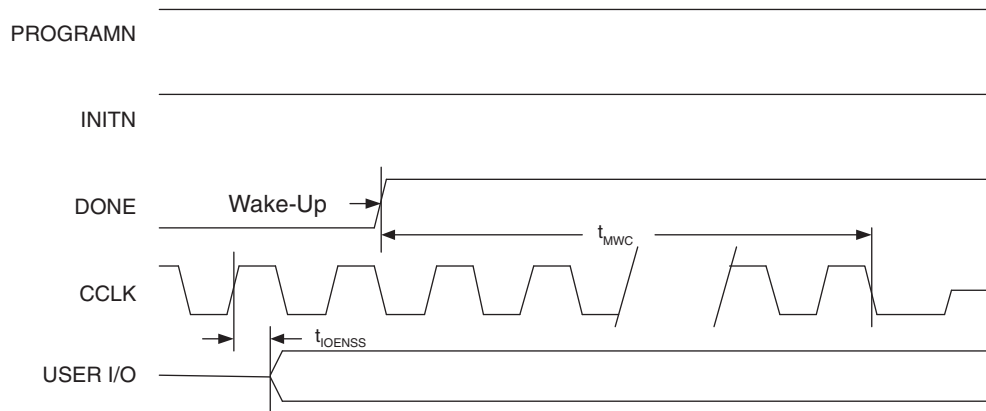
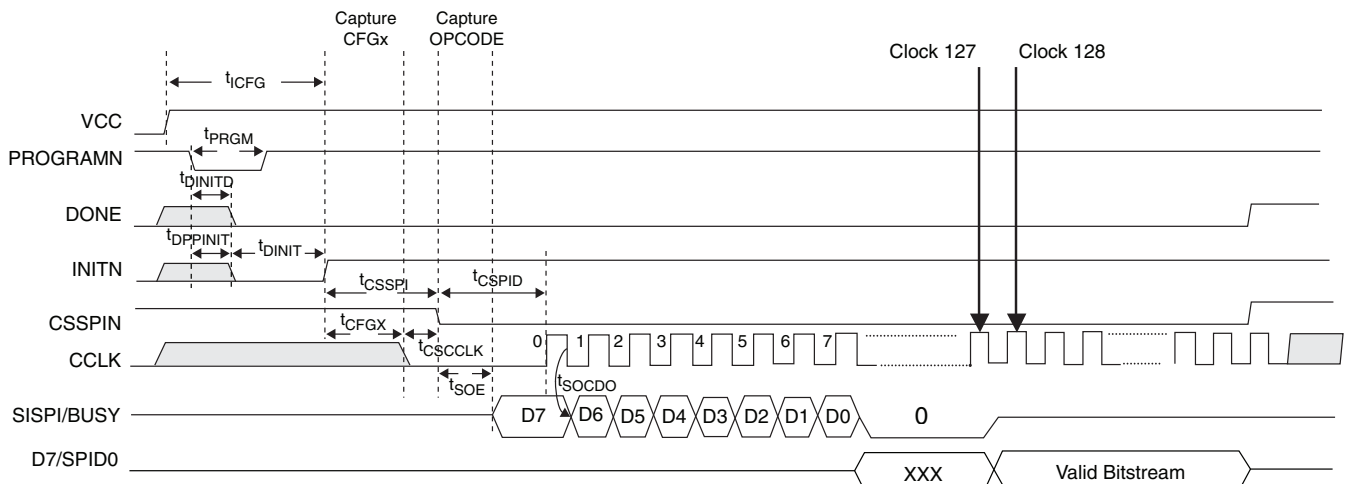


Figure 3-19. sysCONFIG SPI Port Sequence



**LFCEP/EC6, LFCEP/EC10 Logic Signal Connections: 208 PQFP**

Pin Number	LFCEP6/LFCEC6				LFCEP10/LFCEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:  
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
V12	PB16B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5
AB10	PB17A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB11	PB17B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0
Y12	PB18A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN
U11	PB18B	4	C	CS1N	U11	PB26B	4	C	CS1N	U11	PB26B	4	C	CS1N
W12	PB19A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4
U12	PB19B	4	C	CSN	U12	PB27B	4	C	CSN	U12	PB27B	4	C	CSN
W13	PB20A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4
U13	PB20B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7
AA12	PB21A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB12	PB21B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6
T13	PB22A	4	T	BDQS22	T13	PB30A	4	T	BDQS30	T13	PB30A	4	T	BDQS30
V13	PB22B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4
W14	PB23A	4	T		W14	PB31A	4	T		W14	PB31A	4	T	
U14	PB23B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3
Y13	PB24A	4	T		Y13	PB32A	4	T		Y13	PB32A	4	T	
V14	PB24B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2
AA13	PB25A	4	T		AA13	PB33A	4	T		AA13	PB33A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB13	PB25B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1
AA14	PB26A	4	T		AA14	PB34A	4	T		AA14	PB34A	4	T	
Y14	PB26B	4	C		Y14	PB34B	4	C		Y14	PB34B	4	C	
Y15	PB27A	4	T		Y15	PB35A	4	T		Y15	PB35A	4	T	
W15	PB27B	4	C		W15	PB35B	4	C		W15	PB35B	4	C	
V15	PB28A	4	T		V15	PB36A	4	T		V15	PB36A	4	T	
T14	PB28B	4	C		T14	PB36B	4	C		T14	PB36B	4	C	
AB14	PB29A	4	T		AB14	PB37A	4	T		AB14	PB37A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB15	PB29B	4	C		AB15	PB37B	4	C		AB15	PB37B	4	C	
AB16	PB30A	4	T	BDQS30	AB16	PB38A	4	T	BDQS38	AB16	PB38A	4	T	BDQS38
AA15	PB30B	4	C		AA15	PB38B	4	C		AA15	PB38B	4	C	
AB17	PB31A	4	T		AB17	PB39A	4	T		AB17	PB39A	4	T	
AA16	PB31B	4	C		AA16	PB39B	4	C		AA16	PB39B	4	C	
AB18	PB32A	4	T		AB18	PB40A	4	T		AB18	PB40A	4	T	
AA17	PB32B	4	C		AA17	PB40B	4	C		AA17	PB40B	4	C	
AB19	PB33A	4	T		AB19	PB41A	4	T		AB19	PB41A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA18	PB33B	4	C		AA18	PB41B	4	C		AA18	PB41B	4	C	
W16	NC	-			W16	NC	-			W16	PB42A	4	T	
U15	NC	-			U15	NC	-			U15	PB42B	4	C	
V16	NC	-			V16	NC	-			V16	PB43A	4	T	
U16	NC	-			U16	NC	-			U16	PB43B	4	C	
Y17	NC	-			Y17	NC	-			Y17	PB44A	4	T	
V17	NC	-			V17	NC	-			V17	PB44B	4	C	
AB20	NC	-			AB20	NC	-			AB20	PB45A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA19	NC	-			AA19	NC	-			AA19	PB45B	4	C	
Y16	NC	-			Y16	NC	-			Y16	PB46A	4	T	BDQS46

**LFECF/EC6, LFECF/EC10, LFECF/EC15 Logic Signal Connections:  
 484 fpBGA (Cont.)**

LFECF/EC6					LFECF/EC10					LFECF/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR9A	2	T	RUM0_PLLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR8A	2	T	RUM0_PLLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:  
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A4	NC	-			A4	PT9B	0	C		A4	PT9B	0	C	
B4	NC	-			B4	PT9A	0	T		B4	PT9A	0	T	
C4	NC	-			C4	PT8B	0	C		C4	PT8B	0	C	
C5	NC	-			C5	PT8A	0	T		C5	PT8A	0	T	
D6	NC	-			D6	PT7B	0	C		D6	PT7B	0	C	
B5	NC	-			B5	PT7A	0	T		B5	PT7A	0	T	
E6	NC	-			E6	PT6B	0	C		E6	PT6B	0	C	
C6	NC	-			C6	PT6A	0	T	TDQS6	C6	PT6A	0	T	TDQS6
A3	NC	-			A3	PT5B	0	C		A3	PT5B	0	C	
B3	NC	-			B3	PT5A	0	T		B3	PT5A	0	T	
F6	NC	-			F6	PT4B	0	C		F6	PT4B	0	C	
D5	NC	-			D5	PT4A	0	T		D5	PT4A	0	T	
F7	NC	-			F7	PT3B	0	C		F7	PT3B	0	C	
E8	NC	-			E8	PT3A	0	T		E8	PT3A	0	T	
G6	NC	-			G6	PT2B	0	C		G6	PT2B	0	C	
E7	NC	-			E7	PT2A	0	T		E7	PT2A	0	T	
GND	-	-			GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-			A22	GND	-		
AB1	GND	-			AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-			N12	GND	-		

**LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)**

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
A17	PT47A	1	T		A17	PT47A	1	T	
B15	PT46B	1	C		B15	PT46B	1	C	
A16	PT46A	1	T	TDQS46	A16	PT46A	1	T	TDQS46
A15	PT45B	1	C		A15	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
A14	PT45A	1	T		A14	PT45A	1	T	
G14	PT44B	1	C		G14	PT44B	1	C	
E15	PT44A	1	T		E15	PT44A	1	T	
D15	PT43B	1	C		D15	PT43B	1	C	
C15	PT43A	1	T		C15	PT43A	1	T	
C14	PT42B	1	C		C14	PT42B	1	C	
B14	PT42A	1	T		B14	PT42A	1	T	
A13	PT41B	1	C		A13	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
B13	PT41A	1	T		B13	PT41A	1	T	
E14	PT40B	1	C		E14	PT40B	1	C	
C13	PT40A	1	T		C13	PT40A	1	T	
F14	PT39B	1	C		F14	PT39B	1	C	
D14	PT39A	1	T		D14	PT39A	1	T	
E13	PT38B	1	C		E13	PT38B	1	C	
G13	PT38A	1	T	TDQS38	G13	PT38A	1	T	TDQS38
A12	PT37B	1	C		A12	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
B12	PT37A	1	T		B12	PT37A	1	T	
F13	PT36B	1	C		F13	PT36B	1	C	
D13	PT36A	1	T		D13	PT36A	1	T	
F12	PT35B	1	C	VREF2_1	F12	PT35B	1	C	VREF2_1
D12	PT35A	1	T	VREF1_1	D12	PT35A	1	T	VREF1_1
F11	PT34B	1	C		F11	PT34B	1	C	
C12	PT34A	1	T		C12	PT34A	1	T	
A11	PT33B	0	C	PCLKC0_0	A11	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A10	PT33A	0	T	PCLKT0_0	A10	PT33A	0	T	PCLKT0_0
E12	PT32B	0	C	VREF1_0	E12	PT32B	0	C	VREF1_0
E11	PT32A	0	T	VREF2_0	E11	PT32A	0	T	VREF2_0
B11	PT31B	0	C		B11	PT31B	0	C	
C11	PT31A	0	T		C11	PT31A	0	T	
B9	PT30B	0	C		B9	PT30B	0	C	
B10	PT30A	0	T	TDQS30	B10	PT30A	0	T	TDQS30
A9	PT29B	0	C		A9	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
A8	PT29A	0	T		A8	PT29A	0	T	
D11	PT28B	0	C		D11	PT28B	0	C	
C10	PT28A	0	T		C10	PT28A	0	T	



**LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)**

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-		

**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
L24	PR17A	2	T		L24	PR29A	2	T	
K25	PR16B	2	C		K25	PR28B	2	C	
J25	PR16A	2	T		J25	PR28A	2	T	
J26	PR15B	2	C		J26	PR27B	2	C	
H26	PR15A	2	T		H26	PR27A	2	T	
H25	PR14B	2	C		H25	PR26B	2	C	
GND	GND2	2			GND	GND2	2		
J24	PR14A	2	T		J24	PR26A	2	T	
K21	PR13B	2	C		K21	PR25B	2	C	
K22	PR13A	2	T		K22	PR25A	2	T	
K20	PR12B	2	C		K20	PR24B	2	C	
J20	PR12A	2	T		J20	PR24A	2	T	
K23	PR11B	2	C		K23	PR23B	2	C	
K24	PR11A	2	T		K24	PR23A	2	T	RDQS23
J21	NC	-			J21	PR22B	2	C	
-	-	-			GND	GND2	2		
J22	NC	-			J22	PR22A	2	T	
J23	NC	-			J23	PR21B	2	C	
H22	NC	-			H22	PR21A	2	T	
G26	NC	-			G26	PR20B	2	C	
F26	NC	-			F26	PR20A	2	T	
E26	NC	-			E26	PR19B	2	C	
E25	NC	-			E25	PR19A	2	T	
F25	PR9B	2	C	RUM0_PLLC_FB_A	F25	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
G25	PR9A	2	T	RUM0_PLLT_FB_A	G25	PR17A	2	T	RUM0_PLLT_FB_A
H23	PR8B	2	C	RUM0_PLLC_IN_A	H23	PR16B	2	C	RUM0_PLLC_IN_A
H24	PR8A	2	T	RUM0_PLLT_IN_A	H24	PR16A	2	T	RUM0_PLLT_IN_A
H21	PR7B	2	C		H21	PR15B	2	C	
G21	PR7A	2	T		G21	PR15A	2	T	
D26	PR6B	2	C		D26	PR14B	2	C	
D25	PR6A	2	T	RDQS6	D25	PR14A	2	T	RDQS14
F21	PR5B	2	C		F21	PR13B	2	C	
-	-	-			GND	GND2	2		
G22	PR5A	2	T		G22	PR13A	2	T	
G24	PR4B	2	C		G24	PR12B	2	C	
G23	PR4A	2	T		G23	PR12A	2	T	
C26	PR3B	2	C		C26	PR11B	2	C	
C25	PR3A	2	T		C25	PR11A	2	T	
F24	NC	-			F24	PR9B	2	C	
-	-	-			GND	GND2	2		
F23	NC	-			F23	PR9A	2	T	

**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M15	GND	-			M15	GND	-		
M16	GND	-			M16	GND	-		
M17	GND	-			M17	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N16	GND	-			N16	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P16	GND	-			P16	GND	-		
P17	GND	-			P17	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
R15	GND	-			R15	GND	-		
R16	GND	-			R16	GND	-		
R17	GND	-			R17	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T12	GND	-			T12	GND	-		
T13	GND	-			T13	GND	-		
T14	GND	-			T14	GND	-		
T15	GND	-			T15	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		

**LatticeEC Industrial (Continued)**

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

**LatticeECP Industrial**

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Date	Version	Section	Change Summary
December 2004	01.4	Architecture	Updated Hot Socketing Recommended Power Up Sequence section.
		Pinout Information	Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Pin Information
			Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Power Supply and NC Connections
			Added LFEC1 and LFEC3 100 TQFP Pinout
			Added LFEC1 and LFEC3 144 TQFP Pinout
			Added LFEC1, LFEC3 and LFECP/EC10 208 PQFP Pinout
			Added LFEC3, LFECP/EC10 and LFECP/EC15 256 fpBGA Pinout
		Ordering Information	Added LFECP/EC10 and LFECP/EC15 484 fpBGA Pinout
			Added Lead-Free Package Designators
Supplemental Information	Updated list of technical notes.		
April 2005	01.5	Architecture	EBR memory support section has been updated with clarification.
			Updated sysIO buffer pair section.
		DC & Switching Characteristics	Hot Socketing Specification has been updated.
			DC Electrical Characteristics table ( $I_{IL}$ , $I_{IH}$ ) has been updated.
			Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			External Switching Characteristics section has been updated.
			Removed $t_{RSTW}$ spec. from PLL Parameter table.
			$t_{RST}$ specifications have been updated.
		Pinout Information	sysCONFIG Port Timing Specifications ( $t_{BSC}$ , $t_{ODISS}$ , $t_{PRGMRJ}$ ) have been updated.
			Added LFECP/EC33 Pinout Information
			Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
			484-fpBGA logic connection has been updated (Ball # J6, J17, P6 and P17 for ECP/EC33 are now called VCCPLL).
672-fpBGA logic connection has been updated (Ball # K19, L8, U19, U8 for ECP/EC33 are now called VCCPLL).			
May 2005	01.6	Introduction	ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.
		Architecture	Table 2-10 has been updated (ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.)
			Recommended Power Up Sequence section has been removed.
		DC & Switching Characteristics	Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			Vos test condition has been updated to $(VOP+VOM)/2$ .
			Register-to-Register performance table has been updated (rev. G 0.27).
			External switching characteristics have been updated (rev. G 0.27).
			Internal timing parameters have been updated (rev. G 0.27).
			Timing adders have been updated (rev. G 0.27).
		Pinout Information	sysCONFIG port timing specifications have been updated.
			Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	OPN list has been updated.