



Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	97
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-4tn144c

Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

Figure 2-13. DCS Block Primitive

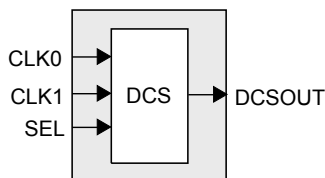


Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-27 shows the input register waveforms for DDR operation and Figure 2-28 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Diagram

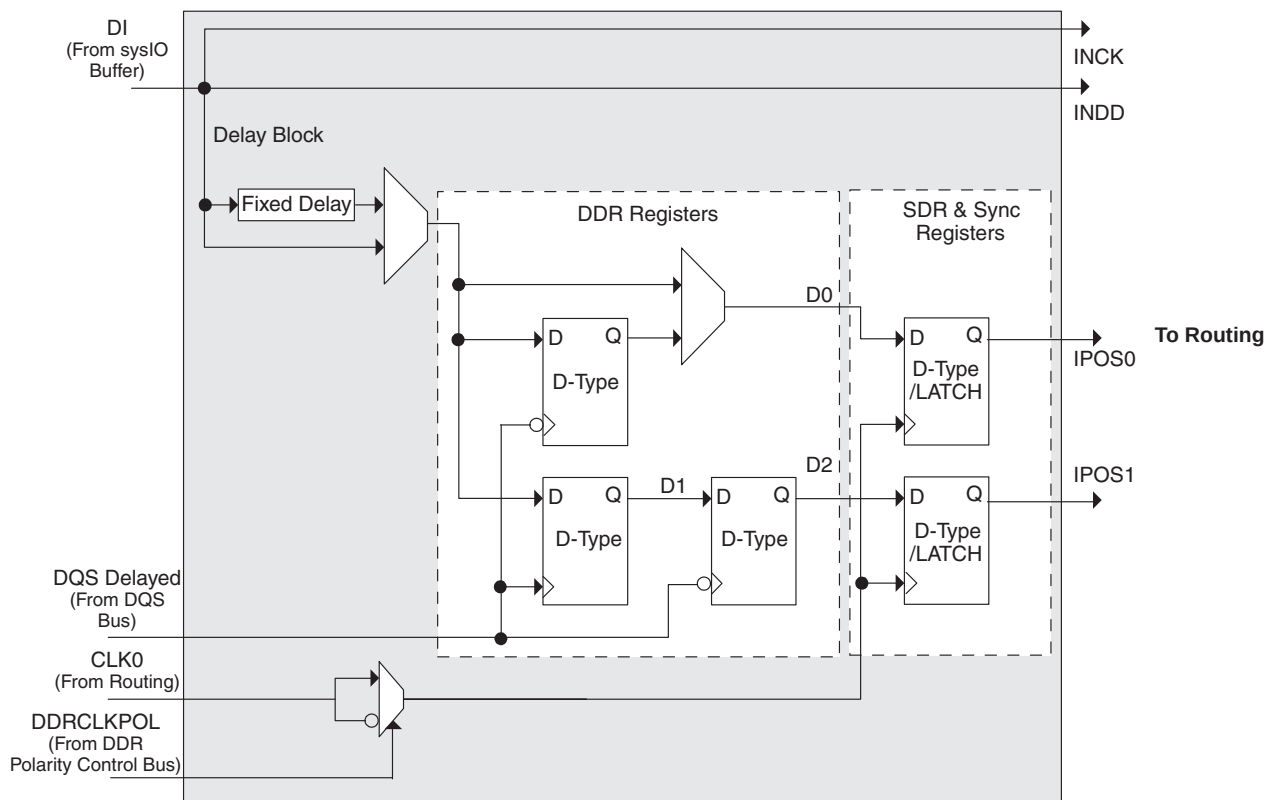


Figure 2-29. Output Register Block

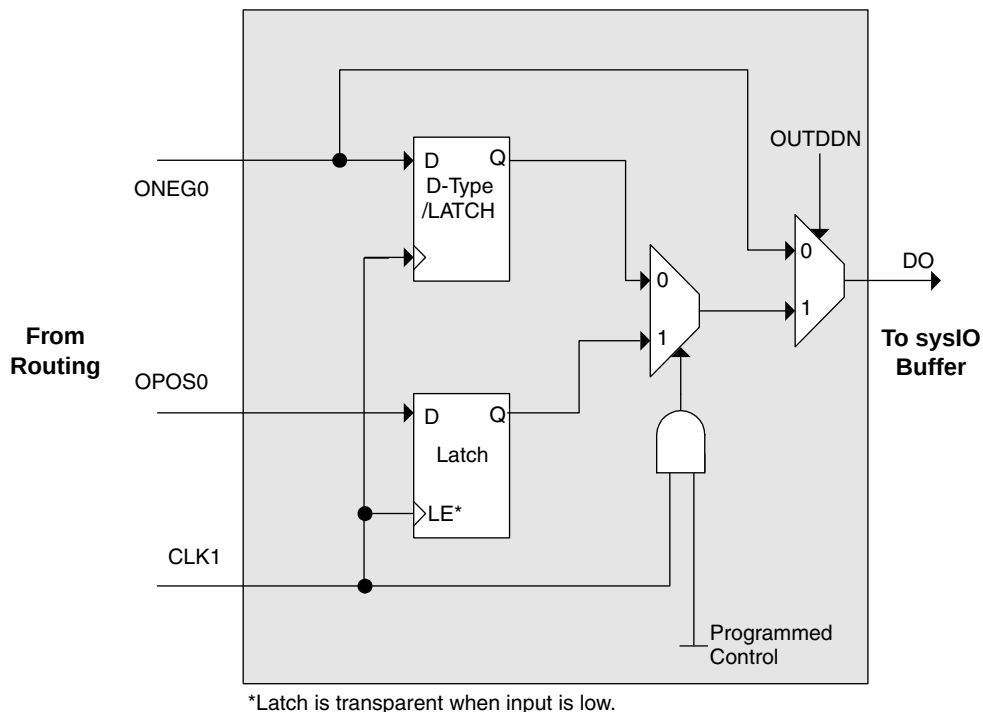
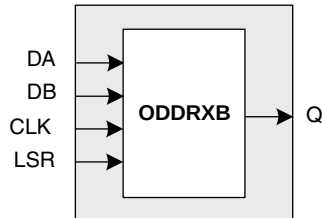


Figure 2-30. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

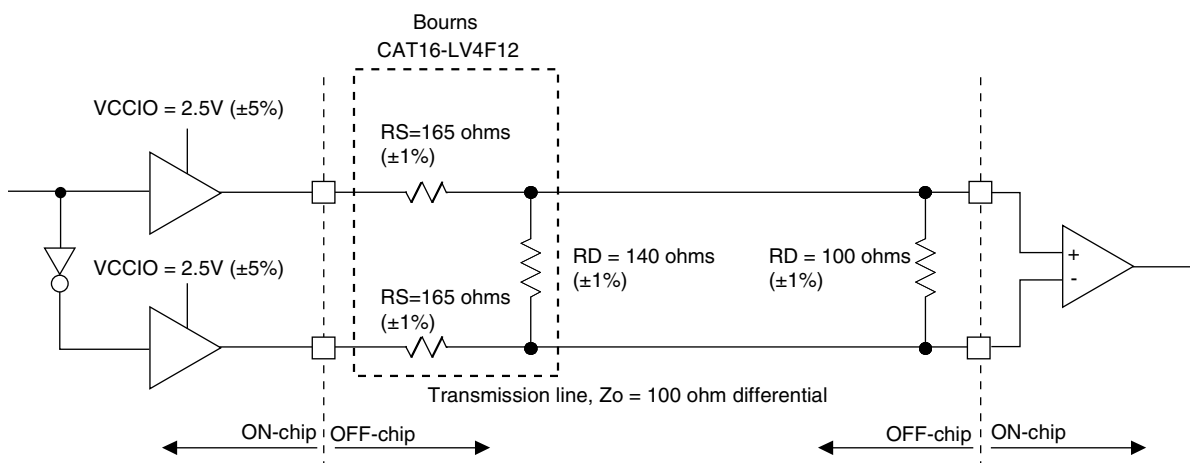
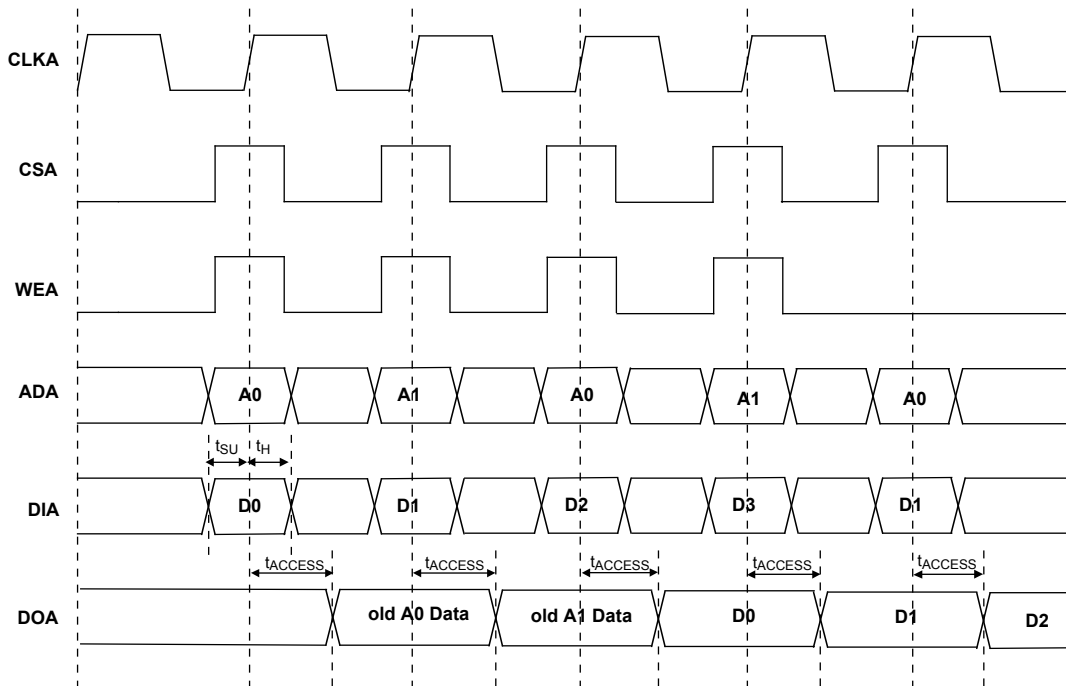


Table 3-1. LVDS25E DC Conditions

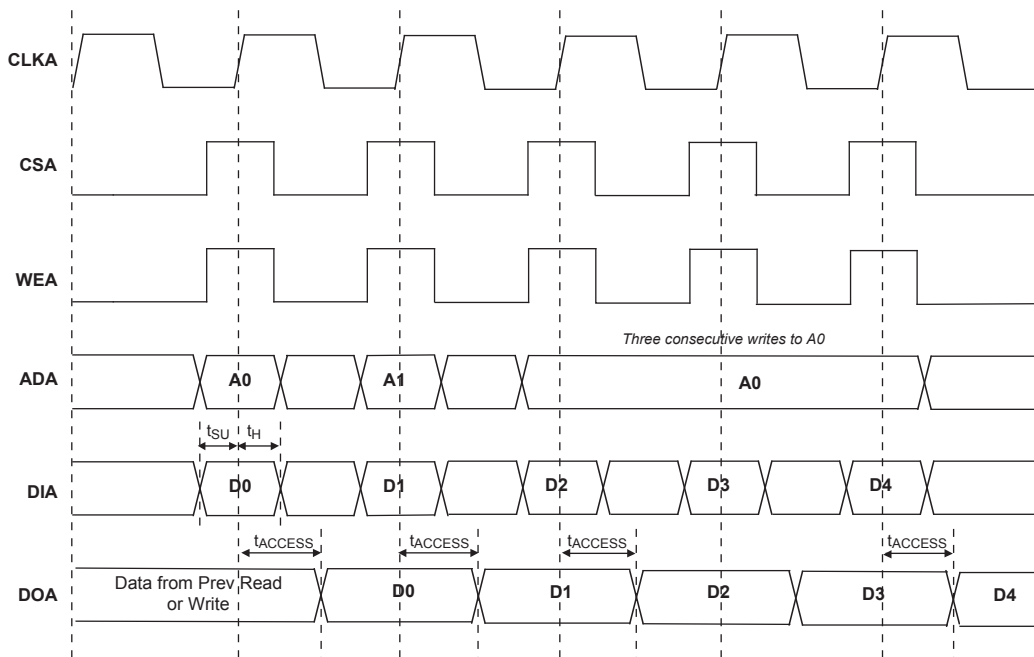
Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.42	V
V_{OL}	Output low voltage	1.08	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	$\%$

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
$t_{HMC DI}$	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from t_{ICFG} to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data out pin used to shift data out of device using 1149.1.
V _{CCJ}	—	V _{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (Active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSO	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPIN	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes.

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
82	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
83	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
84	PT10B	1	C		PT18B	1	C	
85	PT10A	1	T		PT18A	1	T	
86	VCCIO1	1			VCCIO1	1		
87	VCCAUX	-			VCCAUX	-		
88	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
89	GND0	0			GND0	0		
90	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
91	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
92	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
93	PT7B	0			PT15B	0		
94	PT6B	0	C		PT14B	0	C	
95	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
96	PT4B	0	C		PT12B	0	C	
97	PT4A	0	T		PT12A	0	T	
98	PT2B	0	C		PT10B	0	C	
99	PT2A	0	T		PT10A	0	T	
100	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

LFEC6P/EC6, LFEC6P/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC6P/EC6				LFEC6P/EC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB18A	4	T	WRITEN	PB26A	4	T	WRITEN
87	PB18B	4	C	CS1N	PB26B	4	C	CS1N
88	PB19A	4	T	VREF1_4	PB27A	4	T	VREF1_4
89	PB19B	4	C	CSN	PB27B	4	C	CSN
90	PB20A	4	T	VREF2_4	PB28A	4	T	VREF2_4
91	PB20B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
92	PB21A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB21B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
95	PB22A	4	T	BDQS22	PB30A	4	T	BDQS30
96	PB22B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
97	PB23A	4	T		PB31A	4	T	
98	PB23B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
99	PB24A	4	T		PB32A	4	T	
100	PB24B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
101	PB25A	4	T		PB33A	4	T	
102	PB25B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
103	PB33A	4			PB41A	4		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR27B	3	C	VREF2_3	PR36B	3	C	VREF2_3
108	PR27A	3	T	VREF1_3	PR36A	3	T	VREF1_3
109	PR26B	3	C		PR35B	3	C	
110	PR26A	3	T		PR35A	3	T	
111	PR25B	3	C		PR34B	3	C	
112	PR25A	3	T		PR34A	3	T	
113	PR24B	3	C		PR33B	3	C	
114	PR24A	3	T	RDQS24	PR33A	3	T	RDQS33
115	PR23B	3	C	RLM0_PLLC_FB_A	PR32B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR23A	3	T	RLM0_PLLT_FB_A	PR32A	3	T	RLM0_PLLT_FB_A
118	PR22B	3	C	RLM0_PLLC_IN_A	PR31B	3	C	RLM0_PLLC_IN_A
119	PR22A	3	T	RLM0_PLLT_IN_A	PR31A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR21B	3	C	DI/CSSPIN	PR30B	3	C	DI/CSSPIN
122	PR21A	3	T	DOUT/CSON	PR30A	3	T	DOUT/CSON
123	PR20B	3	C	BUSY/SISPI	PR29B	3	C	BUSY/SISPI
124	PR20A	3	T	D7/SPID0	PR29A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
F14	PT23B	1	C		F14	PT31B	1	C		F14	PT31B	1	C	
D14	PT23A	1	T		D14	PT31A	1	T		D14	PT31A	1	T	
E13	PT22B	1	C		E13	PT30B	1	C		E13	PT30B	1	C	
G13	PT22A	1	T	TDQS22	G13	PT30A	1	T	TDQS30	G13	PT30A	1	T	TDQS30
A12	PT21B	1	C		A12	PT29B	1	C		A12	PT29B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B12	PT21A	1	T		B12	PT29A	1	T		B12	PT29A	1	T	
F13	PT20B	1	C		F13	PT28B	1	C		F13	PT28B	1	C	
D13	PT20A	1	T		D13	PT28A	1	T		D13	PT28A	1	T	
F12	PT19B	1	C	VREF2_1	F12	PT27B	1	C	VREF2_1	F12	PT27B	1	C	VREF2_1
D12	PT19A	1	T	VREF1_1	D12	PT27A	1	T	VREF1_1	D12	PT27A	1	T	VREF1_1
F11	PT18B	1	C		F11	PT26B	1	C		F11	PT26B	1	C	
C12	PT18A	1	T		C12	PT26A	1	T		C12	PT26A	1	T	
A11	PT17B	0	C	PCLKC0_0	A11	PT25B	0	C	PCLKC0_0	A11	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0			GND	GND0	0		
A10	PT17A	0	T	PCLKT0_0	A10	PT25A	0	T	PCLKT0_0	A10	PT25A	0	T	PCLKT0_0
E12	PT16B	0	C	VREF1_0	E12	PT24B	0	C	VREF1_0	E12	PT24B	0	C	VREF1_0
E11	PT16A	0	T	VREF2_0	E11	PT24A	0	T	VREF2_0	E11	PT24A	0	T	VREF2_0
B11	PT15B	0	C		B11	PT23B	0	C		B11	PT23B	0	C	
C11	PT15A	0	T		C11	PT23A	0	T		C11	PT23A	0	T	
B9	PT14B	0	C		B9	PT22B	0	C		B9	PT22B	0	C	
B10	PT14A	0	T	TDQS14	B10	PT22A	0	T	TDQS22	B10	PT22A	0	T	TDQS22
A9	PT13B	0	C		A9	PT21B	0	C		A9	PT21B	0	C	
GND	GND0	0			GND	GND0	0			GND	GND0	0		
A8	PT13A	0	T		A8	PT21A	0	T		A8	PT21A	0	T	
D11	PT12B	0	C		D11	PT20B	0	C		D11	PT20B	0	C	
C10	PT12A	0	T		C10	PT20A	0	T		C10	PT20A	0	T	
A7	PT11B	0	C		A7	PT19B	0	C		A7	PT19B	0	C	
A6	PT11A	0	T		A6	PT19A	0	T		A6	PT19A	0	T	
B7	PT10B	0	C		B7	PT18B	0	C		B7	PT18B	0	C	
B8	PT10A	0	T		B8	PT18A	0	T		B8	PT18A	0	T	
A5	PT9B	0	C		A5	PT17B	0	C		A5	PT17B	0	C	
GND	GND0	0			GND	GND0	0			GND	GND0	0		
B6	PT9A	0	T		B6	PT17A	0	T		B6	PT17A	0	T	
G10	PT8B	0	C		G10	PT16B	0	C		G10	PT16B	0	C	
E10	PT8A	0	T		E10	PT16A	0	T		E10	PT16A	0	T	
F10	PT7B	0	C		F10	PT15B	0	C		F10	PT15B	0	C	
D10	PT7A	0	T		D10	PT15A	0	T		D10	PT15A	0	T	
G9	PT6B	0	C		G9	PT14B	0	C		G9	PT14B	0	C	
E9	PT6A	0	T	TDQS6	E9	PT14A	0	T	TDQS14	E9	PT14A	0	T	TDQS14
C9	PT5B	0	C		C9	PT13B	0	C		C9	PT13B	0	C	
GND	-	-			GND	GND0	0			GND	GND0	0		
C8	PT5A	0	T		C8	PT13A	0	T		C8	PT13A	0	T	
F9	PT4B	0	C		F9	PT12B	0	C		F9	PT12B	0	C	
D9	PT4A	0	T		D9	PT12A	0	T		D9	PT12A	0	T	
F8	PT3B	0	C		F8	PT11B	0	C		F8	PT11B	0	C	
D7	PT3A	0	T		D7	PT11A	0	T		D7	PT11A	0	T	
D8	PT2B	0	C		D8	PT10B	0	C		D8	PT10B	0	C	
C7	PT2A	0	T		C7	PT10A	0	T		C7	PT10A	0	T	
GND	GND0	0			GND	GND0	0			GND	GND0	0		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
L7	VCCIO7	7			L7	VCCIO7	7		
L8	VCCIO7	7			L8	VCCIO7	7		
G15	VCCAUX	-			G15	VCCAUX	-		
G16	VCCAUX	-			G16	VCCAUX	-		
G7	VCCAUX	-			G7	VCCAUX	-		
G8	VCCAUX	-			G8	VCCAUX	-		
H16	VCCAUX	-			H16	VCCAUX	-		
H7	VCCAUX	-			H7	VCCAUX	-		
R16	VCCAUX	-			R16	VCCAUX	-		
R7	VCCAUX	-			R7	VCCAUX	-		
T15	VCCAUX	-			T15	VCCAUX	-		
T16	VCCAUX	-			T16	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
J6	VCC ¹	-			J6	VCCPLL	-		
J17	VCC ¹	-			J17	VCCPLL	-		
P6	VCC ¹	-			P6	VCCPLL	-		
P17	VCC ¹	-			P17	VCCPLL	-		
A2	NC	-			A2	NC	-		
AB2	NC	-			AB2	NC	-		
A21	NC	-			A21	NC	-		

 1. Tied to V_{CCPLL}.

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7		
E3	PL2A	7	T	VREF2_7	E3	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
E5	NC	-			E5	PL6A	7	T	LDQS6
D5	NC	-			D5	PL6B	7	C	
F4	NC	-			F4	PL7A	7	T	
F5	NC	-			F5	PL7B	7	C	
C3	NC	-			C3	PL8A	7	T	
D3	NC	-			D3	PL8B	7	C	
C2	NC	-			C2	PL9A	7	T	
-	-	-			GND	GND7	7		
B2	NC	-			B2	PL9B	7	C	
B1	PL3A	7	T		B1	PL10A	7	T	
C1	PL3B	7	C		C1	PL10B	7	C	
F3	PL4A	7	T		F3	PL11A	7	T	
G3	PL4B	7	C		G3	PL11B	7	C	
D2	PL5A	7	T		D2	PL12A	7	T	
E2	PL5B	7	C		E2	PL12B	7	C	
-	-	-			GND	GND7	7		
D1	PL6A	7	T	LDQS6	D1	PL14A	7	T	LDQS14
E1	PL6B	7	C		E1	PL14B	7	C	
F2	PL7A	7	T		F2	PL15A	7	T	
G2	PL7B	7	C		G2	PL15B	7	C	
F6	PL8A	7	T	LUM0_PLLT_IN_A	F6	PL16A	7	T	LUM0_PLLT_IN_A
G6	PL8B	7	C	LUM0_PLLC_IN_A	G6	PL16B	7	C	LUM0_PLLC_IN_A
H4	PL9A	7	T	LUM0_PLLT_FB_A	H4	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
G4	PL9B	7	C	LUM0_PLLC_FB_A	G4	PL17B	7	C	LUM0_PLLC_FB_A
H6	NC	-			H6	PL19A	7	T	
J7	NC	-			J7	PL19B	7	C	
G5	NC	-			G5	PL20A	7	T	
H5	NC	-			H5	PL20B	7	C	
H3	NC	-			H3	PL21A	7	T	
J3	NC	-			J3	PL21B	7	C	
H2	NC	-			H2	PL22A	7	T	
-	-	-			GND	GND7	7		
J2	NC	-			J2	PL22B	7	C	
J4	PL11A	7	T		J4	PL23A	7	T	LDQS23
J5	PL11B	7	C		J5	PL23B	7	C	
K4	PL12A	7	T		K4	PL24A	7	T	
K5	PL12B	7	C		K5	PL24B	7	C	
J6	PL13A	7	T		J6	PL25A	7	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
P5	PL32B	6	C		P5	PL44B	6	C	
P6	PL33A	6	T		P6	PL45A	6	T	
R5	PL33B	6	C		R5	PL45B	6	C	
U1	PL34A	6	T		U1	PL46A	6	T	
U2	PL34B	6	C		U2	PL46B	6	C	
T3	PL35A	6	T		T3	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
T4	PL35B	6	C		T4	PL47B	6	C	
R6	PL36A	6	T	LDQS36	R6	PL48A	6	T	LDQS48
T5	PL36B	6	C		T5	PL48B	6	C	
T6	PL37A	6	T		T6	PL49A	6	T	
U5	PL37B	6	C		U5	PL49B	6	C	
U3	PL38A	6	T		U3	PL50A	6	T	
U4	PL38B	6	C		U4	PL50B	6	C	
V1	PL39A	6	T		V1	PL51A	6	T	
GND	GND6	6			GND	GND6	6		
V2	PL39B	6	C		V2	PL51B	6	C	
U7	TCK	6			U7	TCK	6		
V4	TDI	6			V4	TDI	6		
V5	TMS	6			V5	TMS	6		
V3	TDO	6			V3	TDO	6		
U6	VCCJ	6			U6	VCCJ	6		
W1	PL41A	6	T	LLM0_PLLT_IN_A	W1	PL53A	6	T	LLM0_PLLT_IN_A
W2	PL41B	6	C	LLM0_PLLC_IN_A	W2	PL53B	6	C	LLM0_PLLC_IN_A
V6	PL42A	6	T	LLM0_PLLT_FB_A	V6	PL54A	6	T	LLM0_PLLT_FB_A
W6	PL42B	6	C	LLM0_PLLC_FB_A	W6	PL54B	6	C	LLM0_PLLC_FB_A
Y1	PL43A	6	T		Y1	PL55A	6	T	
Y2	PL43B	6	C		Y2	PL55B	6	C	
W3	PL44A	6	T		W3	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W4	PL44B	6	C		W4	PL56B	6	C	
AA1	PL45A	6	T	LDQS45	AA1	PL57A	6	T	LDQS57
AB1	PL45B	6	C		AB1	PL57B	6	C	
Y4	PL46A	6	T		Y4	PL58A	6	T	
Y3	PL46B	6	C		Y3	PL58B	6	C	
AC1	PL47A	6	T		AC1	PL59A	6	T	
AB2	PL47B	6	C		AB2	PL59B	6	C	
AA2	NC	-			AA2	PL60A	6	T	
-	-	-			GND	GND6	6		
AA3	NC	-			AA3	PL60B	6	C	
W5	NC	-			W5	PL61A	6	T	
Y5	NC	-			Y5	PL61B	6	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K