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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	112
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (Tj)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-5qn208c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-5qn208c</a>

Figure 2-4. Slice Diagram

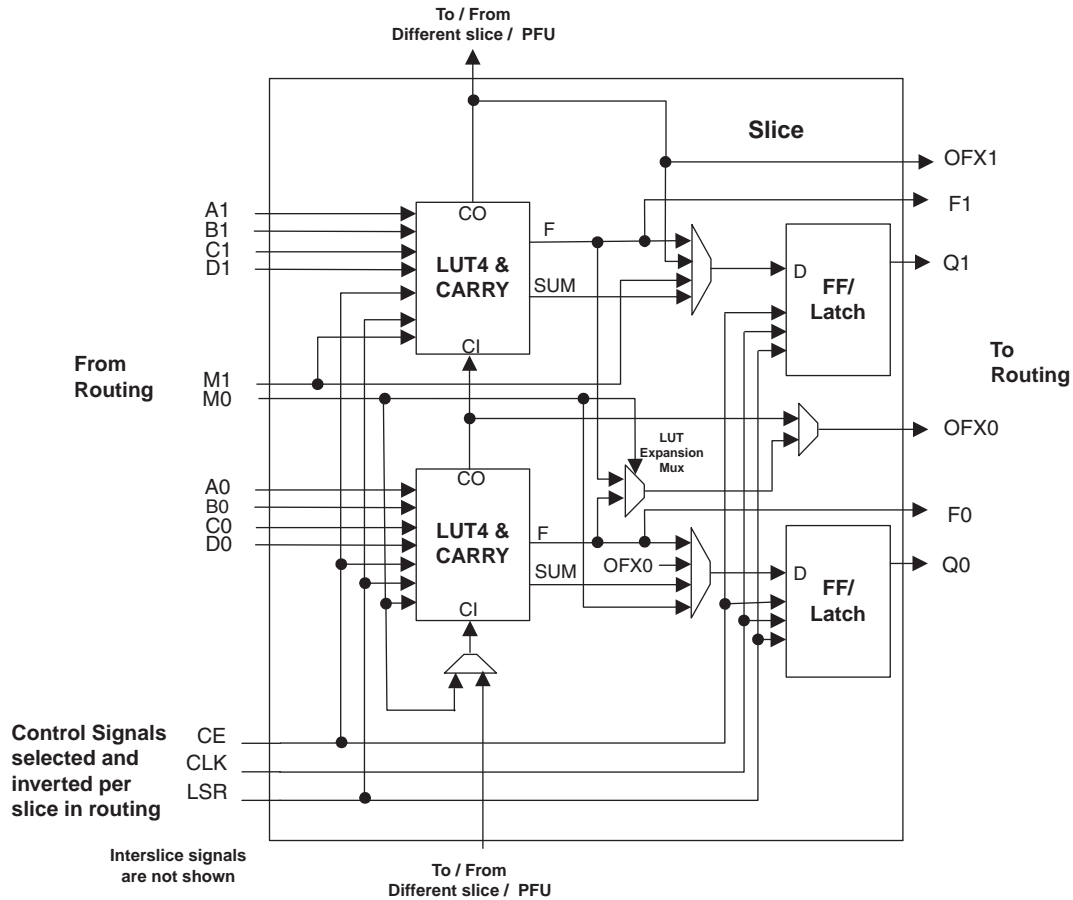


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In <sup>1</sup>
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output <sup>1</sup>

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

## Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

**Figure 2-7. Secondary Clock Sources**



## Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

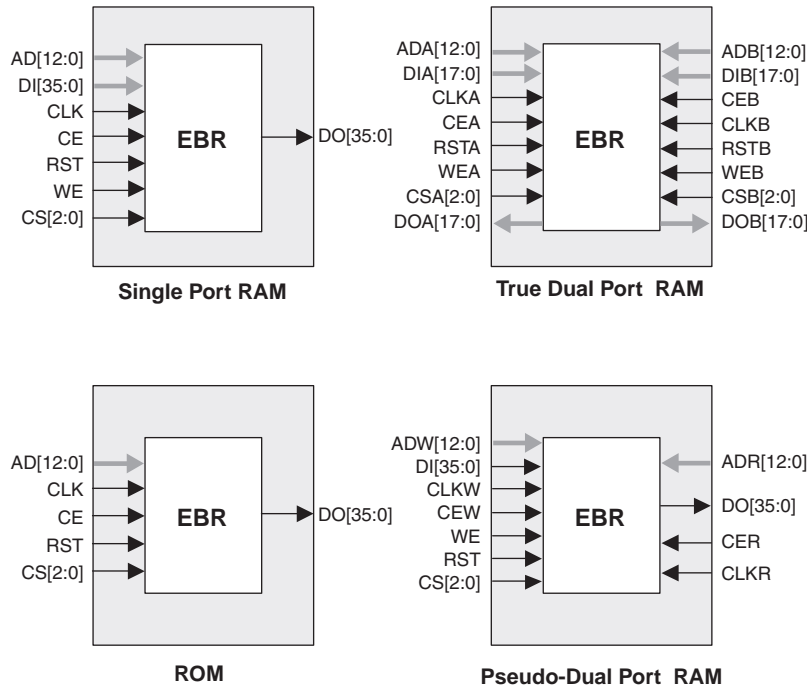
## Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

**Figure 2-15. sysMEM EBR Primitives**



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

**Initialization Supply Current<sup>1, 2, 3, 4, 5, 6</sup>**
**Over Recommended Operating Conditions**

Symbol	Parameter	Devices	Typ. <sup>6</sup>	Units
I <sub>CC</sub>	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFECP6/LFEC6	50	mA
		LFECP10/LFEC10	60	mA
		LFECP15/LFEC15	70	mA
		LFECP20/LFEC20	150	mA
		LFECP33/LFEC33	220	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFECP6/LFEC6	30	mA
		LFECP10/LFEC10	35	mA
		LFECP15/LFEC15	35	mA
		LFECP20/LFEC20	40	mA
		LFECP33/LFEC33	40	mA
I <sub>CCPLL</sub>	PLL Power Supply Current		12	mA
I <sub>CCIO</sub>	Bank Power Supply Current <sup>7</sup>	LFEC1	4	mA
		LFEC3	5	mA
		LFECP6/LFEC6	6	mA
		LFECP10/LFEC10	6	mA
		LFECP15/LFEC15	7	mA
		LFECP20/LFEC20	8	mA
		LFECP33/LFEC33	8	mA
I <sub>CCJ</sub>	V <sub>CCJ</sub> Power Supply Current		20	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.

4. Frequency 0MHz.

5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.

6. T<sub>J</sub>=25°C, power supplies at nominal voltage.

7. Per bank.

### BLVDS

The LatticeECP/EC devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

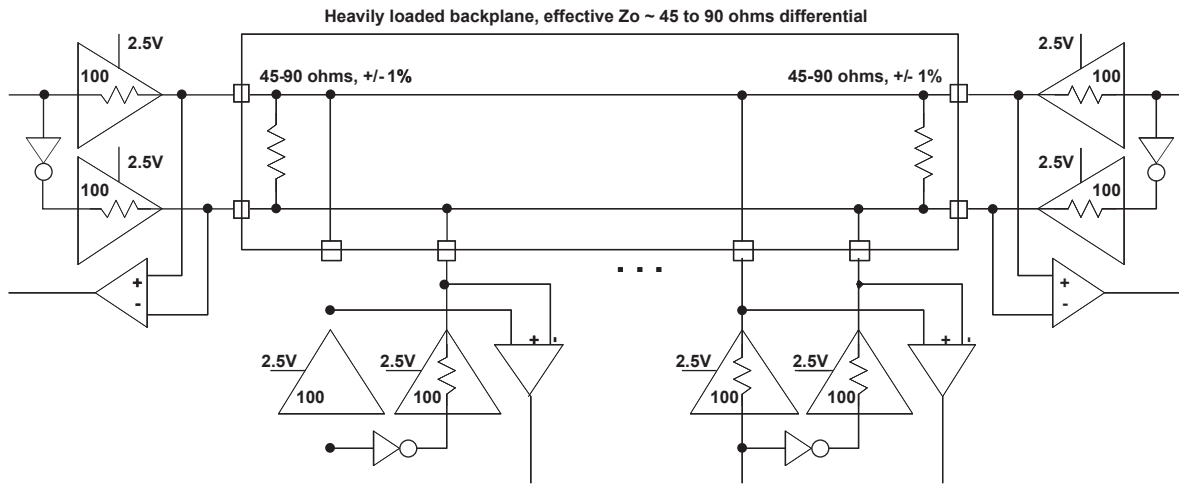


Table 3-2. BLVDS DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45	Zo = 90	
Z <sub>OUT</sub>	Output impedance	100	100	ohm
R <sub>TLEFT</sub>	Left end termination	45	90	ohm
R <sub>TRIGHT</sub>	Right end termination	45	90	ohm
V <sub>OH</sub>	Output high voltage	1.375	1.48	V
V <sub>OL</sub>	Output low voltage	1.125	1.02	V
V <sub>OD</sub>	Output differential voltage	0.25	0.46	V
V <sub>CM</sub>	Output common mode voltage	1.25	1.25	V
I <sub>DC</sub>	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

## Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics ( $\Theta_{JA}$ ), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables:  $T_J$  °C.

**Table 3-5. Delay Derating Table for Internal Blocks**

$T_J$ °C Commercial	$T_J$ °C Industrial	Power Supply Voltage		
		1.14V	1.2V	1.26V
—	-40	0.82	0.77	0.71
—	-25	0.82	0.76	0.71
0	20	0.89	0.83	0.78
25	45	0.93	0.87	0.81
85	105	1.00	0.94	0.89

## LatticeECP/EC Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>PFU/PFF Logic Mode Timing</b>								
t <sub>LUT4_PFU</sub>	LUT4 Delay (A to D Inputs to F Output)	—	0.25	—	0.31	—	0.36	ns
t <sub>LUT6_PFU</sub>	LUT6 Delay (A to D Inputs to OFX Output)	—	0.40	—	0.48	—	0.56	ns
t <sub>LSR_PFU</sub>	Set/Reset to Output of PFU	—	0.81	—	0.98	—	1.14	ns
t <sub>SUM_PFU</sub>	Clock to Mux (M0,M1) Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t <sub>HM_PFU</sub>	Clock to Mux (M0,M1) Input Hold Time	-0.05	—	-0.06	—	-0.06	—	ns
t <sub>SUD_PFU</sub>	Clock to D Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t <sub>HD_PFU</sub>	Clock to D Input Hold time	-0.03	—	-0.03	—	-0.04	—	ns
t <sub>CK2Q_PFU</sub>	Clock to Q Delay, D-type Register Configuration	—	0.36	—	0.44	—	0.51	ns
t <sub>LE2Q_PFU</sub>	Clock to Q Delay Latch Configuration	—	0.48	—	0.58	—	0.68	ns
t <sub>LD2Q_PFU</sub>	D to Q Throughput Delay when Latch is Enabled	—	0.50	—	0.60	—	0.69	ns
<b>PFU Dual Port Memory Mode Timing</b>								
t <sub>CORAM_PFU</sub>	Clock to Output	—	0.36	—	0.44	—	0.51	ns
t <sub>SUDATA_PFU</sub>	Data Setup Time	-0.20	—	-0.24	—	-0.28	—	ns
t <sub>HDATA_PFU</sub>	Data Hold Time	0.26	—	0.31	—	0.36	—	ns
t <sub>SUADDR_PFU</sub>	Address Setup Time	-0.51	—	-0.62	—	-0.72	—	ns
t <sub>HADDR_PFU</sub>	Address Hold Time	0.64	—	0.77	—	0.90	—	ns
t <sub>SUWREN_PFU</sub>	Write/Read Enable Setup Time	-0.24	—	-0.29	—	-0.34	—	ns
t <sub>HWREN_PFU</sub>	Write/Read Enable Hold Time	0.30	—	0.36	—	0.42	—	ns
<b>PIC Timing</b>								
<b>PIO Input/Output Buffer Timing</b>								
t <sub>IN_PIO</sub>	Input Buffer Delay	—	0.56	—	0.67	—	0.78	ns
t <sub>OUT_PIO</sub>	Output Buffer Delay	—	1.92	—	2.31	—	2.69	ns
<b>IOLOGIC Input/Output Timing</b>								
t <sub>SUI_PIO</sub>	Input Register Setup Time (Data Before Clock)	0.90	—	1.08	—	1.26	—	ns
t <sub>HI_PIO</sub>	Input Register Hold Time (Data after Clock)	0.62	—	0.74	—	0.87	—	ns
t <sub>COO_PIO</sub>	Output Register Clock to Output Delay	—	0.33	—	0.40	—	0.46	ns
t <sub>SUCE_PIO</sub>	Input Register Clock Enable Setup Time	-0.10	—	-0.12	—	-0.14	—	ns
t <sub>HCE_PIO</sub>	Input Register Clock Enable Hold Time	0.12	—	0.14	—	0.17	—	ns
t <sub>SULSR_PIO</sub>	Set/Reset Setup Time	0.18	—	0.21	—	0.25	—	ns
t <sub>HLSR_PIO</sub>	Set/Reset Hold Time	-0.15	—	-0.18	—	-0.21	—	ns
<b>EBR Timing</b>								
t <sub>CO_EBR</sub>	Clock to Output from Address or Data	—	3.64	—	4.37	—	5.10	ns
t <sub>COO_EBR</sub>	Clock to Output from EBR output Register	—	0.74	—	0.88	—	1.03	ns
t <sub>SUDATA_EBR</sub>	Setup Data to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t <sub>HDATA_EBR</sub>	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t <sub>SUADDR_EBR</sub>	Setup Address to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t <sub>HADDR_EBR</sub>	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t <sub>SUWREN_EBR</sub>	Setup Write/Read Enable to EBR Memory	-0.18	—	-0.22	—	-0.26	—	ns
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory	0.23	—	0.28	—	0.33	—	ns



**Signal Descriptions (Cont.)**

Signal Name	I/O	Description
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data out pin used to shift data out of device using 1149.1.
V <sub>CCJ</sub>	—	V <sub>CCJ</sub> - The power supply pin for JTAG Test Access Port.
<b>Configuration Pads (used during sysCONFIG)</b>		
CFG[2:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (Active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPIN	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes.

**Power Supply and NC Connections**

Signals	100 TQFP	144 TQFP	208 PQFP	256 fpBGA
VCC	12, 64	<b>EC1, EC3:</b> 13, 92, 99 <b>ECP/EC6:</b> 11, 13, 92, 99	<b>EC1, EC3:</b> 26, 128, 135 <b>ECP/EC6:</b> 24, 26, 128, 135 <b>ECP/EC10:</b> 5, 24, 26, 128, 135, 152	E12, E5, E8, M12, M5, M9, F6, F11, L11, L6
VCCIO0	100	136, 143	<b>EC1:</b> 187, 208 <b>EC3, ECP/EC6, ECP/EC10:</b> 187, 197, 208	F7, F8
VCCIO1	86	110, 125	157, 176	F9, F10
VCCIO2	73	108	<b>EC1:</b> 155 <b>EC3, ECP/EC6, ECP/EC10:</b> 145, 155	G11, H11
VCCIO3	56	73, 84	106, 120	J11, K11
VCCIO4	38	55, 71	85, 104	L9, L10
VCCIO5	26	38, 44	<b>EC1:</b> 53, 74 <b>EC2, ECP/EC6, ECP/EC10:</b> 53, 64, 74	L7, L8
VCCIO6	24	24, 36	37, 51	J6, K6
VCCIO7	2	1	<b>EC1:</b> 2 <b>EC3, ECP/EC6, ECP/EC10:</b> 2, 13	G6, H6
VCCJ	18	19	32	L4
VCCAUX	37, 87	54, 126	<b>EC1:</b> 84, 177 <b>EC3, ECP/EC6, ECP/EC10:</b> 22, 84, 136, 177	B15, R2
VCCPLL	—	—	—	—
GND, GND0-GND7	1, 14, 25, 35, 51, 68, 74, 89	<b>EC1, EC3:</b> 15, 28, 37, 52, 63, 72, 80, 96, 98, 109, 117, 128, 144 <b>ECP/EC6:</b> 12, 15, 28, 37, 52, 63, 72, 80, 96, 98, 109, 117, 128, 144	<b>EC1:</b> 1, 28, 41, 52, 82, 93, 105, 116, 132, 134, 156, 168, 179 <b>EC3:</b> 1, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 156, 168, 179, 189 <b>ECP/EC6:</b> 1, 18, 25, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 156, 168, 179, 189 <b>ECP/EC10:</b> 1, 6, 18, 25, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 151, 156, 168, 179, 189	A1, A16, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, T1, T16
NC	—	<b>EC1, EC3:</b> 11, 12 <b>ECP6/EC6:</b> None	<b>EC1:</b> 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 18, 22, 24, 25, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 72, 103, 136, 138, 144, 145, 146, 147, 148, 149, 150, 151, 152, 158, 189, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207 <b>EC3:</b> 5, 6, 18, 24, 25, 103, 151, 152, 158 <b>ECP/EC6:</b> 5, 6, 151, 152 <b>ECP/EC10:</b> None	<b>EC3:</b> G5, H5, F2, F1, H4, H3, G2, G1, J4, J3, J5, K5, H2, H1, J2, J1, R12, H16, H15, G16, G15, K12, J12, J14, J15, F16, F15, J13, H13, H14, G14, E16, E15, B13, C13 <b>ECP/EC10:</b> None <b>ECP/EC15:</b> None

**LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

**LFCEP/EC6, LFCEP/EC10 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFCEP6/LFCEC6				LFCEP10/LFCEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB18A	4	T	WRITEN	PB26A	4	T	WRITEN
87	PB18B	4	C	CS1N	PB26B	4	C	CS1N
88	PB19A	4	T	VREF1_4	PB27A	4	T	VREF1_4
89	PB19B	4	C	CSN	PB27B	4	C	CSN
90	PB20A	4	T	VREF2_4	PB28A	4	T	VREF2_4
91	PB20B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
92	PB21A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB21B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
95	PB22A	4	T	BDQS22	PB30A	4	T	BDQS30
96	PB22B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
97	PB23A	4	T		PB31A	4	T	
98	PB23B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
99	PB24A	4	T		PB32A	4	T	
100	PB24B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
101	PB25A	4	T		PB33A	4	T	
102	PB25B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
103	PB33A	4			PB41A	4		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR27B	3	C	VREF2_3	PR36B	3	C	VREF2_3
108	PR27A	3	T	VREF1_3	PR36A	3	T	VREF1_3
109	PR26B	3	C		PR35B	3	C	
110	PR26A	3	T		PR35A	3	T	
111	PR25B	3	C		PR34B	3	C	
112	PR25A	3	T		PR34A	3	T	
113	PR24B	3	C		PR33B	3	C	
114	PR24A	3	T	RDQS24	PR33A	3	T	RDQS33
115	PR23B	3	C	RLM0_PLLC_FB_A	PR32B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR23A	3	T	RLM0_PLLT_FB_A	PR32A	3	T	RLM0_PLLT_FB_A
118	PR22B	3	C	RLM0_PLLC_IN_A	PR31B	3	C	RLM0_PLLC_IN_A
119	PR22A	3	T	RLM0_PLLT_IN_A	PR31A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR21B	3	C	DI/CSSPIN	PR30B	3	C	DI/CSSPIN
122	PR21A	3	T	DOUT/CSON	PR30A	3	T	DOUT/CSON
123	PR20B	3	C	BUSY/SISPI	PR29B	3	C	BUSY/SISPI
124	PR20A	3	T	D7/SPID0	PR29A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

**LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA**

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:  
 484 fpBGA**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
C3	NC	-			C3	PL3A	7	T		C3	PL3A	7	T	
B2	NC	-			B2	PL3B	7	C		B2	PL3B	7	C	
E5	NC	-			E5	PL4A	7	T		E5	PL4A	7	T	
F5	NC	-			F5	PL4B	7	C		F5	PL4B	7	C	
D3	NC	-			D3	PL5A	7	T		D3	PL5A	7	T	
C2	NC	-			C2	PL5B	7	C		C2	PL5B	7	C	
F4	NC	-			F4	PL6A	7	T	LDQS6	F4	PL6A	7	T	LDQS6
G4	NC	-			G4	PL6B	7	C		G4	PL6B	7	C	
E3	NC	-			E3	PL7A	7	T		E3	PL7A	7	T	
D2	NC	-			D2	PL7B	7	C		D2	PL7B	7	C	
B1	NC	-			B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL8A	7	T	LUM0_PLLT_IN_A
C1	NC	-			C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL8B	7	C	LUM0_PLLC_IN_A
F3	NC	-			F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL9A	7	T	LUM0_PLLT_FB_A
GND	-	-			GND	GND7	7			GND	GND7	7		
E2	NC	-			E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL9B	7	C	LUM0_PLLC_FB_A
G5	NC	-			G5	NC	-			G5	PL11A	7	T	
H6	NC	-			H6	NC	-			H6	PL11B	7	C	
G3	NC	-			G3	NC	-			G3	PL12A	7	T	
H4	NC	-			H4	NC	-			H4	PL12B	7	C	
J5	NC	-			J5	NC	-			J5	PL13A	7	T	
H5	NC	-			H5	NC	-			H5	PL13B	7	C	
F2	NC	-			F2	NC	-			F2	PL14A	7	T	
GND	-	-			GND	-	-			GND	GND7	7		
F1	NC	-			F1	NC	-			F1	PL14B	7	C	
E1	NC	-			E1	PL11A	7	T		E1	PL15A	7	T	
D1	NC	-			D1	PL11B	7	C		D1	PL15B	7	C	
H3	PL3A	7	T		H3	PL12A	7	T		H3	PL16A	7	T	
G2	PL3B	7	C		G2	PL12B	7	C		G2	PL16B	7	C	
H2	PL4A	7	T		H2	PL13A	7	T		H2	PL17A	7	T	
G1	PL4B	7	C		G1	PL13B	7	C		G1	PL17B	7	C	
J4	PL5A	7	T		J4	PL14A	7	T		J4	PL18A	7	T	
GND	-	-			GND	GND7	7			GND	GND7	7		
J3	PL5B	7	C		J3	PL14B	7	C		J3	PL18B	7	C	
J2	PL6A	7	T	LDQS6	J2	PL15A	7	T	LDQS15	J2	PL19A	7	T	LDQS19
H1	PL6B	7	C		H1	PL15B	7	C		H1	PL19B	7	C	
K4	PL7A	7	T		K4	PL16A	7	T		K4	PL20A	7	T	
K5	PL7B	7	C		K5	PL16B	7	C		K5	PL20B	7	C	
K3	PL8A	7	T		K3	PL17A	7	T		K3	PL21A	7	T	
K2	PL8B	7	C		K2	PL17B	7	C		K2	PL21B	7	C	
J1	PL9A	7	T	PCLKT7_0	J1	PL18A	7	T	PCLKT7_0	J1	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7			GND	GND7	7		
K1	PL9B	7	C	PCLKC7_0	K1	PL18B	7	C	PCLKC7_0	K1	PL22B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6			L3	XRES	6		
L4	PL11A	6	T		L4	PL20A	6	T		L4	PL24A	6	T	
L5	PL11B	6	C		L5	PL20B	6	C		L5	PL24B	6	C	
L2	PL12A	6	T		L2	PL21A	6	T		L2	PL25A	6	T	
L1	PL12B	6	C		L1	PL21B	6	C		L1	PL25B	6	C	

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:  
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N13	GND	-			N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-			J7	VCC	-		
K16	VCC	-			K16	VCC	-			K16	VCC	-		
K17	VCC	-			K17	VCC	-			K17	VCC	-		
K6	VCC	-			K6	VCC	-			K6	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
L17	VCC	-			L17	VCC	-			L17	VCC	-		
L6	VCC	-			L6	VCC	-			L6	VCC	-		
M17	VCC	-			M17	VCC	-			M17	VCC	-		
M6	VCC	-			M6	VCC	-			M6	VCC	-		
N16	VCC	-			N16	VCC	-			N16	VCC	-		
N17	VCC	-			N17	VCC	-			N17	VCC	-		
N6	VCC	-			N6	VCC	-			N6	VCC	-		
N7	VCC	-			N7	VCC	-			N7	VCC	-		
P16	VCC	-			P16	VCC	-			P16	VCC	-		
P7	VCC	-			P7	VCC	-			P7	VCC	-		
G11	VCCIO0	0			G11	VCCIO0	0			G11	VCCIO0	0		
H10	VCCIO0	0			H10	VCCIO0	0			H10	VCCIO0	0		
H11	VCCIO0	0			H11	VCCIO0	0			H11	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0			H9	VCCIO0	0		
G12	VCCIO1	1			G12	VCCIO1	1			G12	VCCIO1	1		
H12	VCCIO1	1			H12	VCCIO1	1			H12	VCCIO1	1		
H13	VCCIO1	1			H13	VCCIO1	1			H13	VCCIO1	1		
H14	VCCIO1	1			H14	VCCIO1	1			H14	VCCIO1	1		
J15	VCCIO2	2			J15	VCCIO2	2			J15	VCCIO2	2		
K15	VCCIO2	2			K15	VCCIO2	2			K15	VCCIO2	2		
L15	VCCIO2	2			L15	VCCIO2	2			L15	VCCIO2	2		
L16	VCCIO2	2			L16	VCCIO2	2			L16	VCCIO2	2		
M15	VCCIO3	3			M15	VCCIO3	3			M15	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3			M16	VCCIO3	3		
N15	VCCIO3	3			N15	VCCIO3	3			N15	VCCIO3	3		
P15	VCCIO3	3			P15	VCCIO3	3			P15	VCCIO3	3		
R12	VCCIO4	4			R12	VCCIO4	4			R12	VCCIO4	4		
R13	VCCIO4	4			R13	VCCIO4	4			R13	VCCIO4	4		
R14	VCCIO4	4			R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4			T12	VCCIO4	4		
R10	VCCIO5	5			R10	VCCIO5	5			R10	VCCIO5	5		
R11	VCCIO5	5			R11	VCCIO5	5			R11	VCCIO5	5		
R9	VCCIO5	5			R9	VCCIO5	5			R9	VCCIO5	5		

**LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)**

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR17A	2	T	RUM0_PLLT_FB_A
G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR16B	2	C	RUM0_PLLC_IN_A
G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR16A	2	T	RUM0_PLLT_IN_A
F20	PR7B	2	C		F20	PR15B	2	C	
F19	PR7A	2	T		F19	PR15A	2	T	
E20	PR6B	2	C		E20	PR14B	2	C	
D20	PR6A	2	T	RDQS6	D20	PR14A	2	T	RDQS14
C21	PR5B	2	C		C21	PR13B	2	C	
GND	-	-			GND	GND2	2		
C20	PR5A	2	T		C20	PR13A	2	T	
F18	PR4B	2	C		F18	PR12B	2	C	
E18	PR4A	2	T		E18	PR12A	2	T	
B22	PR3B	2	C		B22	PR11B	2	C	
B21	PR3A	2	T		B21	PR11A	2	T	
GND	-	-			GND	GND2	2		
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
GND	-	-			GND	GND1	1		
G17	PT57B	1	C		G17	PT57B	1	C	
GND	-	-			GND	GND1	1		
F17	PT57A	1	T		F17	PT57A	1	T	
D18	PT56B	1	C		D18	PT56B	1	C	
C18	PT56A	1	T		C18	PT56A	1	T	
C19	PT55B	1	C		C19	PT55B	1	C	
B20	PT55A	1	T		B20	PT55A	1	T	
D17	PT54B	1	C		D17	PT54B	1	C	
C16	PT54A	1	T	TDQS54	C16	PT54A	1	T	TDQS54
B19	PT53B	1	C		B19	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
A20	PT53A	1	T		A20	PT53A	1	T	
E17	PT52B	1	C		E17	PT52B	1	C	
C17	PT52A	1	T		C17	PT52A	1	T	
F16	PT51B	1	C		F16	PT51B	1	C	
E16	PT51A	1	T		E16	PT51A	1	T	
F15	PT50B	1	C		F15	PT50B	1	C	
D16	PT50A	1	T		D16	PT50A	1	T	
B18	PT49B	1	C		B18	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
A19	PT49A	1	T		A19	PT49A	1	T	
B17	PT48B	1	C		B17	PT48B	1	C	
A18	PT48A	1	T		A18	PT48A	1	T	
B16	PT47B	1	C		B16	PT47B	1	C	



**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
P5	PL32B	6	C		P5	PL44B	6	C	
P6	PL33A	6	T		P6	PL45A	6	T	
R5	PL33B	6	C		R5	PL45B	6	C	
U1	PL34A	6	T		U1	PL46A	6	T	
U2	PL34B	6	C		U2	PL46B	6	C	
T3	PL35A	6	T		T3	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
T4	PL35B	6	C		T4	PL47B	6	C	
R6	PL36A	6	T	LDQS36	R6	PL48A	6	T	LDQS48
T5	PL36B	6	C		T5	PL48B	6	C	
T6	PL37A	6	T		T6	PL49A	6	T	
U5	PL37B	6	C		U5	PL49B	6	C	
U3	PL38A	6	T		U3	PL50A	6	T	
U4	PL38B	6	C		U4	PL50B	6	C	
V1	PL39A	6	T		V1	PL51A	6	T	
GND	GND6	6			GND	GND6	6		
V2	PL39B	6	C		V2	PL51B	6	C	
U7	TCK	6			U7	TCK	6		
V4	TDI	6			V4	TDI	6		
V5	TMS	6			V5	TMS	6		
V3	TDO	6			V3	TDO	6		
U6	VCCJ	6			U6	VCCJ	6		
W1	PL41A	6	T	LLM0_PLLT_IN_A	W1	PL53A	6	T	LLM0_PLLT_IN_A
W2	PL41B	6	C	LLM0_PLLC_IN_A	W2	PL53B	6	C	LLM0_PLLC_IN_A
V6	PL42A	6	T	LLM0_PLLT_FB_A	V6	PL54A	6	T	LLM0_PLLT_FB_A
W6	PL42B	6	C	LLM0_PLLC_FB_A	W6	PL54B	6	C	LLM0_PLLC_FB_A
Y1	PL43A	6	T		Y1	PL55A	6	T	
Y2	PL43B	6	C		Y2	PL55B	6	C	
W3	PL44A	6	T		W3	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W4	PL44B	6	C		W4	PL56B	6	C	
AA1	PL45A	6	T	LDQS45	AA1	PL57A	6	T	LDQS57
AB1	PL45B	6	C		AB1	PL57B	6	C	
Y4	PL46A	6	T		Y4	PL58A	6	T	
Y3	PL46B	6	C		Y3	PL58B	6	C	
AC1	PL47A	6	T		AC1	PL59A	6	T	
AB2	PL47B	6	C		AB2	PL59B	6	C	
AA2	NC	-			AA2	PL60A	6	T	
-	-	-			GND	GND6	6		
AA3	NC	-			AA3	PL60B	6	C	
W5	NC	-			W5	PL61A	6	T	
Y5	NC	-			Y5	PL61B	6	C	

**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y6	NC	-			Y6	PL62A	6	T	
W7	NC	-			W7	PL62B	6	C	
AA4	NC	-			AA4	PL63A	6	T	
AB3	NC	-			AB3	PL63B	6	C	
AC2	NC	-			AC2	PL64A	6	T	
-	-	-			GND	GND6	6		
AC3	NC	-			AC3	PL64B	6	C	
AA5	NC	-			AA5	PL65A	6	T	LDQS65
AB5	NC	-			AB5	PL65B	6	C	
AD3	NC	-			AD3	PL66A	6	T	
AD2	NC	-			AD2	PL66B	6	C	
AE1	NC	-			AE1	PL67A	6	T	
AD1	NC	-			AD1	PL67B	6	C	
AB4	PL48A	6	T	VREF1_6	AB4	PL68A	6	T	VREF1_6
AC4	PL48B	6	C	VREF2_6	AC4	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND5	5		
AB6	PB2A	5	T		AB6	PB2A	5	T	
AA6	PB2B	5	C		AA6	PB2B	5	C	
AC7	PB3A	5	T		AC7	PB3A	5	T	
Y8	PB3B	5	C		Y8	PB3B	5	C	
AB7	PB4A	5	T		AB7	PB4A	5	T	
AA7	PB4B	5	C		AA7	PB4B	5	C	
AC6	PB5A	5	T		AC6	PB5A	5	T	
AC5	PB5B	5	C		AC5	PB5B	5	C	
AB8	PB6A	5	T	BDQS6	AB8	PB6A	5	T	BDQS6
AC8	PB6B	5	C		AC8	PB6B	5	C	
AE2	PB7A	5	T		AE2	PB7A	5	T	
AA8	PB7B	5	C		AA8	PB7B	5	C	
AF2	PB8A	5	T		AF2	PB8A	5	T	
Y9	PB8B	5	C		Y9	PB8B	5	C	
AD5	PB9A	5	T		AD5	PB9A	5	T	
GND	GND5	5			GND	GND5	5		
AD4	PB9B	5	C		AD4	PB9B	5	C	
AD8	PB10A	5	T		AD8	PB10A	5	T	
AC9	PB10B	5	C		AC9	PB10B	5	C	
AE3	PB11A	5	T		AE3	PB11A	5	T	
AB9	PB11B	5	C		AB9	PB11B	5	C	
AF3	PB12A	5	T		AF3	PB12A	5	T	
AD9	PB12B	5	C		AD9	PB12B	5	C	
AE4	PB13A	5	T		AE4	PB13A	5	T	
GND	GND5	5			GND	GND5	5		

**LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)**

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

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**LatticeECP Industrial (Continued)**

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFCEP20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFCEP20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFCEP20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672I	496	-3	fpBGA	672	IND	32.8K
LFCEP33E-4F672I	496	-4	fpBGA	672	IND	32.8K
LFCEP33E-3F484I	360	-3	fpBGA	484	IND	32.8K
LFCEP33E-4F484I	360	-4	fpBGA	484	IND	32.8K

**LatticeECP Commercial**

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K