Lattice Semiconductor Corporation - LFEC1E-5TN144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1500
Total RAM Bits	18432
Number of I/O	97
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec1e-5tn144c

LatticeECP/EC Family Data Sheet Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

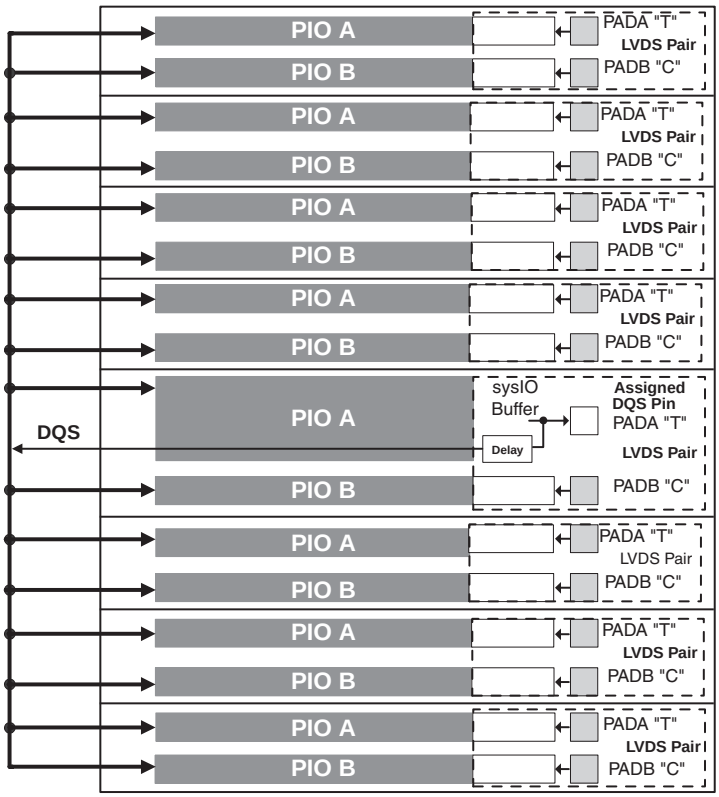
Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

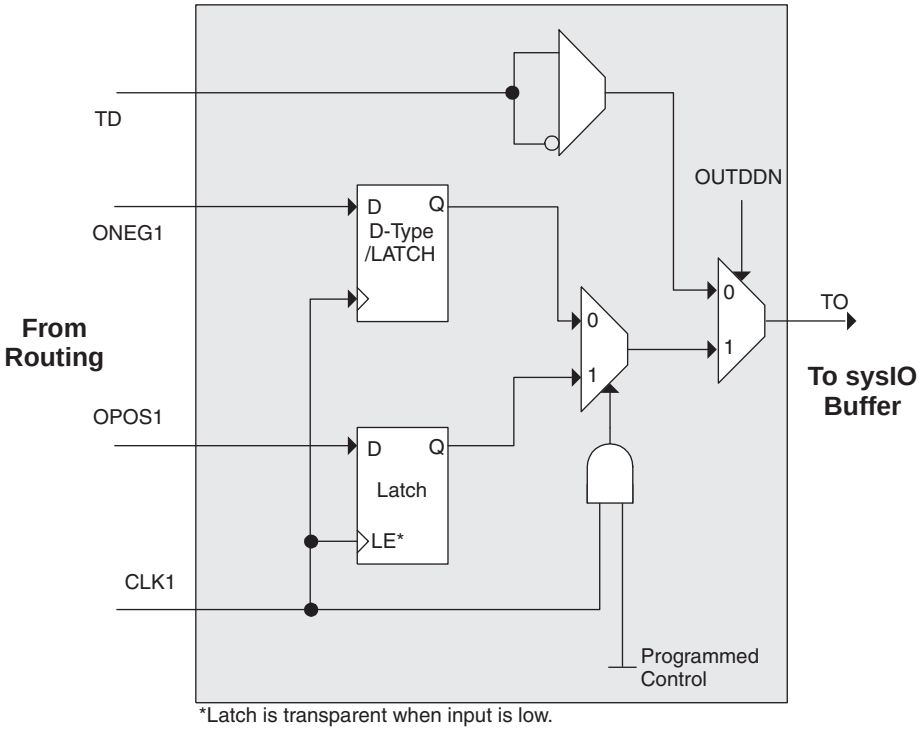
Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Figure 2-31. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeECP/EC family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysI/O Buffer Banks

LatticeECP/EC devices have eight sysI/O buffer banks; each is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-34 shows the eight banks and their associated supplies.

In the LatticeECP/EC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO.}$ LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold input independent of $V_{CCIO.}$ In addition to the bank V_{CCIO} supplies, the LatticeECP/EC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeECP/EC devices, some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

LatticeECP/EC Family Data Sheet DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

Dedicated Input Voltage Applied[4] . . . . . -0.5 to 4.25V

I/O Tristate Voltage Applied [4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temp. (Tj) . . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[3]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage for ECP/EC33	1.14	1.26	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.140	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.140	3.465	V
t_{JCOM}	Junction Commercial Operation	0	85	°C
t_{JIND}	Junction Industrial Operation	-40	100	°C

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCAUX} ramp rate must not exceed 3mV/µs for commercial and 0.6 mV/µs for industrial device operations during power up when transitioning between 0.8V and 1.8V.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Top and Bottom General Purpose sysI/Os (Banks 0, 1, 4 and 5), JTAG and Dedicated sysCONFIG Pins						
I_{DK_TB}	Input or I/O Leakage Current	0 ð V_{IN} ð V_{IH} (MAX.)	—	—	+/-1000	µA
Left and Right General Purpose sysI/Os (Banks 2, 3, 6 and 7)						
I_{DK_LR}	Input or I/O Leakage Current	V_{IN} ð V_{CCIO}	—	—	+/-1000	µA
		V_{IN} > V_{CCIO}	—	35	—	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. 0 ð V_{CC} ð V_{CC} (MAX), 0 ð V_{CCIO} ð V_{CCIO} (MAX) or 0 ð V_{CCAUX} ð V_{CCAUX} (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.

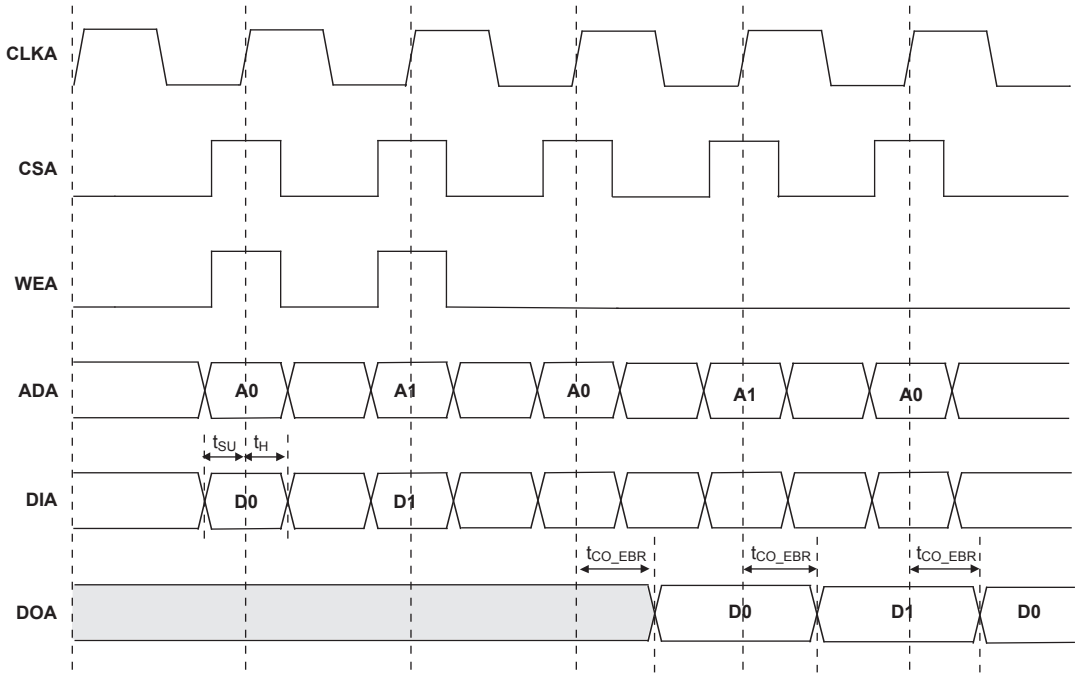
sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

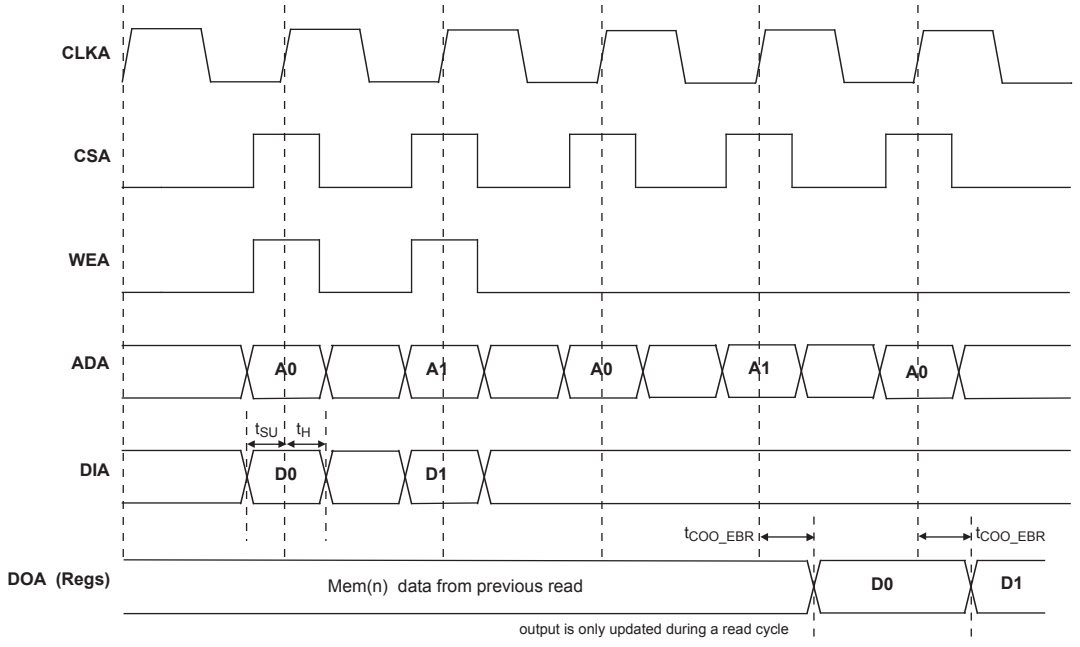
EBR Memory Timing Diagrams

Figure 3-8. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-9. Read/Write Mode with Input and Output Registers



LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

Pin Information Summary

Pin Type		LFEC1			LFEC3				LFECP6/EC6				LFECP/EC10		
		100-TQFP	144-TQFP	208-PQFP	100-TQFP	144-TQFP	208-PQFP	256-fpBGA	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	208-PQFP	256-fpBGA	484-fpBGA
Single Ended User I/O		67	97	112	67	97	145	160	97	147	195	224	147	195	288
Differential Pair User I/O		29	46	56	29	46	72	80	46	72	97	112	72	97	144
Configuration	Dedicated	13	13	13	13	13	13	13	13	13	13	13	13	13	13
	Muxed	48	48	48	48	48	48	48	48	48	48	48	56	56	56
TAP		5	5	5	5	5	5	5	5	5	5	5	5	5	5
Dedicated (total without supplies)		80	110	160	80	110	160	208	110	160	208	373	160	208	373
V_{CC}		2	3	3	2	3	3	10	4	4	10	20	6	10	20
V_{CCAUX}		2	2	2	4	4	4	4	2	4	2	12	4	2	12
V_{CCPLL}		0	0	0	0	0	0	0	0	0	0	0	0	0	0
V_{CCIO}	Bank0	1	2	2	1	2	3	2	2	3	2	4	3	2	4
	Bank1	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank2	1	1	1	2	2	2	2	1	2	2	4	2	2	4
	Bank3	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank4	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank5	1	2	2	1	2	2	2	2	3	2	4	3	2	4
	Bank6	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank7	1	1	1	2	2	2	2	1	2	2	4	2	2	4
GND, GND0-GND7		8	13	13	8	13	16	20	14	18	20	44	20	20	44
NC		0	2	51	0	2	9	35	0	4	0	139	0	0	75
Single Ended/ Differential I/O Pair per Bank	Bank 0	11/5	14/7	16/8	11/5	14/7	26/13	32/16	14/7	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 1	11/5	13/6	16/8	11/5	13/6	16/8	16/8	13/6	17/8	18/9	32/16	17/8	18/9	32/16
	Bank 2	3/1	8/4	8/4	3/1	8/4	14/7	16/8	8/4	14/7	16/8	16/8	14/7	16/8	32/16
	Bank 3	8/4	13/6	16/8	8/4	13/6	16/8	16/8	13/6	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 4	12/4	14/6	16/8	12/4	14/6	16/8	16/8	14/6	17/8	17/8	32/16	17/8	17/8	32/16
	Bank 5	9/4	13/6	16/8	9/4	13/6	26/13	32/16	13/6	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 6	5/2	14/7	16/8	5/2	14/7	16/8	16/8	14/7	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 7	8/4	8/4	8/4	8/4	8/4	15/7	16/8	8/4	15/7	16/8	16/8	15/7	16/8	32/16
V_{CCJ}		1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
169	PT13A	1	T		PT21A	1	T	
170	PT12B	1	C		PT20B	1	C	
171	PT12A	1	T		PT20A	1	T	
172	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
173	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
174	PT10B	1	C		PT18B	1	C	
175	PT10A	1	T		PT18A	1	T	
176	VCCIO1	1			VCCIO1	1		
177	VCCAUX	-			VCCAUX	-		
178	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
179	GND0	0			GND0	0		
180	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
181	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
182	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
183	PT7B	0	C		PT15B	0	C	
184	PT7A	0	T		PT15A	0	T	
185	PT6B	0	C		PT14B	0	C	
186	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
187	VCCIO0	0			VCCIO0	0		
188	PT5B	0	C		PT13B	0	C	
189	NC	-			GND0	0		
190	PT5A	0	T		PT13A	0	T	
191	PT4B	0	C		PT12B	0	C	
192	PT4A	0	T		PT12A	0	T	
193	PT3B	0	C		PT11B	0	C	
194	PT3A	0	T		PT11A	0	T	
195	PT2B	0	C		PT10B	0	C	
196	PT2A	0	T		PT10A	0	T	
197	NC	-			VCCIO0	0		
198	NC	-			PT6B	0	C	
199	NC	-			PT6A	0	T	TDQS6
200	NC	-			PT5B	0	C	
201	NC	-			PT5A	0	T	
202	NC	-			PT4B	0	C	
203	NC	-			PT4A	0	T	
204	NC	-			PT3B	0	C	
205	NC	-			PT3A	0	T	
206	NC	-			PT2B	0	C	
207	NC	-			PT2A	0	T	
208	VCCIO0	0			VCCIO0	0		

* Double bonded to the pin.

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
V12	PB16B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5
AB10	PB17A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB11	PB17B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0
Y12	PB18A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN
U11	PB18B	4	C	CS1N	U11	PB26B	4	C	CS1N	U11	PB26B	4	C	CS1N
W12	PB19A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4
U12	PB19B	4	C	CSN	U12	PB27B	4	C	CSN	U12	PB27B	4	C	CSN
W13	PB20A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4
U13	PB20B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7
AA12	PB21A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB12	PB21B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6
T13	PB22A	4	T	BDQS22	T13	PB30A	4	T	BDQS30	T13	PB30A	4	T	BDQS30
V13	PB22B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4
W14	PB23A	4	T		W14	PB31A	4	T		W14	PB31A	4	T	
U14	PB23B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3
Y13	PB24A	4	T		Y13	PB32A	4	T		Y13	PB32A	4	T	
V14	PB24B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2
AA13	PB25A	4	T		AA13	PB33A	4	T		AA13	PB33A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB13	PB25B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1
AA14	PB26A	4	T		AA14	PB34A	4	T		AA14	PB34A	4	T	
Y14	PB26B	4	C		Y14	PB34B	4	C		Y14	PB34B	4	C	
Y15	PB27A	4	T		Y15	PB35A	4	T		Y15	PB35A	4	T	
W15	PB27B	4	C		W15	PB35B	4	C		W15	PB35B	4	C	
V15	PB28A	4	T		V15	PB36A	4	T		V15	PB36A	4	T	
T14	PB28B	4	C		T14	PB36B	4	C		T14	PB36B	4	C	
AB14	PB29A	4	T		AB14	PB37A	4	T		AB14	PB37A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB15	PB29B	4	C		AB15	PB37B	4	C		AB15	PB37B	4	C	
AB16	PB30A	4	T	BDQS30	AB16	PB38A	4	T	BDQS38	AB16	PB38A	4	T	BDQS38
AA15	PB30B	4	C		AA15	PB38B	4	C		AA15	PB38B	4	C	
AB17	PB31A	4	T		AB17	PB39A	4	T		AB17	PB39A	4	T	
AA16	PB31B	4	C		AA16	PB39B	4	C		AA16	PB39B	4	C	
AB18	PB32A	4	T		AB18	PB40A	4	T		AB18	PB40A	4	T	
AA17	PB32B	4	C		AA17	PB40B	4	C		AA17	PB40B	4	C	
AB19	PB33A	4	T		AB19	PB41A	4	T		AB19	PB41A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA18	PB33B	4	C		AA18	PB41B	4	C		AA18	PB41B	4	C	
W16	NC	-			W16	NC	-			W16	PB42A	4	T	
U15	NC	-			U15	NC	-			U15	PB42B	4	C	
V16	NC	-			V16	NC	-			V16	PB43A	4	T	
U16	NC	-			U16	NC	-			U16	PB43B	4	C	
Y17	NC	-			Y17	NC	-			Y17	PB44A	4	T	
V17	NC	-			V17	NC	-			V17	PB44B	4	C	
AB20	NC	-			AB20	NC	-			AB20	PB45A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA19	NC	-			AA19	NC	-			AA19	PB45B	4	C	
Y16	NC	-			Y16	NC	-			Y16	PB46A	4	T	BDQS46

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
GND	-	-			GND	GND7	7		
C3	PL3A	7	T		C3	PL10A	7	T	
B2	PL3B	7	C		B2	PL10B	7	C	
E5	PL4A	7	T		E5	PL11A	7	T	
F5	PL4B	7	C		F5	PL11B	7	C	
D3	PL5A	7	T		D3	PL12A	7	T	
C2	PL5B	7	C		C2	PL12B	7	C	
GND	-	-			GND	GND7	7		
F4	PL6A	7	T	LDQS6	F4	PL14A	7	T	LDQS14
G4	PL6B	7	C		G4	PL14B	7	C	
E3	PL7A	7	T		E3	PL15A	7	T	
D2	PL7B	7	C		D2	PL15B	7	C	
B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL16A	7	T	LUM0_PLLT_IN_A
C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL16B	7	C	LUM0_PLLC_IN_A
F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL17B	7	C	LUM0_PLLC_FB_A
GND	-	-			GND	GND7	7		
G5	PL11A	7	T		G5	PL23A	7	T	LDQS23
H6	PL11B	7	C		H6	PL23B	7	C	
G3	PL12A	7	T		G3	PL24A	7	T	
H4	PL12B	7	C		H4	PL24B	7	C	
J5	PL13A	7	T		J5	PL25A	7	T	
H5	PL13B	7	C		H5	PL25B	7	C	
F2	PL14A	7	T		F2	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
F1	PL14B	7	C		F1	PL26B	7	C	
E1	PL15A	7	T		E1	PL27A	7	T	
D1	PL15B	7	C		D1	PL27B	7	C	
H3	PL16A	7	T		H3	PL28A	7	T	
G2	PL16B	7	C		G2	PL28B	7	C	
H2	PL17A	7	T		H2	PL29A	7	T	
G1	PL17B	7	C		G1	PL29B	7	C	
J4	PL18A	7	T		J4	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
J3	PL18B	7	C		J3	PL30B	7	C	
J2	PL19A	7	T	LDQS19	J2	PL31A	7	T	LDQS31
H1	PL19B	7	C		H1	PL31B	7	C	
K4	PL20A	7	T		K4	PL32A	7	T	
K5	PL20B	7	C		K5	PL32B	7	C	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K16	VCC	-			K16	VCC	-		
K17	VCC	-			K17	VCC	-		
K6	VCC	-			K6	VCC	-		
K7	VCC	-			K7	VCC	-		
L17	VCC	-			L17	VCC	-		
L6	VCC	-			L6	VCC	-		
M17	VCC	-			M17	VCC	-		
M6	VCC	-			M6	VCC	-		
N16	VCC	-			N16	VCC	-		
N17	VCC	-			N17	VCC	-		
N6	VCC	-			N6	VCC	-		
N7	VCC	-			N7	VCC	-		
P16	VCC	-			P16	VCC	-		
P7	VCC	-			P7	VCC	-		
G11	VCCIO0	0			G11	VCCIO0	0		
H10	VCCIO0	0			H10	VCCIO0	0		
H11	VCCIO0	0			H11	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0		
G12	VCCIO1	1			G12	VCCIO1	1		
H12	VCCIO1	1			H12	VCCIO1	1		
H13	VCCIO1	1			H13	VCCIO1	1		
H14	VCCIO1	1			H14	VCCIO1	1		
J15	VCCIO2	2			J15	VCCIO2	2		
K15	VCCIO2	2			K15	VCCIO2	2		
L15	VCCIO2	2			L15	VCCIO2	2		
L16	VCCIO2	2			L16	VCCIO2	2		
M15	VCCIO3	3			M15	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3		
N15	VCCIO3	3			N15	VCCIO3	3		
P15	VCCIO3	3			P15	VCCIO3	3		
R12	VCCIO4	4			R12	VCCIO4	4		
R13	VCCIO4	4			R13	VCCIO4	4		
R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4		
R10	VCCIO5	5			R10	VCCIO5	5		
R11	VCCIO5	5			R11	VCCIO5	5		
R9	VCCIO5	5			R9	VCCIO5	5		
T11	VCCIO5	5			T11	VCCIO5	5		
M7	VCCIO6	6			M7	VCCIO6	6		
M8	VCCIO6	6			M8	VCCIO6	6		
N8	VCCIO6	6			N8	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6		
J8	VCCIO7	7			J8	VCCIO7	7		
K8	VCCIO7	7			K8	VCCIO7	7		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
L24	PR17A	2	T		L24	PR29A	2	T	
K25	PR16B	2	C		K25	PR28B	2	C	
J25	PR16A	2	T		J25	PR28A	2	T	
J26	PR15B	2	C		J26	PR27B	2	C	
H26	PR15A	2	T		H26	PR27A	2	T	
H25	PR14B	2	C		H25	PR26B	2	C	
GND	GND2	2			GND	GND2	2		
J24	PR14A	2	T		J24	PR26A	2	T	
K21	PR13B	2	C		K21	PR25B	2	C	
K22	PR13A	2	T		K22	PR25A	2	T	
K20	PR12B	2	C		K20	PR24B	2	C	
J20	PR12A	2	T		J20	PR24A	2	T	
K23	PR11B	2	C		K23	PR23B	2	C	
K24	PR11A	2	T		K24	PR23A	2	T	RDQS23
J21	NC	-			J21	PR22B	2	C	
-	-	-			GND	GND2	2		
J22	NC	-			J22	PR22A	2	T	
J23	NC	-			J23	PR21B	2	C	
H22	NC	-			H22	PR21A	2	T	
G26	NC	-			G26	PR20B	2	C	
F26	NC	-			F26	PR20A	2	T	
E26	NC	-			E26	PR19B	2	C	
E25	NC	-			E25	PR19A	2	T	
F25	PR9B	2	C	RUM0_PLLC_FB_A	F25	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
G25	PR9A	2	T	RUM0_PLLT_FB_A	G25	PR17A	2	T	RUM0_PLLT_FB_A
H23	PR8B	2	C	RUM0_PLLC_IN_A	H23	PR16B	2	C	RUM0_PLLC_IN_A
H24	PR8A	2	T	RUM0_PLLT_IN_A	H24	PR16A	2	T	RUM0_PLLT_IN_A
H21	PR7B	2	C		H21	PR15B	2	C	
G21	PR7A	2	T		G21	PR15A	2	T	
D26	PR6B	2	C		D26	PR14B	2	C	
D25	PR6A	2	T	RDQS6	D25	PR14A	2	T	RDQS14
F21	PR5B	2	C		F21	PR13B	2	C	
-	-	-			GND	GND2	2		
G22	PR5A	2	T		G22	PR13A	2	T	
G24	PR4B	2	C		G24	PR12B	2	C	
G23	PR4A	2	T		G23	PR12A	2	T	
C26	PR3B	2	C		C26	PR11B	2	C	
C25	PR3A	2	T		C25	PR11A	2	T	
F24	NC	-			F24	PR9B	2	C	
-	-	-			GND	GND2	2		
F23	NC	-			F23	PR9A	2	T	

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFEC10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFEC10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFEC10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFEC10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFEC15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFEC15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFEC15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFEC15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFEC15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFEC20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFEC20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFEC20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFEC20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFEC20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFEC33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFEC33E-5F672C	496	-5	fpBGA	672	COM	32.8K
LFEC33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFEC33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFEC33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeECP/EC Family Data Sheet Revision History

Revision History

Date	Version	Section	Change Summary
June 2004	01.0	—	Initial release.
August 2004	01.1	Introduction	Added new device LFECP/LFEC33 in Table 1-1.
		Architecture	Added New device LFECP/LFEC33 in Tables 2-9, 2-10 and 2-11.
		DC & Switching Characteristics	Added New device LFECP/LFEC33 on Supply current (Standby) tables.
			Added New device LFECP/LFEC33 on Initialization Supply current tables.
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section.
			Added EC33, ECP33 device: Industrial and Commercial to Part Number table.
			Corrected I/O counts in the part number tables for 100/144 TQFP and 208 PQFP packages to match Table 1-1 on page 1.
November 2004	01.3	Introduction	Changed DDR333 (166MHz) to DDR400 (200MHz)
			Added “RSDS” offering to the Features list: Flexible I/O Buffer
		Architecture	Added information about Secondary Clock Sources
			Added information about DCS
			Added a section on “Recommended Power-up Sequence”
			Updated Figure 2-24 “DQS Routing”
			Added DSP Block performance numbers to Table 2-11
			Added another row for RSDS in Table 2-13 and Table 2-14
		DC & Switching Characteristics	Updated new timing numbers
			Added numbers to derating table
			Added DC conditions to RSDS table
			Changed LVDS Max. V_{CCIO} to 2.625
			Added a row for RSDS in “Operating Condition” table
			Updated standby and initialization current table
			Added figure 3-12: sysConfig SPI port sequence
			Added DDR Timing Table and DDR Timings Figure 3-6
		Pinout Information	Added LFECP/EC6 to Pin Information
			Added LFECP/EC6 to Power Supply and NC Connections
			Added LFECP/EC6 144 TQFP Logic Signal Connections
			Added LFECP/EC6 208 PQFP Logic Signal Connections
			Added LFECP/EC6 256 fpBGA Logic Signal Connections
			Added LFECP/EC6 484 fpBGA Logic Signal Connections
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section.
			Added Part Number table for Commercial EC33.
			Added Part Number table for Commercial ECP33.
			Added Part Number table for Industrial EC33.
			Added Part Number table for Industrial ECP33.

Date	Version	Section	Change Summary
September 2005	02.0	Architecture	sysIO section has been updated.
		DC & Switching Characteristics	Recommended Operating Conditions has been updated with V_{CCPLL}.
			DC Electrical Characteristics table has been updated
			Removed 5V Tolerant Input Buffer section.
			Register-to-Register performance table has been updated (rev. G 0.28).
			LatticeECP/EC External Switching Characteristics table has been updated (rev. G 0.28).
			LatticeECP/EC Internal Switching Characteristics table has been updated (rev. G 0.28).
			LatticeECP/EC Family Timing Adders have been updated (rev. G 0.28).
			sysCLOCK PLL timing table has been updated (rev. G 0.28)
			LatticeECP/EC sysCONFIG Port Timing specification table has been updated (rev. G 0.28).
			Master Clock table has been updated (rev. G 0.28).
			JTAG Port Timing specification table has been updated (rev. G 0.28).
		Pinout Information	Signal Description table has been updated with V_{CCPLL}.
November 2005	02.1	DC & Switching Characteristics	Pin-to-Pin Performance table has been updated (G 0.30) - 4:1MUX, 8:1MUX, 16:1MUX, 32:1MUX Register-to-Register Performance (G 0.30) - No timing number changes.
			External Switching Characteristics (G 0.30) - No timing number changes.
			Internal Switching Characteristics (G 0.30) -t_{SUP_DSP}, t_{HP_DSP}, t_{SUO_DSP}, t_{HO_DSP}, t_{COI_DSP}, t_{COD_DSP} numbers have been updated.
			Family Timing Adders (G 0.30) - No timing number changes.
			sysCLOCK PLL Timing (G 0.30) - No timing number changes.
			sysCONFIG Port Timing Specifications (G 0.30) - No timing number changes.
			Master Clock (G 0.30) - No timing number changes.
			JTAG Port Timing Specification (G 0.30) - No timing number changes.
		Ordering Information	Added 208-PQFP lead-free part numbers.
March 2006	02.2	DC & Switching Characteristics	Added footnote 3. to V_{CCAUX} in the Recommended Operating Conditions table.
January 2007	02.3	Architecture	EBR Asynchronous Reset section added.
February 2007	02.4	Architecture	Updated EBR Asynchronous Reset section.
			Updated Maximum Number of Elements in a Block table - MAC value for x9 changed to 2.
May 2007	02.5	Architecture	Updated text in Ripple Mode section.
November 2007	02.6	DC & Switching Characteristics	Added JTAG Port Waveforms diagram.
			Updated t_{RST} timing information in the sysCLOCK PLL Timing table.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
February 2008	02.7	DC & Switching Characteristics	Read/Write Mode (Normal) and Read/Write Mode with Input and Output Registers waveforms in the EBR Memory Timing Diagrams section have been updated.
September 2012	02.8	All	Updated document with new corporate logo.