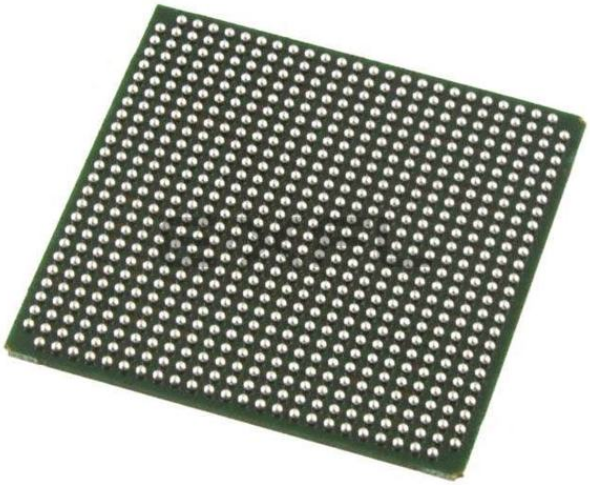

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 19700 |
| Total RAM Bits | 434176 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec20e-3fn672c |

*Table 2-5. PLL Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | "1" to reset PLL |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (No phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | "1" indicates PLL LOCK to CLKI |
| DDAMODE | I | Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static) |
| DDAIZR | I | Dynamic Delay Zero. "1": delay = 0, "0": delay = on |
| DDAILAG | I | Dynamic Delay Lag/Lead. "1": Lead, "0": Lag |
| DDAIDEL[2:0] | I | Dynamic Delay Input |
| DDAOZR | O | Dynamic Delay Zero Output |
| DDAOLAG | O | Dynamic Delay Lag/Lead Output |
| DDAODEL[2:0] | O | Dynamic Delay Output |

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

## Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

*Figure 2-13. DCS Block Primitive*

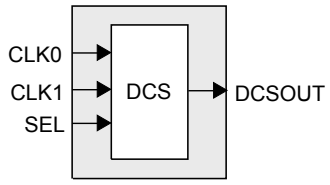
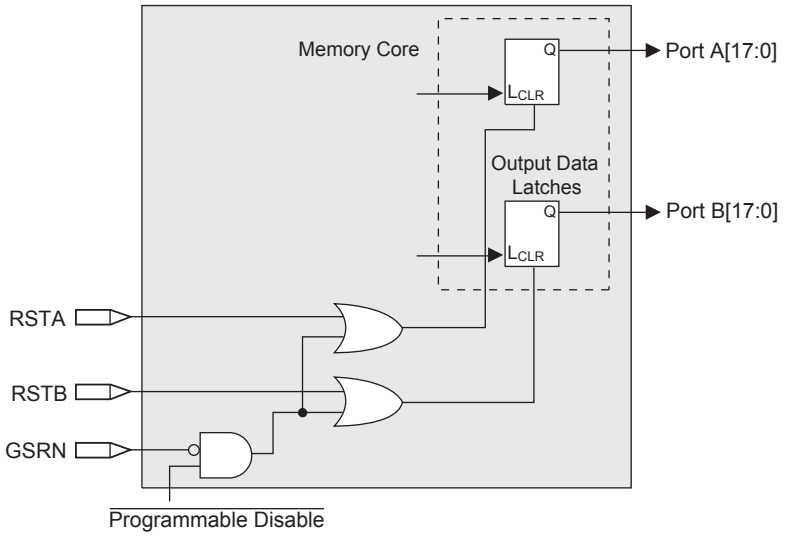



Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

*Figure 2-16. Memory Core Reset*

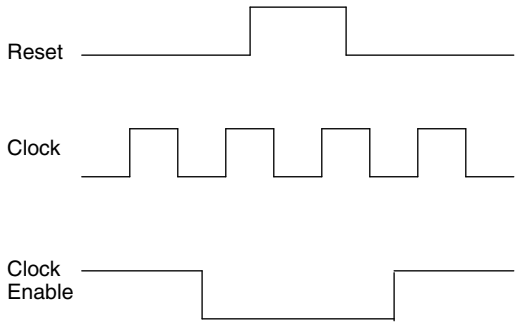



For further information about sysMEM EBR block, please see the the list of technical documentation at the end of this data sheet.

## EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-17. The GSR input to the EBR is always asynchronous.

*Figure 2-17. EBR Asynchronous Reset (Including GSR) Timing Diagram*




If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

# sysDSP Block

The LatticeECP-DSP family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and

*Table 2-7. Maximum Number of Elements in a Block*

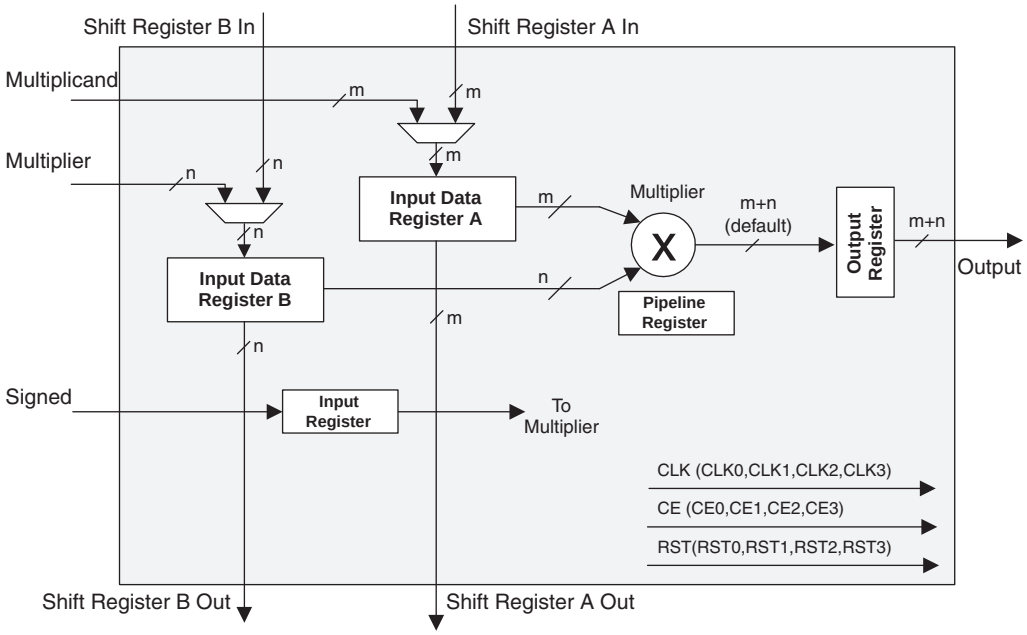
| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADD | 4 | 2 | — |
| MULTADDSUM | 2 | 1 | — |

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift registers from previous operand registers. In addition by selecting “dynamic operation” in the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle. Similarly by selecting ‘Dynamic operation’ in the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.

## MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-19 shows the MULT sysDSP element.

*Figure 2-19. MULT sysDSP Element*




## MAC sysDSP Element

In this case the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-20 shows the MAC sysDSP element.

## Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

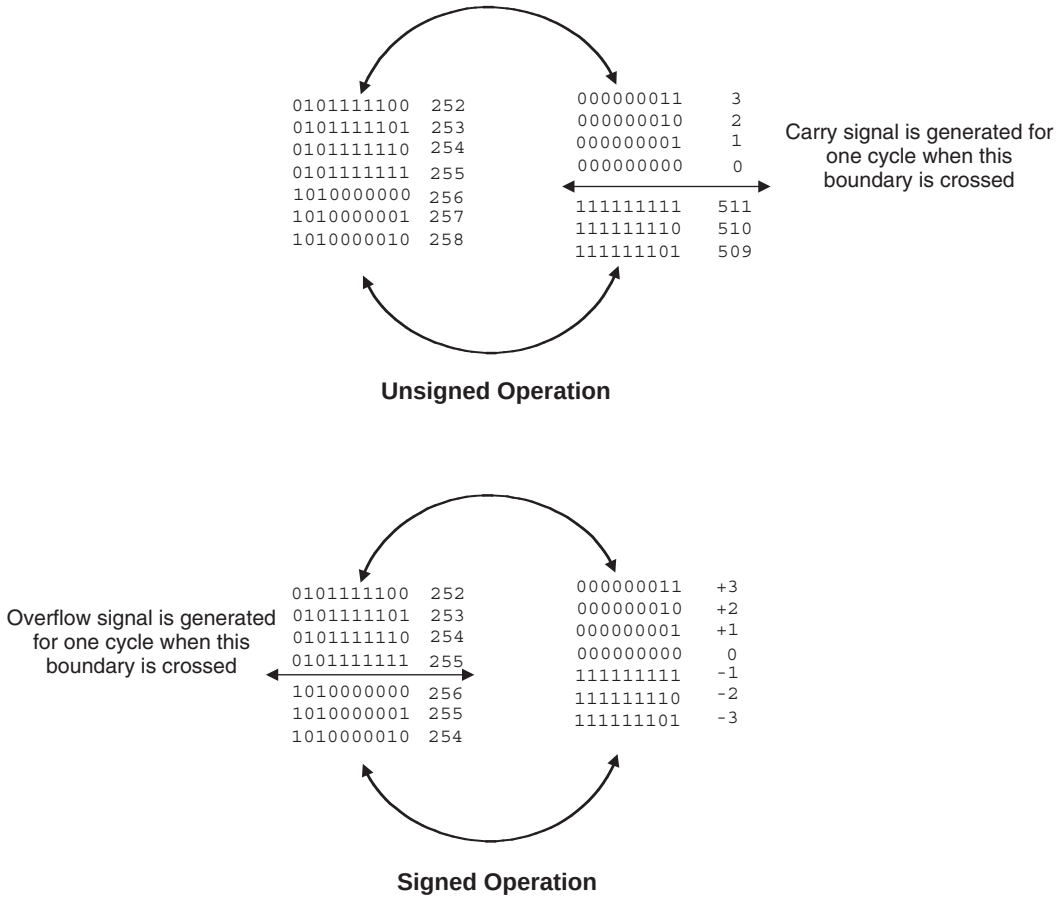
***Table 2-8. An Example of Sign Extension***

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9-Bits | Two's Complement Signed 18-bits |
|---|---|---|---|---|---|---|
| +5 | 0101 | 000000101 | 000000000000000101 | 0101 | 000000101 | 000000000000000101 |
| -6 | 0110 | 000000110 | 000000000000000110 | 1010 | 111111010 | 111111111111111010 |

## OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number then accumulator roll over is said to occur and overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-23.

***Figure 2-23. Accumulator Overflow/Underflow Conditions***

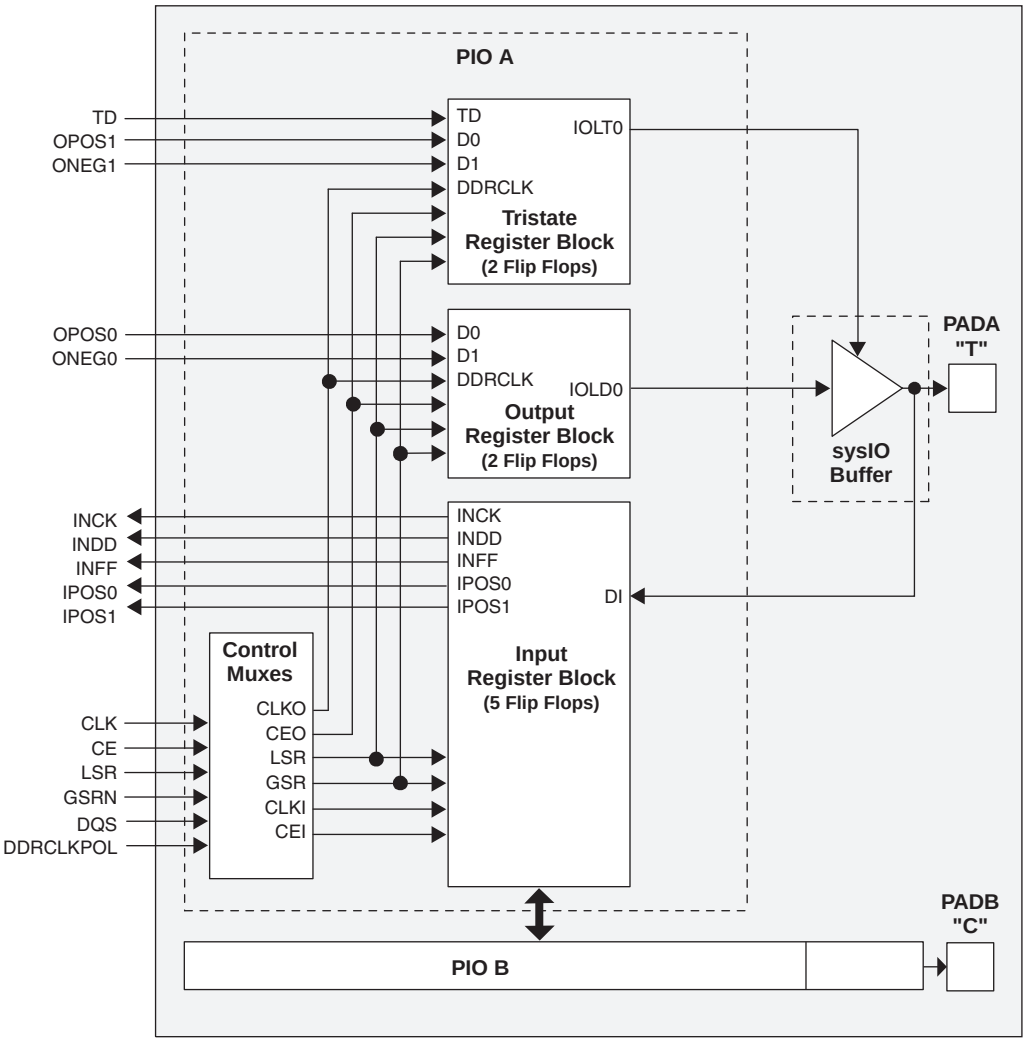


For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

## Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

***Figure 2-24. PIC Diagram***




Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

*Figure 2-27. Input Register DDR Waveforms*

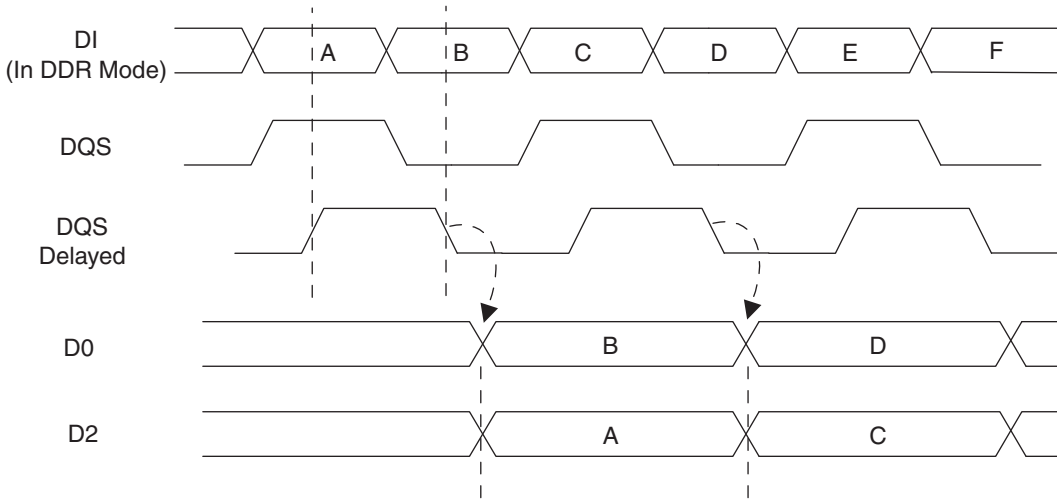
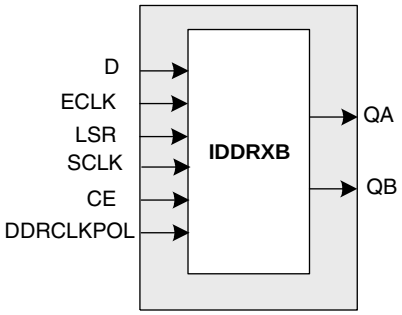



*Figure 2-28. INDDRXB Primitive*




**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

## Supply Current (Standby)[1, 2, 3, 4]

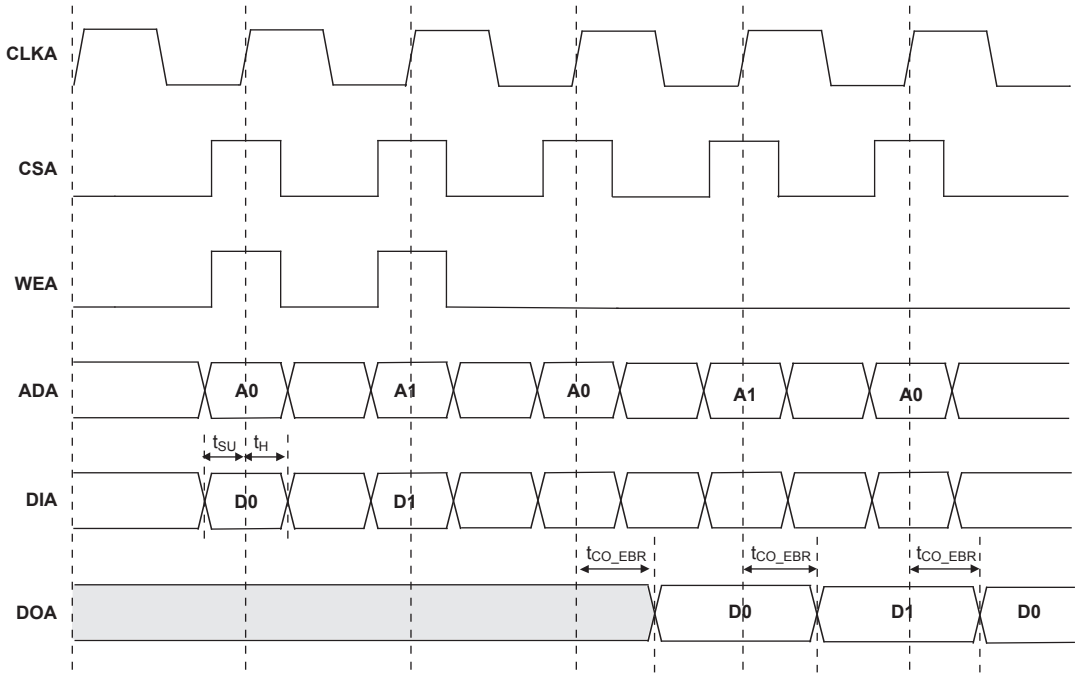
**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | LFEC1 | 6 | mA |
| | | LFEC3 | 10 | mA |
| | | LFECP6/LFEC6 | 15 | mA |
| | | LFECP10/LFEC10 | 25 | mA |
| | | LFECP15/LFEC15 | 35 | mA |
| | | LFECP20/LFEC20 | 60 | mA |
| | | LFECP33/LFEC33 | 85 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | | 15 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current | | 5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current[6] | | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply Current | | 5 | mA |

1. For further information about supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$=25ºC, power supplies at nominal voltage.
6. Per bank.

## EBR Memory Timing Diagrams

***Figure 3-8. Read/Write Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-9. Read/Write Mode with Input and Output Registers***

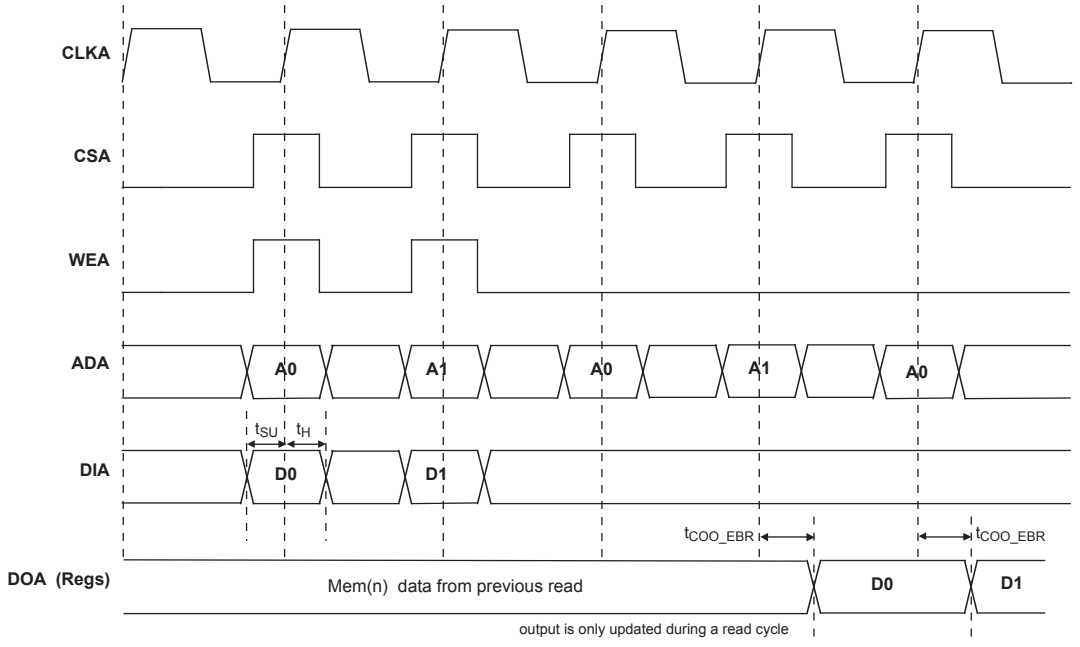
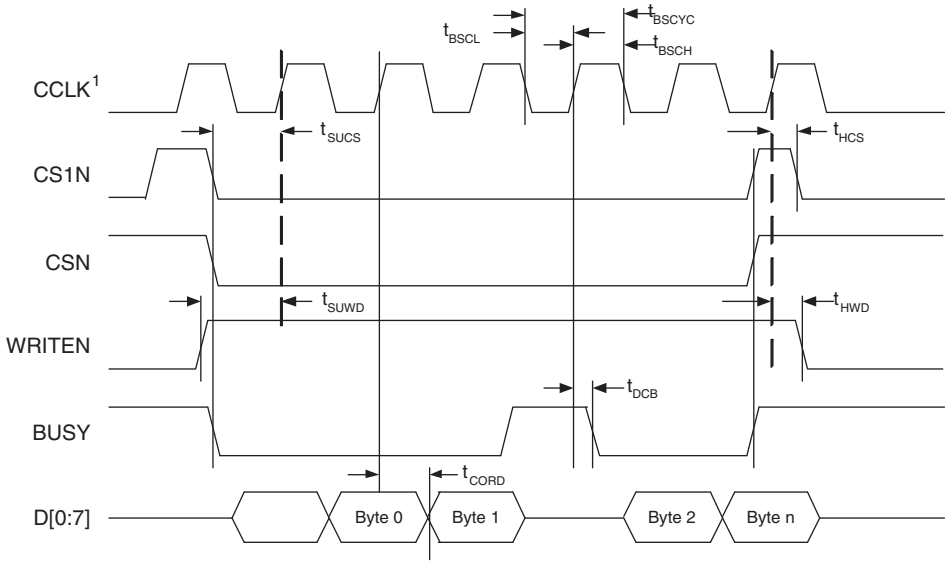
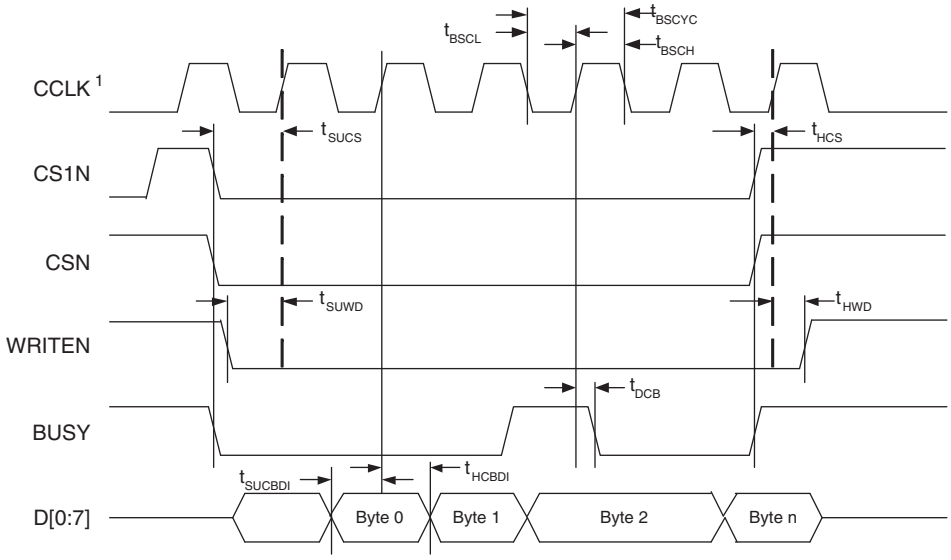


*Figure 3-12. sysCONFIG Parallel Port Read Cycle*




1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

*Figure 3-13. sysCONFIG Parallel Port Write Cycle*




1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

*Figure 3-14. sysCONFIG Master Serial Port Timing*

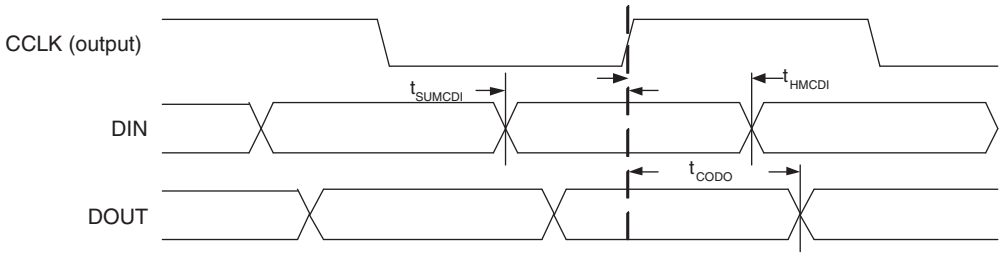



*Figure 3-15. sysCONFIG Slave Serial Port Timing*

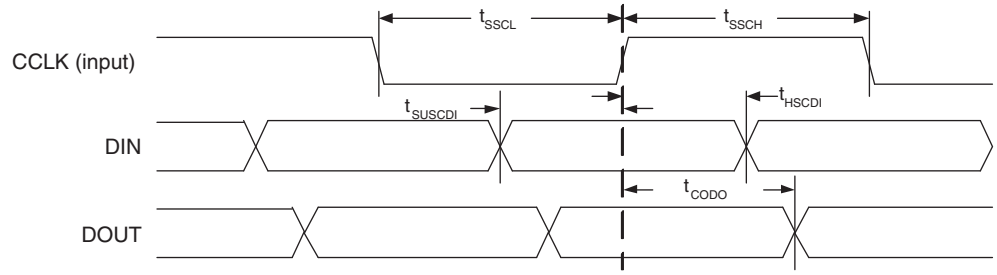
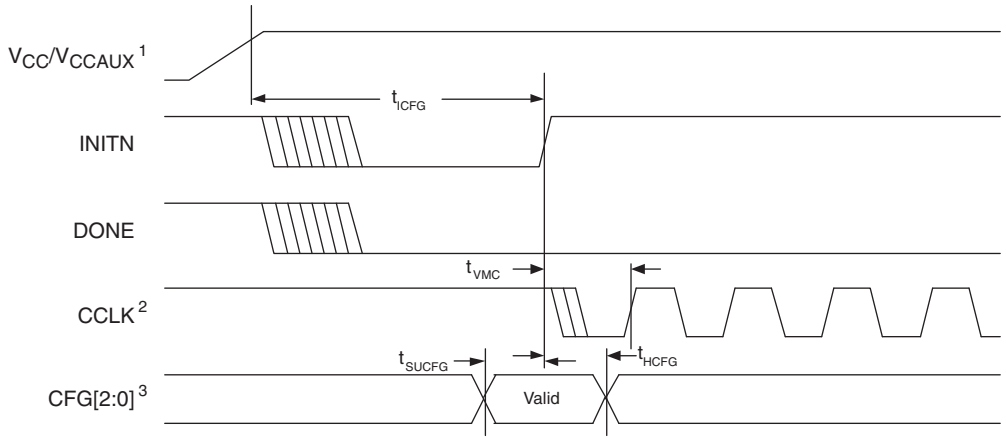



*Figure 3-16. Power-On-Reset (POR) Timing*




1. Time taken from $V_{CC}$ or $V_{CCAUX}$, whichever is the last to reach its $V_{MIN}$.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |
| TDO | O | Output pin. Test Data out pin used to shift data out of device using 1149.1. |
| $V_{CCJ}$ | — | $V_{CCJ}$ - The power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (used during sysCONFIG) | | |
| CFG[2:0] | I | Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY/SISPI | I/O | Read control command in SPI3 or SPIX mode. |
| CSN | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. |
| CS1N | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. |
| WRITEN | I | Write Data on Parallel port (Active low). |
| D[7:0]/SPID[0:7] | I/O | sysCONFIG Port Data I/O. |
| DOUT/CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. |
| DI/CSSPIN | I/O | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes. |

## LFEC1, LFEC3 Logic Signal Connections: 100 TQFP

| Pin Number | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 1* | GND0 GND7 | - | | | GND0 GND7 | - | | |
| 2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 3 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 |
| 4 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 |
| 5 | PL3A | 7 | T | | PL7A | 7 | T | |
| 6 | PL3B | 7 | C | | PL7B | 7 | C | |
| 7 | PL4A | 7 | T | | PL8A | 7 | T | |
| 8 | PL4B | 7 | C | | PL8B | 7 | C | |
| 9 | PL5A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 |
| 10 | PL5B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 |
| 11 | XRES | 6 | | | XRES | 6 | | |
| 12 | VCC | - | | | VCC | - | | |
| 13 | TCK | 6 | | | TCK | 6 | | |
| 14 | GND | - | | | GND | - | | |
| 15 | TDI | 6 | | | TDI | 6 | | |
| 16 | TMS | 6 | | | TMS | 6 | | |
| 17 | TDO | 6 | | | TDO | 6 | | |
| 18 | VCCJ | 6 | | | VCCJ | 6 | | |
| 19 | PL7A | 6 | T | LLM0_PLLT_IN_A | PL11A | 6 | T | LUM0_PLLT_IN_A |
| 20 | PL7B | 6 | C | LLM0_PLLC_IN_A | PL11B | 6 | C | LUM0_PLLC_IN_A |
| 21 | PL8A | 6 | T | LLM0_PLLT_FB_A | PL12A | 6 | T | LUM0_PLLT_FB_A |
| 22 | PL8B | 6 | C | LLM0_PLLC_FB_A | PL12B | 6 | C | LUM0_PLLC_FB_A |
| 23 | PL14A | 6 | | VREF1_6 | PL18A | 6 | | VREF1_6 |
| 24 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 25* | GND5 GND6 | - | | | GND5 GND6 | - | | |
| 26 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 27 | PB2A | 5 | T | | PB10A | 5 | T | |
| 28 | PB2B | 5 | C | | PB10B | 5 | C | |
| 29 | PB3A | 5 | T | | PB11A | 5 | T | |
| 30 | PB3B | 5 | C | | PB11B | 5 | C | |
| 31 | PB6A | 5 | | BDQS6 | PB14A | 5 | | BDQS14 |
| 32 | PB8A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 |
| 33 | PB8B | 5 | C | VREF1_5 | PB16B | 5 | C | VREF1_5 |
| 34 | PB9A | 5 | T | PCLKT5_0 | PB17A | 5 | T | PCLKT5_0 |
| 35 | GND5 | 5 | | | GND5 | 5 | | |
| 36 | PB9B | 5 | C | PCLKC5_0 | PB17B | 5 | C | PCLKC5_0 |
| 37 | VCCAUX | - | | | VCCAUX | - | | |
| 38 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 39 | PB10A | 4 | T | WRITEN | PB18A | 4 | T | WRITEN |
| 40 | PB10B | 4 | C | CS1N | PB18B | 4 | C | CS1N |

# LFEC1, LFEC3, LFECP/EC6 Logic Signal Connections: 144 TQFP

| Pin Number | LFEC1 | | | | LFEC3 | | | | LFECP6/EC6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 1 | VCCIO7 | 7 | | | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 2 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 |
| 3 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 |
| 4 | PL3A | 7 | T | | PL7A | 7 | T | | PL7A | 7 | T | |
| 5 | PL3B | 7 | C | | PL7B | 7 | C | | PL7B | 7 | C | |
| 6 | PL4A | 7 | T | | PL8A | 7 | T | | PL8A | 7 | T | |
| 7 | PL4B | 7 | C | | PL8B | 7 | C | | PL8B | 7 | C | |
| 8 | PL5A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 |
| 9 | PL5B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 |
| 10 | XRES | 6 | | | XRES | 6 | | | XRES | 6 | | |
| 11 | NC | - | | | NC | - | | | VCC | - | | |
| 12 | NC | - | | | NC | - | | | GND | - | | |
| 13 | VCC | - | | | VCC | - | | | VCC | - | | |
| 14 | TCK | 6 | | | TCK | 6 | | | TCK | 6 | | |
| 15 | GND | - | | | GND | - | | | GND | - | | |
| 16 | TDI | 6 | | | TDI | 6 | | | TDI | 6 | | |
| 17 | TMS | 6 | | | TMS | 6 | | | TMS | 6 | | |
| 18 | TDO | 6 | | | TDO | 6 | | | TDO | 6 | | |
| 19 | VCCJ | 6 | | | VCCJ | 6 | | | VCCJ | 6 | | |
| 20 | PL7A | 6 | T | LLM0_PLLT_IN_A | PL11A | 6 | T | LLM0_PLLT_IN_A | PL20A | 6 | T | LLM0_PLLT_IN_A |
| 21 | PL7B | 6 | C | LLM0_PLLC_IN_A | PL11B | 6 | C | LLM0_PLLC_IN_A | PL20B | 6 | C | LLM0_PLLC_IN_A |
| 22 | PL8A | 6 | T | LLM0_PLLT_FB_A | PL12A | 6 | T | LLM0_PLLT_FB_A | PL21A | 6 | T | LLM0_PLLT_FB_A |
| 23 | PL8B | 6 | C | LLM0_PLLC_FB_A | PL12B | 6 | C | LLM0_PLLC_FB_A | PL21B | 6 | C | LLM0_PLLC_FB_A |
| 24 | VCCIO6 | 6 | | | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 25 | PL9A | 6 | T | | PL13A | 6 | T | | PL22A | 6 | T | |
| 26 | PL9B | 6 | C | | PL13B | 6 | C | | PL22B | 6 | C | |
| 27 | PL10A | 6 | T | | PL14A | 6 | T | | PL23A | 6 | T | |
| 28 | GND6 | 6 | | | GND6 | 6 | | | GND6 | 6 | | |
| 29 | PL10B | 6 | C | | PL14B | 6 | C | | PL23B | 6 | C | |
| 30 | PL11A | 6 | T | LDQS11 | PL15A | 6 | T | LDQS15 | PL24A | 6 | T | LDQS24 |
| 31 | PL11B | 6 | C | | PL15B | 6 | C | | PL24B | 6 | C | |
| 32 | PL12A | 6 | T | | PL16A | 6 | T | | PL25A | 6 | T | |
| 33 | PL12B | 6 | C | | PL16B | 6 | C | | PL25B | 6 | C | |
| 34 | PL14A | 6 | T | VREF1_6 | PL18A | 6 | T | VREF1_6 | PL27A | 6 | T | VREF1_6 |
| 35 | PL14B | 6 | C | VREF2_6 | PL18B | 6 | C | VREF2_6 | PL27B | 6 | C | VREF2_6 |
| 36 | VCCIO6 | 6 | | | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 37* | GND5 GND6 | - | | | GND5 GND6 | - | | | GND5 GND6 | - | | |
| 38 | VCCIO5 | 5 | | | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 39 | PB2A | 5 | T | | PB10A | 5 | T | | PB10A | 5 | T | |
| 40 | PB2B | 5 | C | | PB10B | 5 | C | | PB10B | 5 | C | |
| 41 | PB3A | 5 | T | | PB11A | 5 | T | | PB11A | 5 | T | |
| 42 | PB3B | 5 | C | | PB11B | 5 | C | | PB11B | 5 | C | |
| 43 | PB5B | 5 | | | PB13B | 5 | | | PB13B | 5 | | |
| 44 | VCCIO5 | 5 | | | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 45 | PB6A | 5 | T | BDQS6 | PB14A | 5 | T | BDQS14 | PB14A | 5 | T | BDQS14 |
| 46 | PB6B | 5 | C | | PB14B | 5 | C | | PB14B | 5 | C | |
| 47 | PB7A | 5 | T | | PB15A | 5 | T | | PB15A | 5 | T | |
| 48 | PB7B | 5 | C | | PB15B | 5 | C | | PB15B | 5 | C | |
| 49 | PB8A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 |

## LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 43 | PL11A | 6 | T | LDQS11 | PL15A | 6 | T | LDQS15 |
| 44 | PL11B | 6 | C | | PL15B | 6 | C | |
| 45 | PL12A | 6 | T | | PL16A | 6 | T | |
| 46 | PL12B | 6 | C | | PL16B | 6 | C | |
| 47 | PL13A | 6 | T | | PL17A | 6 | T | |
| 48 | PL13B | 6 | C | | PL17B | 6 | C | |
| 49 | PL14A | 6 | T | VREF1_6 | PL18A | 6 | T | VREF1_6 |
| 50 | PL14B | 6 | C | VREF2_6 | PL18B | 6 | C | VREF2_6 |
| 51 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 52* | GND5<br>GND6 | - | | | GND5<br>GND6 | - | | |
| 53 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 54 | NC | - | | | PB2A | 5 | T | |
| 55 | NC | - | | | PB2B | 5 | C | |
| 56 | NC | - | | | PB3A | 5 | T | |
| 57 | NC | - | | | PB3B | 5 | C | |
| 58 | NC | - | | | PB4A | 5 | T | |
| 59 | NC | - | | | PB4B | 5 | C | |
| 60 | NC | - | | | PB5A | 5 | T | |
| 61 | NC | - | | | PB5B | 5 | C | |
| 62 | NC | - | | | PB6A | 5 | T | BDQS6 |
| 63 | NC | - | | | PB6B | 5 | C | |
| 64 | NC | - | | | VCCIO5 | 5 | | |
| 65 | PB2A | 5 | T | | PB10A | 5 | T | |
| 66 | PB2B | 5 | C | | PB10B | 5 | C | |
| 67 | PB3A | 5 | T | | PB11A | 5 | T | |
| 68 | PB3B | 5 | C | | PB11B | 5 | C | |
| 69 | PB4A | 5 | T | | PB12A | 5 | T | |
| 70 | PB4B | 5 | C | | PB12B | 5 | C | |
| 71 | PB5A | 5 | T | | PB13A | 5 | T | |
| 72 | NC | - | | | GND5 | 5 | | |
| 73 | PB5B | 5 | C | | PB13B | 5 | C | |
| 74 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 75 | PB6A | 5 | T | BDQS6 | PB14A | 5 | T | BDQS14 |
| 76 | PB6B | 5 | C | | PB14B | 5 | C | |
| 77 | PB7A | 5 | T | | PB15A | 5 | T | |
| 78 | PB7B | 5 | C | | PB15B | 5 | C | |
| 79 | PB8A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 |
| 80 | PB8B | 5 | C | VREF1_5 | PB16B | 5 | C | VREF1_5 |
| 81 | PB9A | 5 | T | PCLKT5_0 | PB17A | 5 | T | PCLKT5_0 |
| 82 | GND5 | 5 | | | GND5 | 5 | | |
| 83 | PB9B | 5 | C | PCLKC5_0 | PB17B | 5 | C | PCLKC5_0 |
| 84 | VCCAUX | - | | | VCCAUX | - | | |

## LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFEC3 | | | | LFECP6/LFEC6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | LVDS | Dual Function | Ball Function | Bank | LVDS | Dual Function |
| D7 | PT11B | 0 | C | | PT11B | 0 | C | |
| C7 | PT11A | 0 | T | | PT11A | 0 | T | |
| A7 | PT10B | 0 | C | | PT10B | 0 | C | |
| A6 | PT10A | 0 | T | | PT10A | 0 | T | |
| E7 | PT9B | 0 | C | | PT9B | 0 | C | |
| GND | GND0 | 0 | | | GND0 | 0 | | |
| E6 | PT9A | 0 | T | | PT9A | 0 | T | |
| D6 | PT8B | 0 | C | | PT8B | 0 | C | |
| C6 | PT8A | 0 | T | | PT8A | 0 | T | |
| B6 | PT7B | 0 | C | | PT7B | 0 | C | |
| B5 | PT7A | 0 | T | | PT7A | 0 | T | |
| A5 | PT6B | 0 | C | | PT6B | 0 | C | |
| A4 | PT6A | 0 | T | TDQS6 | PT6A | 0 | T | TDQS6 |
| A3 | PT5B | 0 | C | | PT5B | 0 | C | |
| A2 | PT5A | 0 | T | | PT5A | 0 | T | |
| B2 | PT4B | 0 | C | | PT4B | 0 | C | |
| B3 | PT4A | 0 | T | | PT4A | 0 | T | |
| D5 | PT3B | 0 | C | | PT3B | 0 | C | |
| C5 | PT3A | 0 | T | | PT3A | 0 | T | |
| C4 | PT2B | 0 | C | | PT2B | 0 | C | |
| B4 | PT2A | 0 | T | | PT2A | 0 | T | |
| GND | GND0 | 0 | | | GND0 | 0 | | |
| A1 | GND | - | | | GND | - | | |
| A16 | GND | - | | | GND | - | | |
| G10 | GND | - | | | GND | - | | |
| G7 | GND | - | | | GND | - | | |
| G8 | GND | - | | | GND | - | | |
| G9 | GND | - | | | GND | - | | |
| H10 | GND | - | | | GND | - | | |
| H7 | GND | - | | | GND | - | | |
| H8 | GND | - | | | GND | - | | |
| H9 | GND | - | | | GND | - | | |
| J10 | GND | - | | | GND | - | | |
| J7 | GND | - | | | GND | - | | |
| J8 | GND | - | | | GND | - | | |
| J9 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K7 | GND | - | | | GND | - | | |
| K8 | GND | - | | | GND | - | | |
| K9 | GND | - | | | GND | - | | |
| T1 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| E12 | VCC | - | | | VCC | - | | |

# LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP6/LFEC6 | | | | | LFECP10/LFEC10 | | | | | LFECP/LFEC15 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| F14 | PT23B | 1 | C | | F14 | PT31B | 1 | C | | F14 | PT31B | 1 | C | |
| D14 | PT23A | 1 | T | | D14 | PT31A | 1 | T | | D14 | PT31A | 1 | T | |
| E13 | PT22B | 1 | C | | E13 | PT30B | 1 | C | | E13 | PT30B | 1 | C | |
| G13 | PT22A | 1 | T | TDQS22 | G13 | PT30A | 1 | T | TDQS30 | G13 | PT30A | 1 | T | TDQS30 |
| A12 | PT21B | 1 | C | | A12 | PT29B | 1 | C | | A12 | PT29B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B12 | PT21A | 1 | T | | B12 | PT29A | 1 | T | | B12 | PT29A | 1 | T | |
| F13 | PT20B | 1 | C | | F13 | PT28B | 1 | C | | F13 | PT28B | 1 | C | |
| D13 | PT20A | 1 | T | | D13 | PT28A | 1 | T | | D13 | PT28A | 1 | T | |
| F12 | PT19B | 1 | C | VREF2_1 | F12 | PT27B | 1 | C | VREF2_1 | F12 | PT27B | 1 | C | VREF2_1 |
| D12 | PT19A | 1 | T | VREF1_1 | D12 | PT27A | 1 | T | VREF1_1 | D12 | PT27A | 1 | T | VREF1_1 |
| F11 | PT18B | 1 | C | | F11 | PT26B | 1 | C | | F11 | PT26B | 1 | C | |
| C12 | PT18A | 1 | T | | C12 | PT26A | 1 | T | | C12 | PT26A | 1 | T | |
| A11 | PT17B | 0 | C | PCLKC0_0 | A11 | PT25B | 0 | C | PCLKC0_0 | A11 | PT25B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A10 | PT17A | 0 | T | PCLKT0_0 | A10 | PT25A | 0 | T | PCLKT0_0 | A10 | PT25A | 0 | T | PCLKT0_0 |
| E12 | PT16B | 0 | C | VREF1_0 | E12 | PT24B | 0 | C | VREF1_0 | E12 | PT24B | 0 | C | VREF1_0 |
| E11 | PT16A | 0 | T | VREF2_0 | E11 | PT24A | 0 | T | VREF2_0 | E11 | PT24A | 0 | T | VREF2_0 |
| B11 | PT15B | 0 | C | | B11 | PT23B | 0 | C | | B11 | PT23B | 0 | C | |
| C11 | PT15A | 0 | T | | C11 | PT23A | 0 | T | | C11 | PT23A | 0 | T | |
| B9 | PT14B | 0 | C | | B9 | PT22B | 0 | C | | B9 | PT22B | 0 | C | |
| B10 | PT14A | 0 | T | TDQS14 | B10 | PT22A | 0 | T | TDQS22 | B10 | PT22A | 0 | T | TDQS22 |
| A9 | PT13B | 0 | C | | A9 | PT21B | 0 | C | | A9 | PT21B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A8 | PT13A | 0 | T | | A8 | PT21A | 0 | T | | A8 | PT21A | 0 | T | |
| D11 | PT12B | 0 | C | | D11 | PT20B | 0 | C | | D11 | PT20B | 0 | C | |
| C10 | PT12A | 0 | T | | C10 | PT20A | 0 | T | | C10 | PT20A | 0 | T | |
| A7 | PT11B | 0 | C | | A7 | PT19B | 0 | C | | A7 | PT19B | 0 | C | |
| A6 | PT11A | 0 | T | | A6 | PT19A | 0 | T | | A6 | PT19A | 0 | T | |
| B7 | PT10B | 0 | C | | B7 | PT18B | 0 | C | | B7 | PT18B | 0 | C | |
| B8 | PT10A | 0 | T | | B8 | PT18A | 0 | T | | B8 | PT18A | 0 | T | |
| A5 | PT9B | 0 | C | | A5 | PT17B | 0 | C | | A5 | PT17B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| B6 | PT9A | 0 | T | | B6 | PT17A | 0 | T | | B6 | PT17A | 0 | T | |
| G10 | PT8B | 0 | C | | G10 | PT16B | 0 | C | | G10 | PT16B | 0 | C | |
| E10 | PT8A | 0 | T | | E10 | PT16A | 0 | T | | E10 | PT16A | 0 | T | |
| F10 | PT7B | 0 | C | | F10 | PT15B | 0 | C | | F10 | PT15B | 0 | C | |
| D10 | PT7A | 0 | T | | D10 | PT15A | 0 | T | | D10 | PT15A | 0 | T | |
| G9 | PT6B | 0 | C | | G9 | PT14B | 0 | C | | G9 | PT14B | 0 | C | |
| E9 | PT6A | 0 | T | TDQS6 | E9 | PT14A | 0 | T | TDQS14 | E9 | PT14A | 0 | T | TDQS14 |
| C9 | PT5B | 0 | C | | C9 | PT13B | 0 | C | | C9 | PT13B | 0 | C | |
| GND | - | - | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| C8 | PT5A | 0 | T | | C8 | PT13A | 0 | T | | C8 | PT13A | 0 | T | |
| F9 | PT4B | 0 | C | | F9 | PT12B | 0 | C | | F9 | PT12B | 0 | C | |
| D9 | PT4A | 0 | T | | D9 | PT12A | 0 | T | | D9 | PT12A | 0 | T | |
| F8 | PT3B | 0 | C | | F8 | PT11B | 0 | C | | F8 | PT11B | 0 | C | |
| D7 | PT3A | 0 | T | | D7 | PT11A | 0 | T | | D7 | PT11A | 0 | T | |
| D8 | PT2B | 0 | C | | D8 | PT10B | 0 | C | | D8 | PT10B | 0 | C | |
| C7 | PT2A | 0 | T | | C7 | PT10A | 0 | T | | C7 | PT10A | 0 | T | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| A5 | PT13B | 0 | C | | A5 | PT13B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A4 | PT13A | 0 | T | | A4 | PT13A | 0 | T | |
| F9 | PT12B | 0 | C | | F9 | PT12B | 0 | C | |
| B6 | PT12A | 0 | T | | B6 | PT12A | 0 | T | |
| E9 | PT11B | 0 | C | | E9 | PT11B | 0 | C | |
| C8 | PT11A | 0 | T | | C8 | PT11A | 0 | T | |
| G8 | PT10B | 0 | C | | G8 | PT10B | 0 | C | |
| B5 | PT10A | 0 | T | | B5 | PT10A | 0 | T | |
| A3 | PT9B | 0 | C | | A3 | PT9B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A2 | PT9A | 0 | T | | A2 | PT9A | 0 | T | |
| F8 | PT8B | 0 | C | | F8 | PT8B | 0 | C | |
| B4 | PT8A | 0 | T | | B4 | PT8A | 0 | T | |
| E8 | PT7B | 0 | C | | E8 | PT7B | 0 | C | |
| B3 | PT7A | 0 | T | | B3 | PT7A | 0 | T | |
| D8 | PT6B | 0 | C | | D8 | PT6B | 0 | C | |
| G7 | PT6A | 0 | T | TDQS6 | G7 | PT6A | 0 | T | TDQS6 |
| C4 | PT5B | 0 | C | | C4 | PT5B | 0 | C | |
| C5 | PT5A | 0 | T | | C5 | PT5A | 0 | T | |
| E7 | PT4B | 0 | C | | E7 | PT4B | 0 | C | |
| D4 | PT4A | 0 | T | | D4 | PT4A | 0 | T | |
| F7 | PT3B | 0 | C | | F7 | PT3B | 0 | C | |
| D6 | PT3A | 0 | T | | D6 | PT3A | 0 | T | |
| D7 | PT2B | 0 | C | | D7 | PT2B | 0 | C | |
| E6 | PT2A | 0 | T | | E6 | PT2A | 0 | T | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| K10 | GND | - | | | K10 | GND | - | | |
| K11 | GND | - | | | K11 | GND | - | | |
| K12 | GND | - | | | K12 | GND | - | | |
| K13 | GND | - | | | K13 | GND | - | | |
| K14 | GND | - | | | K14 | GND | - | | |
| K15 | GND | - | | | K15 | GND | - | | |
| K16 | GND | - | | | K16 | GND | - | | |
| L10 | GND | - | | | L10 | GND | - | | |
| L11 | GND | - | | | L11 | GND | - | | |
| L12 | GND | - | | | L12 | GND | - | | |
| L13 | GND | - | | | L13 | GND | - | | |
| L14 | GND | - | | | L14 | GND | - | | |
| L15 | GND | - | | | L15 | GND | - | | |
| L16 | GND | - | | | L16 | GND | - | | |
| L17 | GND | - | | | L17 | GND | - | | |

**LatticeEC Commercial (Continued)**

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC10E-4F256C | 195 | -4 | fpBGA | 256 | COM | 10.2K |
| LFEC10E-5F256C | 195 | -5 | fpBGA | 256 | COM | 10.2K |
| LFEC10E-3Q208C | 147 | -3 | PQFP | 208 | COM | 10.2K |
| LFEC10E-4Q208C | 147 | -4 | PQFP | 208 | COM | 10.2K |
| LFEC10E-5Q208C | 147 | -5 | PQFP | 208 | COM | 10.2K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC15E-3F484C | 352 | -3 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-4F484C | 352 | -4 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-5F484C | 352 | -5 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-3F256C | 195 | -3 | fpBGA | 256 | COM | 15.3K |
| LFEC15E-4F256C | 195 | -4 | fpBGA | 256 | COM | 15.3K |
| LFEC15E-5F256C | 195 | -5 | fpBGA | 256 | COM | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC20E-3F672C | 400 | -3 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-4F672C | 400 | -4 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-5F672C | 400 | -5 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-3F484C | 360 | -3 | fpBGA | 484 | COM | 19.7K |
| LFEC20E-4F484C | 360 | -4 | fpBGA | 484 | COM | 19.7K |
| LFEC20E-5F484C | 360 | -5 | fpBGA | 484 | COM | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC33E-3F672C | 496 | -3 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-4F672C | 496 | -4 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-5F672C | 496 | -5 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-3F484C | 360 | -3 | fpBGA | 484 | COM | 32.8K |
| LFEC33E-4F484C | 360 | -4 | fpBGA | 484 | COM | 32.8K |
| LFEC33E-5F484C | 360 | -5 | fpBGA | 484 | COM | 32.8K |

## LatticeECP Commercial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP6E-3F484C | 224 | -3 | fpBGA | 484 | COM | 6.1K |
| LFECP6E-4F484C | 224 | -4 | fpBGA | 484 | COM | 6.1K |
| LFECP6E-5F484C | 224 | -5 | fpBGA | 484 | COM | 6.1K |
| LFECP6E-3F256C | 195 | -3 | fpBGA | 256 | COM | 6.1K |
| LFECP6E-4F256C | 195 | -4 | fpBGA | 256 | COM | 6.1K |
| LFECP6E-5F256C | 195 | -5 | fpBGA | 256 | COM | 6.1K |
| LFECP6E-3Q208C | 147 | -3 | PQFP | 208 | COM | 6.1K |
| LFECP6E-4Q208C | 147 | -4 | PQFP | 208 | COM | 6.1K |
| LFECP6E-5Q208C | 147 | -5 | PQFP | 208 | COM | 6.1K |
| LFECP6E-3T144C | 97 | -3 | TQFP | 144 | COM | 6.1K |
| LFECP6E-4T144C | 97 | -4 | TQFP | 144 | COM | 6.1K |
| LFECP6E-5T144C | 97 | -5 | TQFP | 144 | COM | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP10E-3F484C | 288 | -3 | fpBGA | 484 | COM | 10.2K |
| LFECP10E-4F484C | 288 | -4 | fpBGA | 484 | COM | 10.2K |
| LFECP10E-5F484C | 288 | -5 | fpBGA | 484 | COM | 10.2K |
| LFECP10E-3F256C | 195 | -3 | fpBGA | 256 | COM | 10.2K |
| LFECP10E-4F256C | 195 | -4 | fpBGA | 256 | COM | 10.2K |
| LFECP10E-5F256C | 195 | -5 | fpBGA | 256 | COM | 10.2K |
| LFECP10E-3Q208C | 147 | -3 | PQFP | 208 | COM | 10.2K |
| LFECP10E-4Q208C | 147 | -4 | PQFP | 208 | COM | 10.2K |
| LFECP10E-5Q208C | 147 | -5 | PQFP | 208 | COM | 10.2K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP15E-3F484C | 352 | -3 | fpBGA | 484 | COM | 15.3K |
| LFECP15E-4F484C | 352 | -4 | fpBGA | 484 | COM | 15.3K |
| LFECP15E-5F484C | 352 | -5 | fpBGA | 484 | COM | 15.3K |
| LFECP15E-3F256C | 195 | -3 | fpBGA | 256 | COM | 15.3K |
| LFECP15E-4F256C | 195 | -4 | fpBGA | 256 | COM | 15.3K |
| LFECP15E-5F256C | 195 | -5 | fpBGA | 256 | COM | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP20E-3F672C | 400 | -3 | fpBGA | 672 | COM | 19.7K |
| LFECP20E-4F672C | 400 | -4 | fpBGA | 672 | COM | 19.7K |
| LFECP20E-5F672C | 400 | -5 | fpBGA | 672 | COM | 19.7K |
| LFECP20E-3F484C | 360 | -3 | fpBGA | 484 | COM | 19.7K |
| LFECP20E-4F484C | 360 | -4 | fpBGA | 484 | COM | 19.7K |
| LFECP20E-5F484C | 360 | -5 | fpBGA | 484 | COM | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3F672C | 496 | -3 | fpBGA | 672 | COM | 32.8K |
| LFECP33E-4F672C | 496 | -4 | fpBGA | 672 | COM | 32.8K |
| LFECP33E-5F672C | 496 | -5 | fpBGA | 672 | COM | 32.8K |

### LatticeECP Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3F484C | 360 | -3 | fpBGA | 484 | COM | 32.8K |
| LFECP33E-4F484C | 360 | -4 | fpBGA | 484 | COM | 32.8K |
| LFECP33E-5F484C | 360 | -5 | fpBGA | 484 | COM | 32.8K |

### LatticeEC Industrial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC1E-3Q208I | 112 | -3 | PQFP | 208 | IND | 1.5K |
| LFEC1E-4Q208I | 112 | -4 | PQFP | 208 | IND | 1.5K |
| LFEC1E-3T144I | 97 | -3 | TQFP | 144 | IND | 1.5K |
| LFEC1E-4T144I | 97 | -4 | TQFP | 144 | IND | 1.5K |
| LFEC1E-3T100I | 67 | -3 | TQFP | 100 | IND | 1.5K |
| LFEC1E-4T100I | 67 | -4 | TQFP | 100 | IND | 1.5K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC3E-3F256I | 160 | -3 | fpBGA | 256 | IND | 3.1K |
| LFEC3E-4F256I | 160 | -4 | fpBGA | 256 | IND | 3.1K |
| LFEC3E-3Q208I | 145 | -3 | PQFP | 208 | IND | 3.1K |
| LFEC3E-4Q208I | 145 | -4 | PQFP | 208 | IND | 3.1K |
| LFEC3E-3T144I | 97 | -3 | TQFP | 144 | IND | 3.1K |
| LFEC3E-4T144I | 97 | -4 | TQFP | 144 | IND | 3.1K |
| LFEC3E-3T100I | 67 | -3 | TQFP | 100 | IND | 3.1K |
| LFEC3E-4T100I | 67 | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC6E-3F484I | 224 | -3 | fpBGA | 484 | IND | 6.1K |
| LFEC6E-4F484I | 224 | -4 | fpBGA | 484 | IND | 6.1K |
| LFEC6E-3F256I | 195 | -3 | fpBGA | 256 | IND | 6.1K |
| LFEC6E-4F256I | 195 | -4 | fpBGA | 256 | IND | 6.1K |
| LFEC6E-3Q208I | 147 | -3 | PQFP | 208 | IND | 6.1K |
| LFEC6E-4Q208I | 147 | -4 | PQFP | 208 | IND | 6.1K |
| LFEC6E-3T144I | 97 | -3 | TQFP | 144 | IND | 6.1K |
| LFEC6E-4T144I | 97 | -4 | TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC10E-3F484I | 288 | -3 | fpBGA | 484 | IND | 10.2K |
| LFEC10E-4F484I | 288 | -4 | fpBGA | 484 | IND | 10.2K |
| LFEC10E-3F256I | 195 | -3 | fpBGA | 256 | IND | 10.2K |
| LFEC10E-4F256I | 195 | -4 | fpBGA | 256 | IND | 10.2K |
| LFEC10E-3 P208I | 147 | -3 | PQFP | 208 | IND | 10.2K |
| LFEC10E-4 P208I | 147 | -4 | PQFP | 208 | IND | 10.2K |