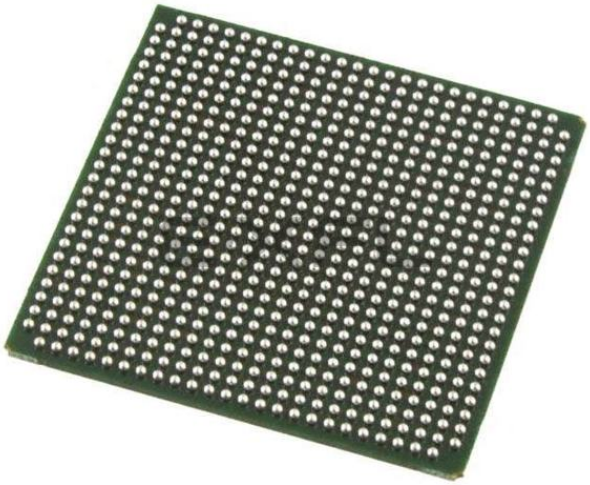


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 19700 |
| Total RAM Bits | 434176 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec20e-4fn672c |

*Figure 2-4. Slice Diagram*

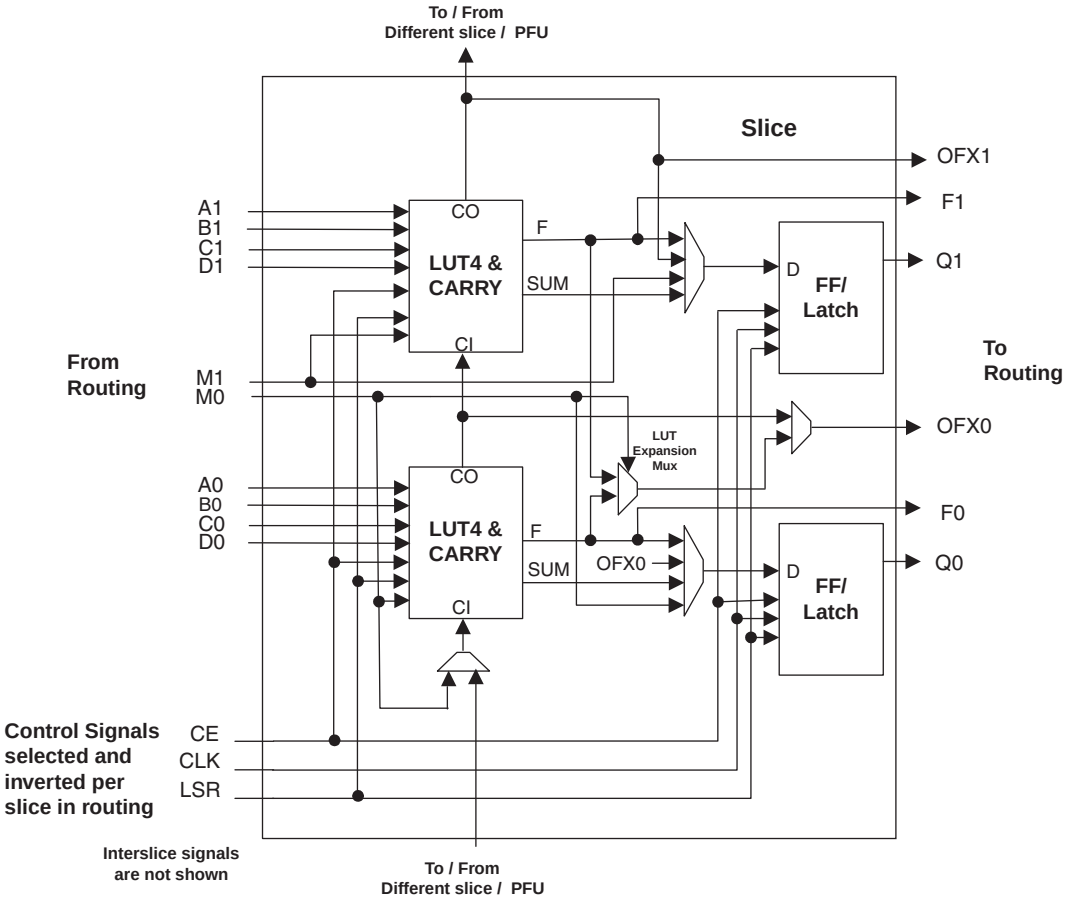



*Table 2-1. Slice Signal Descriptions*

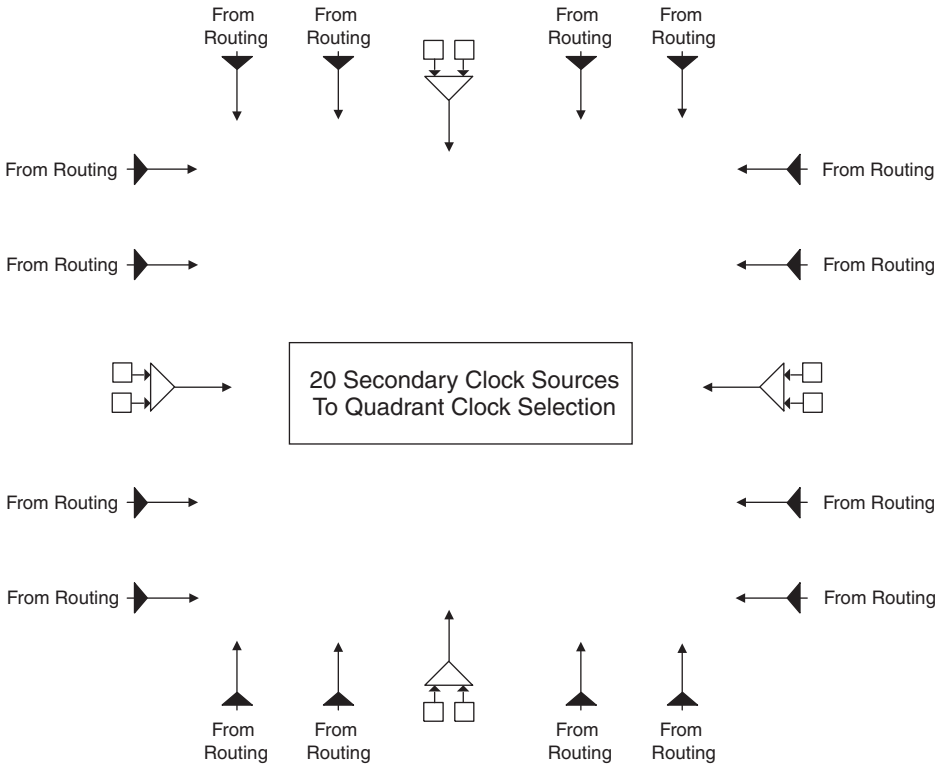
| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

## Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

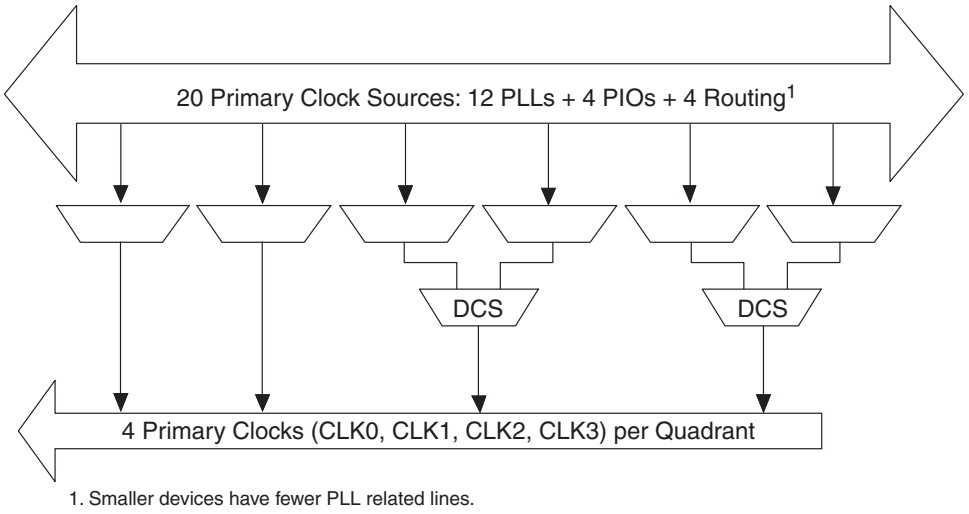
***Figure 2-7. Secondary Clock Sources***




## Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

*Figure 2-8. Per Quadrant Primary Clock Selection*




1. Smaller devices have fewer PLL related lines.

*Figure 2-9. Per Quadrant Secondary Clock Selection*

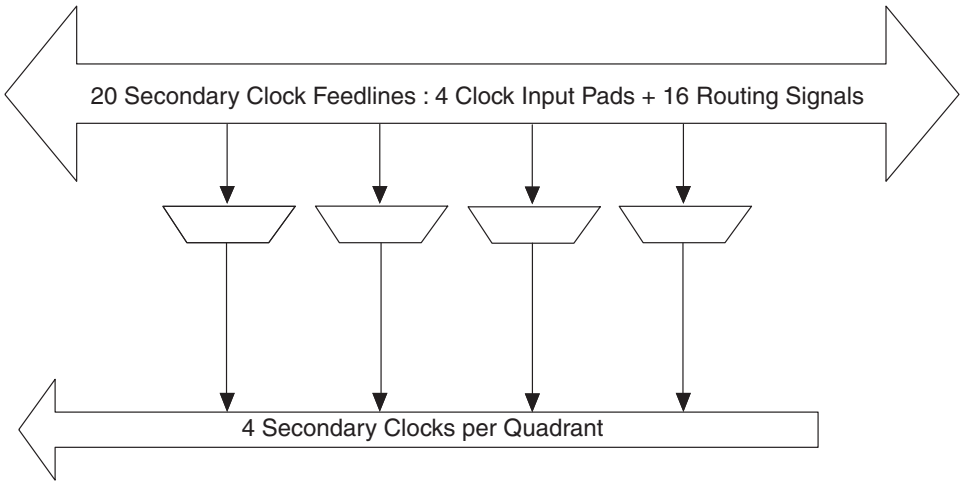
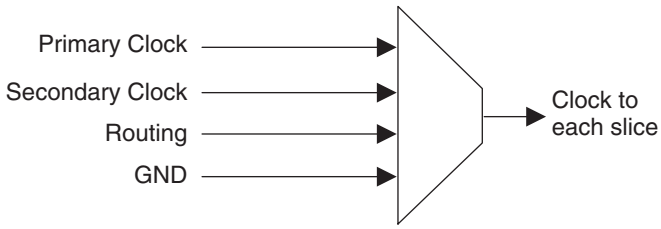



*Figure 2-10. Slice Clock Selection*




## sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

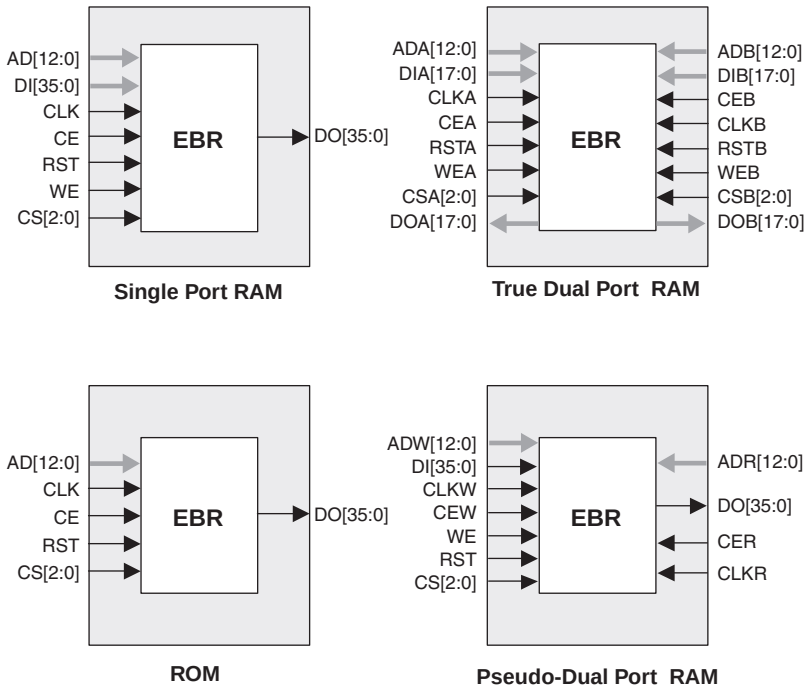
## Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

***Figure 2-15. sysMEM EBR Primitives***




The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

## IPexpress™

The user can access the sysDSP block via the IPexpress configuration tool, included with the ispLEVER design tool suite. IPexpress has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

## Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

## Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

***Table 2-9. Number of DSP Blocks in LatticeECP Family***

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---|---|---|---|---|
| LFECP6 | 4 | 32 | 16 | 4 |
| LFECP10 | 5 | 40 | 20 | 5 |
| LFECP15 | 6 | 48 | 24 | 6 |
| LFECP20 | 7 | 56 | 28 | 7 |
| LFECP33 | 8 | 64 | 32 | 8 |

***Table 2-10. Embedded SRAM in LatticeECP Family***

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) |
|---|---|---|
| LFECP6 | 10 | 92 |
| LFECP10 | 30 | 276 |
| LFECP15 | 38 | 350 |
| LFECP20 | 46 | 424 |
| LFECP33 | 54 | 498 |

## DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

***Table 2-11. DSP Block Performance of LatticeECP Family***

| Device | DSP Block | DSP Performance MMAC |
|---|---|---|
| LFECP6 | 4 | 3680 |
| LFECP10 | 5 | 4600 |
| LFECP15 | 6 | 5520 |
| LFECP20 | 7 | 6440 |
| LFECP33 | 8 | 7360 |

*Figure 2-27. Input Register DDR Waveforms*

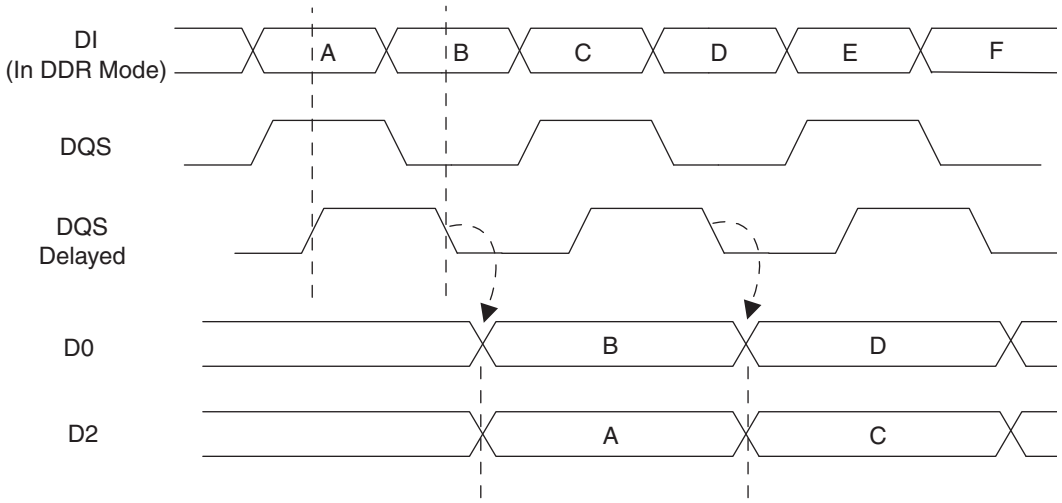
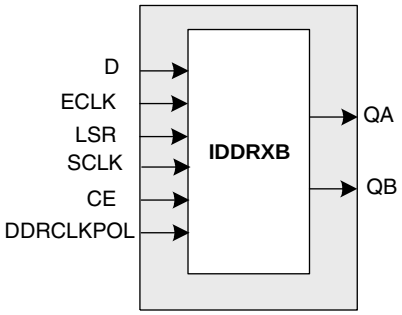



*Figure 2-28. INDDRXB Primitive*




**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

### Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeECP/EC family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

## sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

### sysI/O Buffer Banks

LatticeECP/EC devices have eight sysI/O buffer banks; each is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage ($V_{CCIO}$), and two voltage references $V_{REF1}$ and $V_{REF2}$ resources allowing each bank to be completely independent from each other. Figure 2-34 shows the eight banks and their associated supplies.

In the LatticeECP/EC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO.}$ LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold input independent of $V_{CCIO.}$ In addition to the bank $V_{CCIO}$ supplies, the LatticeECP/EC devices have a $V_{CC}$ core logic power supply, and a $V_{CCAUX}$ supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeECP/EC devices, some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

## Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master clock for configuration. The oscillator and the master clock run continuously. The default value of the master clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information about the use of this oscillator for configuration, please see the list of technical documentation at the end of this data sheet.

***Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration***

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|---|---|---|
| 2.5* | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |

# Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

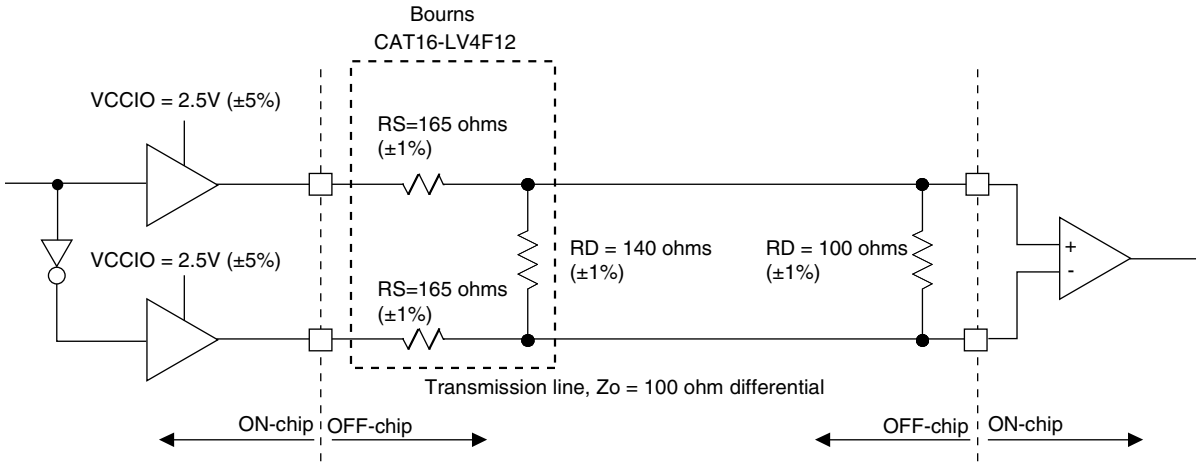



***Table 3-1. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.42 | V |
| $V_{OL}$ | Output low voltage | 1.08 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | ¾ |

## Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected.<br><br>Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.<br><br>During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins. |
| $V_{CCIOx}$ | — | Power supply pins for I/O bank x. Dedicated pins. |
| $V_{REF1\_x}$, $V_{REF2\_x}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| XRES | — | 10K ohm +/-1% resistor must be connected between this pad and ground. |
| $V_{CCPLL}$ | — | Power supply pin for PLL.þApplicable to ECP/EC33 device. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN_A | I | Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_PLL[T, C]_FB_A | I | Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |
| [LOC]DQS[num] | I | DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output. |
| **Test and Programming** (Dedicated pins) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |

## PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO Within PIC | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |

Notes:
1. “n” is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

## LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFECP6/LFEC6 | | | | LFECP10/LFEC10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 43 | PL24A | 6 | T | LDQS24 | PL33A | 6 | T | LDQS33 |
| 44 | PL24B | 6 | C | | PL33B | 6 | C | |
| 45 | PL25A | 6 | T | | PL34A | 6 | T | |
| 46 | PL25B | 6 | C | | PL34B | 6 | C | |
| 47 | PL26A | 6 | T | | PL35A | 6 | T | |
| 48 | PL26B | 6 | C | | PL35B | 6 | C | |
| 49 | PL27A | 6 | T | VREF1_6 | PL36A | 6 | T | VREF1_6 |
| 50 | PL27B | 6 | C | VREF2_6 | PL36B | 6 | C | VREF2_6 |
| 51 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 52* | GND5<br>GND6 | - | | | GND5<br>GND6 | - | | |
| 53 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 54 | PB2A | 5 | T | | PB2A | 5 | T | |
| 55 | PB2B | 5 | C | | PB2B | 5 | C | |
| 56 | PB3A | 5 | T | | PB3A | 5 | T | |
| 57 | PB3B | 5 | C | | PB3B | 5 | C | |
| 58 | PB4A | 5 | T | | PB4A | 5 | T | |
| 59 | PB4B | 5 | C | | PB4B | 5 | C | |
| 60 | PB5A | 5 | T | | PB5A | 5 | T | |
| 61 | PB5B | 5 | C | | PB5B | 5 | C | |
| 62 | PB6A | 5 | T | BDQS6 | PB6A | 5 | T | BDQS6 |
| 63 | PB6B | 5 | C | | PB6B | 5 | C | |
| 64 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 65 | PB10A | 5 | T | | PB18A | 5 | T | |
| 66 | PB10B | 5 | C | | PB18B | 5 | C | |
| 67 | PB11A | 5 | T | | PB19A | 5 | T | |
| 68 | PB11B | 5 | C | | PB19B | 5 | C | |
| 69 | PB12A | 5 | T | | PB20A | 5 | T | |
| 70 | PB12B | 5 | C | | PB20B | 5 | C | |
| 71 | PB13A | 5 | T | | PB21A | 5 | T | |
| 72 | GND5 | 5 | | | GND5 | 5 | | |
| 73 | PB13B | 5 | C | | PB21B | 5 | C | |
| 74 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 75 | PB14A | 5 | T | BDQS14 | PB22A | 5 | T | BDQS22 |
| 76 | PB14B | 5 | C | | PB22B | 5 | C | |
| 77 | PB15A | 5 | T | | PB23A | 5 | T | |
| 78 | PB15B | 5 | C | | PB23B | 5 | C | |
| 79 | PB16A | 5 | T | VREF2_5 | PB24A | 5 | T | VREF2_5 |
| 80 | PB16B | 5 | C | VREF1_5 | PB24B | 5 | C | VREF1_5 |
| 81 | PB17A | 5 | T | PCLKT5_0 | PB25A | 5 | T | PCLKT5_0 |
| 82 | GND5 | 5 | | | GND5 | 5 | | |
| 83 | PB17B | 5 | C | PCLKC5_0 | PB25B | 5 | C | PCLKC5_0 |
| 84 | VCCAUX | - | | | VCCAUX | - | | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| V2 | PL41B | 6 | C | LLM0_PLLC_IN_A | V2 | PL53B | 6 | C | LLM0_PLLC_IN_A |
| U3 | PL42A | 6 | T | LLM0_PLLT_FB_A | U3 | PL54A | 6 | T | LLM0_PLLT_FB_A |
| V3 | PL42B | 6 | C | LLM0_PLLC_FB_A | V3 | PL54B | 6 | C | LLM0_PLLC_FB_A |
| U4 | PL43A | 6 | T | | U4 | PL55A | 6 | T | |
| V5 | PL43B | 6 | C | | V5 | PL55B | 6 | C | |
| W1 | PL44A | 6 | T | | W1 | PL56A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| W2 | PL44B | 6 | C | | W2 | PL56B | 6 | C | |
| Y1 | PL45A | 6 | T | LDQS45 | Y1 | PL57A | 6 | T | LDQS57 |
| Y2 | PL45B | 6 | C | | Y2 | PL57B | 6 | C | |
| AA1 | PL46A | 6 | T | | AA1 | PL58A | 6 | T | |
| AA2 | PL46B | 6 | C | | AA2 | PL58B | 6 | C | |
| W4 | PL47A | 6 | T | | W4 | PL59A | 6 | T | |
| V4 | PL47B | 6 | C | | V4 | PL59B | 6 | C | |
| W3 | PL48A | 6 | T | VREF1_6 | W3 | PL68A | 6 | T | VREF1_6 |
| Y3 | PL48B | 6 | C | VREF2_6 | Y3 | PL68B | 6 | C | VREF2_6 |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| GND | GND5 | 5 | | | GND | GND6 | 6 | | |
| GND | - | | | | GND | GND6 | 6 | | |
| GND | - | | | | GND | GND5 | 5 | | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| V7 | PB10A | 5 | T | | V7 | PB10A | 5 | T | |
| T6 | PB10B | 5 | C | | T6 | PB10B | 5 | C | |
| V8 | PB11A | 5 | T | | V8 | PB11A | 5 | T | |
| U7 | PB11B | 5 | C | | U7 | PB11B | 5 | C | |
| W5 | PB12A | 5 | T | | W5 | PB12A | 5 | T | |
| U6 | PB12B | 5 | C | | U6 | PB12B | 5 | C | |
| AA3 | PB13A | 5 | T | | AA3 | PB13A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB3 | PB13B | 5 | C | | AB3 | PB13B | 5 | C | |
| Y6 | PB14A | 5 | T | BDQS14 | Y6 | PB14A | 5 | T | BDQS14 |
| V6 | PB14B | 5 | C | | V6 | PB14B | 5 | C | |
| AA5 | PB15A | 5 | T | | AA5 | PB15A | 5 | T | |
| W6 | PB15B | 5 | C | | W6 | PB15B | 5 | C | |
| Y5 | PB16A | 5 | T | | Y5 | PB16A | 5 | T | |
| Y4 | PB16B | 5 | C | | Y4 | PB16B | 5 | C | |
| AA4 | PB17A | 5 | T | | AA4 | PB17A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB4 | PB17B | 5 | C | | AB4 | PB17B | 5 | C | |
| Y7 | PB18A | 5 | T | | Y7 | PB18A | 5 | T | |
| W8 | PB18B | 5 | C | | W8 | PB18B | 5 | C | |
| W7 | PB19A | 5 | T | | W7 | PB19A | 5 | T | |
| U8 | PB19B | 5 | C | | U8 | PB19B | 5 | C | |
| W9 | PB20A | 5 | T | | W9 | PB20A | 5 | T | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| AB1 | GND | - | | | AB1 | GND | - | | |
| AB22 | GND | - | | | AB22 | GND | - | | |
| H15 | GND | - | | | H15 | GND | - | | |
| H8 | GND | - | | | H8 | GND | - | | |
| J10 | GND | - | | | J10 | GND | - | | |
| J11 | GND | - | | | J11 | GND | - | | |
| J12 | GND | - | | | J12 | GND | - | | |
| J13 | GND | - | | | J13 | GND | - | | |
| J14 | GND | - | | | J14 | GND | - | | |
| J9 | GND | - | | | J9 | GND | - | | |
| K10 | GND | - | | | K10 | GND | - | | |
| K11 | GND | - | | | K11 | GND | - | | |
| K12 | GND | - | | | K12 | GND | - | | |
| K13 | GND | - | | | K13 | GND | - | | |
| K14 | GND | - | | | K14 | GND | - | | |
| K9 | GND | - | | | K9 | GND | - | | |
| L10 | GND | - | | | L10 | GND | - | | |
| L11 | GND | - | | | L11 | GND | - | | |
| L12 | GND | - | | | L12 | GND | - | | |
| L13 | GND | - | | | L13 | GND | - | | |
| L14 | GND | - | | | L14 | GND | - | | |
| L9 | GND | - | | | L9 | GND | - | | |
| M10 | GND | - | | | M10 | GND | - | | |
| M11 | GND | - | | | M11 | GND | - | | |
| M12 | GND | - | | | M12 | GND | - | | |
| M13 | GND | - | | | M13 | GND | - | | |
| M14 | GND | - | | | M14 | GND | - | | |
| M9 | GND | - | | | M9 | GND | - | | |
| N10 | GND | - | | | N10 | GND | - | | |
| N11 | GND | - | | | N11 | GND | - | | |
| N12 | GND | - | | | N12 | GND | - | | |
| N13 | GND | - | | | N13 | GND | - | | |
| N14 | GND | - | | | N14 | GND | - | | |
| N9 | GND | - | | | N9 | GND | - | | |
| P10 | GND | - | | | P10 | GND | - | | |
| P11 | GND | - | | | P11 | GND | - | | |
| P12 | GND | - | | | P12 | GND | - | | |
| P13 | GND | - | | | P13 | GND | - | | |
| P14 | GND | - | | | P14 | GND | - | | |
| P9 | GND | - | | | P9 | GND | - | | |
| R15 | GND | - | | | R15 | GND | - | | |
| R8 | GND | - | | | R8 | GND | - | | |
| J16 | VCC | - | | | J16 | VCC | - | | |
| J7 | VCC | - | | | J7 | VCC | - | | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| L7 | VCCIO7 | 7 | | | L7 | VCCIO7 | 7 | | |
| L8 | VCCIO7 | 7 | | | L8 | VCCIO7 | 7 | | |
| G15 | VCCAUX | - | | | G15 | VCCAUX | - | | |
| G16 | VCCAUX | - | | | G16 | VCCAUX | - | | |
| G7 | VCCAUX | - | | | G7 | VCCAUX | - | | |
| G8 | VCCAUX | - | | | G8 | VCCAUX | - | | |
| H16 | VCCAUX | - | | | H16 | VCCAUX | - | | |
| H7 | VCCAUX | - | | | H7 | VCCAUX | - | | |
| R16 | VCCAUX | - | | | R16 | VCCAUX | - | | |
| R7 | VCCAUX | - | | | R7 | VCCAUX | - | | |
| T15 | VCCAUX | - | | | T15 | VCCAUX | - | | |
| T16 | VCCAUX | - | | | T16 | VCCAUX | - | | |
| T7 | VCCAUX | - | | | T7 | VCCAUX | - | | |
| T8 | VCCAUX | - | | | T8 | VCCAUX | - | | |
| J6 | VCC[1] | - | | | J6 | VCCPLL | - | | |
| J17 | VCC[1] | - | | | J17 | VCCPLL | - | | |
| P6 | VCC[1] | - | | | P6 | VCCPLL | - | | |
| P17 | VCC[1] | - | | | P17 | VCCPLL | - | | |
| A2 | NC | - | | | A2 | NC | - | | |
| AB2 | NC | - | | | AB2 | NC | - | | |
| A21 | NC | - | | | A21 | NC | - | | |

1. Tied to $V_{CCPLL}$.

# LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| E3 | PL2A | 7 | T | VREF2_7 | E3 | PL2A | 7 | T | VREF2_7 |
| E4 | PL2B | 7 | C | VREF1_7 | E4 | PL2B | 7 | C | VREF1_7 |
| E5 | NC | - | | | E5 | PL6A | 7 | T | LDQS6 |
| D5 | NC | - | | | D5 | PL6B | 7 | C | |
| F4 | NC | - | | | F4 | PL7A | 7 | T | |
| F5 | NC | - | | | F5 | PL7B | 7 | C | |
| C3 | NC | - | | | C3 | PL8A | 7 | T | |
| D3 | NC | - | | | D3 | PL8B | 7 | C | |
| C2 | NC | - | | | C2 | PL9A | 7 | T | |
| - | - | - | | | GND | GND7 | 7 | | |
| B2 | NC | - | | | B2 | PL9B | 7 | C | |
| B1 | PL3A | 7 | T | | B1 | PL10A | 7 | T | |
| C1 | PL3B | 7 | C | | C1 | PL10B | 7 | C | |
| F3 | PL4A | 7 | T | | F3 | PL11A | 7 | T | |
| G3 | PL4B | 7 | C | | G3 | PL11B | 7 | C | |
| D2 | PL5A | 7 | T | | D2 | PL12A | 7 | T | |
| E2 | PL5B | 7 | C | | E2 | PL12B | 7 | C | |
| - | - | - | | | GND | GND7 | 7 | | |
| D1 | PL6A | 7 | T | LDQS6 | D1 | PL14A | 7 | T | LDQS14 |
| E1 | PL6B | 7 | C | | E1 | PL14B | 7 | C | |
| F2 | PL7A | 7 | T | | F2 | PL15A | 7 | T | |
| G2 | PL7B | 7 | C | | G2 | PL15B | 7 | C | |
| F6 | PL8A | 7 | T | LUM0_PLLT_IN_A | F6 | PL16A | 7 | T | LUM0_PLLT_IN_A |
| G6 | PL8B | 7 | C | LUM0_PLLC_IN_A | G6 | PL16B | 7 | C | LUM0_PLLC_IN_A |
| H4 | PL9A | 7 | T | LUM0_PLLT_FB_A | H4 | PL17A | 7 | T | LUM0_PLLT_FB_A |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| G4 | PL9B | 7 | C | LUM0_PLLC_FB_A | G4 | PL17B | 7 | C | LUM0_PLLC_FB_A |
| H6 | NC | - | | | H6 | PL19A | 7 | T | |
| J7 | NC | - | | | J7 | PL19B | 7 | C | |
| G5 | NC | - | | | G5 | PL20A | 7 | T | |
| H5 | NC | - | | | H5 | PL20B | 7 | C | |
| H3 | NC | - | | | H3 | PL21A | 7 | T | |
| J3 | NC | - | | | J3 | PL21B | 7 | C | |
| H2 | NC | - | | | H2 | PL22A | 7 | T | |
| - | - | - | | | GND | GND7 | 7 | | |
| J2 | NC | - | | | J2 | PL22B | 7 | C | |
| J4 | PL11A | 7 | T | | J4 | PL23A | 7 | T | LDQS23 |
| J5 | PL11B | 7 | C | | J5 | PL23B | 7 | C | |
| K4 | PL12A | 7 | T | | K4 | PL24A | 7 | T | |
| K5 | PL12B | 7 | C | | K5 | PL24B | 7 | C | |
| J6 | PL13A | 7 | T | | J6 | PL25A | 7 | T | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| P5 | PL32B | 6 | C | | P5 | PL44B | 6 | C | |
| P6 | PL33A | 6 | T | | P6 | PL45A | 6 | T | |
| R5 | PL33B | 6 | C | | R5 | PL45B | 6 | C | |
| U1 | PL34A | 6 | T | | U1 | PL46A | 6 | T | |
| U2 | PL34B | 6 | C | | U2 | PL46B | 6 | C | |
| T3 | PL35A | 6 | T | | T3 | PL47A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| T4 | PL35B | 6 | C | | T4 | PL47B | 6 | C | |
| R6 | PL36A | 6 | T | LDQS36 | R6 | PL48A | 6 | T | LDQS48 |
| T5 | PL36B | 6 | C | | T5 | PL48B | 6 | C | |
| T6 | PL37A | 6 | T | | T6 | PL49A | 6 | T | |
| U5 | PL37B | 6 | C | | U5 | PL49B | 6 | C | |
| U3 | PL38A | 6 | T | | U3 | PL50A | 6 | T | |
| U4 | PL38B | 6 | C | | U4 | PL50B | 6 | C | |
| V1 | PL39A | 6 | T | | V1 | PL51A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| V2 | PL39B | 6 | C | | V2 | PL51B | 6 | C | |
| U7 | TCK | 6 | | | U7 | TCK | 6 | | |
| V4 | TDI | 6 | | | V4 | TDI | 6 | | |
| V5 | TMS | 6 | | | V5 | TMS | 6 | | |
| V3 | TDO | 6 | | | V3 | TDO | 6 | | |
| U6 | VCCJ | 6 | | | U6 | VCCJ | 6 | | |
| W1 | PL41A | 6 | T | LLM0_PLLT_IN_A | W1 | PL53A | 6 | T | LLM0_PLLT_IN_A |
| W2 | PL41B | 6 | C | LLM0_PLLC_IN_A | W2 | PL53B | 6 | C | LLM0_PLLC_IN_A |
| V6 | PL42A | 6 | T | LLM0_PLLT_FB_A | V6 | PL54A | 6 | T | LLM0_PLLT_FB_A |
| W6 | PL42B | 6 | C | LLM0_PLLC_FB_A | W6 | PL54B | 6 | C | LLM0_PLLC_FB_A |
| Y1 | PL43A | 6 | T | | Y1 | PL55A | 6 | T | |
| Y2 | PL43B | 6 | C | | Y2 | PL55B | 6 | C | |
| W3 | PL44A | 6 | T | | W3 | PL56A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| W4 | PL44B | 6 | C | | W4 | PL56B | 6 | C | |
| AA1 | PL45A | 6 | T | LDQS45 | AA1 | PL57A | 6 | T | LDQS57 |
| AB1 | PL45B | 6 | C | | AB1 | PL57B | 6 | C | |
| Y4 | PL46A | 6 | T | | Y4 | PL58A | 6 | T | |
| Y3 | PL46B | 6 | C | | Y3 | PL58B | 6 | C | |
| AC1 | PL47A | 6 | T | | AC1 | PL59A | 6 | T | |
| AB2 | PL47B | 6 | C | | AB2 | PL59B | 6 | C | |
| AA2 | NC | - | | | AA2 | PL60A | 6 | T | |
| - | - | - | | | GND | GND6 | 6 | | |
| AA3 | NC | - | | | AA3 | PL60B | 6 | C | |
| W5 | NC | - | | | W5 | PL61A | 6 | T | |
| Y5 | NC | - | | | Y5 | PL61B | 6 | C | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| A21 | PT51A | 1 | T | | A21 | PT51A | 1 | T | |
| E17 | PT50B | 1 | C | | E17 | PT50B | 1 | C | |
| B17 | PT50A | 1 | T | | B17 | PT50A | 1 | T | |
| C17 | PT49B | 1 | C | | C17 | PT49B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| D17 | PT49A | 1 | T | | D17 | PT49A | 1 | T | |
| F17 | PT48B | 1 | C | | F17 | PT48B | 1 | C | |
| E20 | PT48A | 1 | T | | E20 | PT48A | 1 | T | |
| G17 | PT47B | 1 | C | | G17 | PT47B | 1 | C | |
| B20 | PT47A | 1 | T | | B20 | PT47A | 1 | T | |
| E16 | PT46B | 1 | C | | E16 | PT46B | 1 | C | |
| A20 | PT46A | 1 | T | TDQS46 | A20 | PT46A | 1 | T | TDQS46 |
| A19 | PT45B | 1 | C | | A19 | PT45B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B19 | PT45A | 1 | T | | B19 | PT45A | 1 | T | |
| D16 | PT44B | 1 | C | | D16 | PT44B | 1 | C | |
| C16 | PT44A | 1 | T | | C16 | PT44A | 1 | T | |
| F16 | PT43B | 1 | C | | F16 | PT43B | 1 | C | |
| A18 | PT43A | 1 | T | | A18 | PT43A | 1 | T | |
| G16 | PT42B | 1 | C | | G16 | PT42B | 1 | C | |
| B18 | PT42A | 1 | T | | B18 | PT42A | 1 | T | |
| A17 | PT41B | 1 | C | | A17 | PT41B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A16 | PT41A | 1 | T | | A16 | PT41A | 1 | T | |
| D15 | PT40B | 1 | C | | D15 | PT40B | 1 | C | |
| B16 | PT40A | 1 | T | | B16 | PT40A | 1 | T | |
| E15 | PT39B | 1 | C | | E15 | PT39B | 1 | C | |
| C15 | PT39A | 1 | T | | C15 | PT39A | 1 | T | |
| F15 | PT38B | 1 | C | | F15 | PT38B | 1 | C | |
| G15 | PT38A | 1 | T | TDQS38 | G15 | PT38A | 1 | T | TDQS38 |
| B15 | PT37B | 1 | C | | B15 | PT37B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A15 | PT37A | 1 | T | | A15 | PT37A | 1 | T | |
| E14 | PT36B | 1 | C | | E14 | PT36B | 1 | C | |
| G14 | PT36A | 1 | T | | G14 | PT36A | 1 | T | |
| D14 | PT35B | 1 | C | VREF2_1 | D14 | PT35B | 1 | C | VREF2_1 |
| E13 | PT35A | 1 | T | VREF1_1 | E13 | PT35A | 1 | T | VREF1_1 |
| F14 | PT34B | 1 | C | | F14 | PT34B | 1 | C | |
| C14 | PT34A | 1 | T | | C14 | PT34A | 1 | T | |
| B14 | PT33B | 0 | C | PCLKC0_0 | B14 | PT33B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A14 | PT33A | 0 | T | PCLKT0_0 | A14 | PT33A | 0 | T | PCLKT0_0 |

### LatticeEC Industrial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC15E-3F484I | 352 | -3 | fpBGA | 484 | IND | 15.3K |
| LFEC15E-4F484I | 352 | -4 | fpBGA | 484 | IND | 15.3K |
| LFEC15E-3F256I | 195 | -3 | fpBGA | 256 | IND | 15.3K |
| LFEC15E-4F256I | 195 | -4 | fpBGA | 256 | IND | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC20E-3F672I | 400 | -3 | fpBGA | 672 | IND | 19.7K |
| LFEC20E-4F672I | 400 | -4 | fpBGA | 672 | IND | 19.7K |
| LFEC20E-3F484I | 360 | -3 | fpBGA | 484 | IND | 19.7K |
| LFEC20E-4F484I | 360 | -4 | fpBGA | 484 | IND | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC33E-3F672I | 496 | -3 | fpBGA | 672 | IND | 32.8 |
| LFEC33E-4F672I | 496 | -4 | fpBGA | 672 | IND | 32.8 |
| LFEC33E-3F484I | 360 | -3 | fpBGA | 484 | IND | 32.8 |
| LFEC33E-4F484I | 360 | -4 | fpBGA | 484 | IND | 32.8 |

### LatticeECP Industrial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP6E-3F484I | 224 | -3 | fpBGA | 484 | IND | 6.1K |
| LFECP6E-4F484I | 224 | -4 | fpBGA | 484 | IND | 6.1K |
| LFECP6E-3F256I | 195 | -3 | fpBGA | 256 | IND | 6.1K |
| LFECP6E-4F256I | 195 | -4 | fpBGA | 256 | IND | 6.1K |
| LFECP6E-3Q208I | 147 | -3 | PQFP | 208 | IND | 6.1K |
| LFECP6E-4Q208I | 147 | -4 | PQFP | 208 | IND | 6.1K |
| LFECP6E-3T144I | 97 | -3 | TQFP | 144 | IND | 6.1K |
| LFECP6E-4T144I | 97 | -4 | TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP10E-3F484I | 288 | -3 | fpBGA | 484 | IND | 10.2K |
| LFECP10E-4F484I | 288 | -4 | fpBGA | 484 | IND | 10.2K |
| LFECP10E-3F256I | 195 | -3 | fpBGA | 256 | IND | 10.2K |
| LFECP10E-4F256I | 195 | -4 | fpBGA | 256 | IND | 10.2K |
| LFECP10E-3Q208I | 147 | -3 | PQFP | 208 | IND | 10.2K |
| LFECP10E-4Q208I | 147 | -4 | PQFP | 208 | IND | 10.2K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP15E-3F484I | 352 | -3 | fpBGA | 484 | IND | 15.3K |
| LFECP15E-4F484I | 352 | -4 | fpBGA | 484 | IND | 15.3K |
| LFECP15E-3F256I | 195 | -3 | fpBGA | 256 | IND | 15.3K |
| LFECP15E-4F256I | 195 | -4 | fpBGA | 256 | IND | 15.3K |

### LatticeECP Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3FN484C | 360 | -3 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFECP33E-4FN484C | 360 | -4 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFECP33E-5FN484C | 360 | -5 | Lead-Free fpBGA | 484 | COM | 32.8K |

### LatticeEC Industrial

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC1E-3QN208I | 112 | -3 | Lead-Free PQFP | 208 | IND | 1.5K |
| LFEC1E-4QN208I | 112 | -4 | Lead-Free PQFP | 208 | IND | 1.5K |
| LFEC1E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 1.5K |
| LFEC1E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 1.5K |
| LFEC1E-3TN100I | 67 | -3 | Lead-Free TQFP | 100 | IND | 1.5K |
| LFEC1E-4TN100I | 67 | -4 | Lead-Free TQFP | 100 | IND | 1.5K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC3E-3FN256I | 160 | -3 | Lead-Free fpBGA | 256 | IND | 3.1K |
| LFEC3E-4FN256I | 160 | -4 | Lead-Free fpBGA | 256 | IND | 3.1K |
| LFEC3E-3QN208I | 145 | -3 | Lead-Free PQFP | 208 | IND | 3.1K |
| LFEC3E-4QN208I | 145 | -4 | Lead-Free PQFP | 208 | IND | 3.1K |
| LFEC3E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 3.1K |
| LFEC3E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 3.1K |
| LFEC3E-3TN100I | 67 | -3 | Lead-Free TQFP | 100 | IND | 3.1K |
| LFEC3E-4TN100I | 67 | -4 | Lead-Free TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC6E-3FN484I | 224 | -3 | Lead-Free fpBGA | 484 | IND | 6.1K |
| LFEC6E-4FN484I | 224 | -4 | Lead-Free fpBGA | 484 | IND | 6.1K |
| LFEC6E-3FN256I | 195 | -3 | Lead-Free fpBGA | 256 | IND | 6.1K |
| LFEC6E-4FN256I | 195 | -4 | Lead-Free fpBGA | 256 | IND | 6.1K |
| LFEC6E-3QN208I | 147 | -3 | Lead-Free PQFP | 208 | IND | 6.1K |
| LFEC6E-4QN208I | 147 | -4 | Lead-Free PQFP | 208 | IND | 6.1K |
| LFEC6E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 6.1K |
| LFEC6E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC10E-3FN484I | 288 | -3 | Lead-Free fpBGA | 484 | IND | 10.2K |
| LFEC10E-4FN484I | 288 | -4 | Lead-Free fpBGA | 484 | IND | 10.2K |
| LFEC10E-3FN256I | 195 | -3 | Lead-Free fpBGA | 256 | IND | 10.2K |
| LFEC10E-4FN256I | 195 | -4 | Lead-Free fpBGA | 256 | IND | 10.2K |
| LFEC10E-3QN208I | 147 | -3 | Lead-Free PQFP | 208 | IND | 10.2K |
| LFEC10E-4QN208I | 147 | -4 | Lead-Free PQFP | 208 | IND | 10.2K |