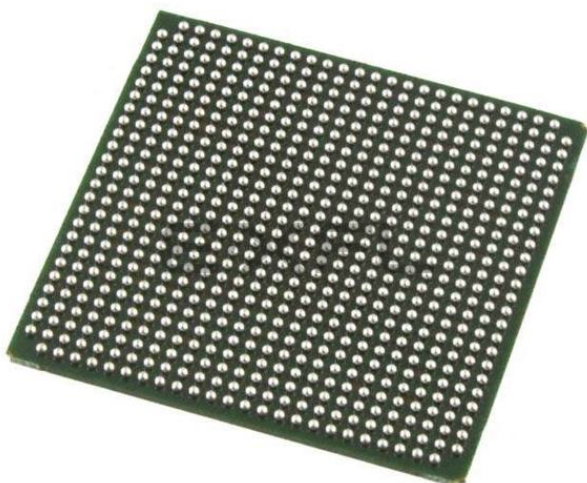




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

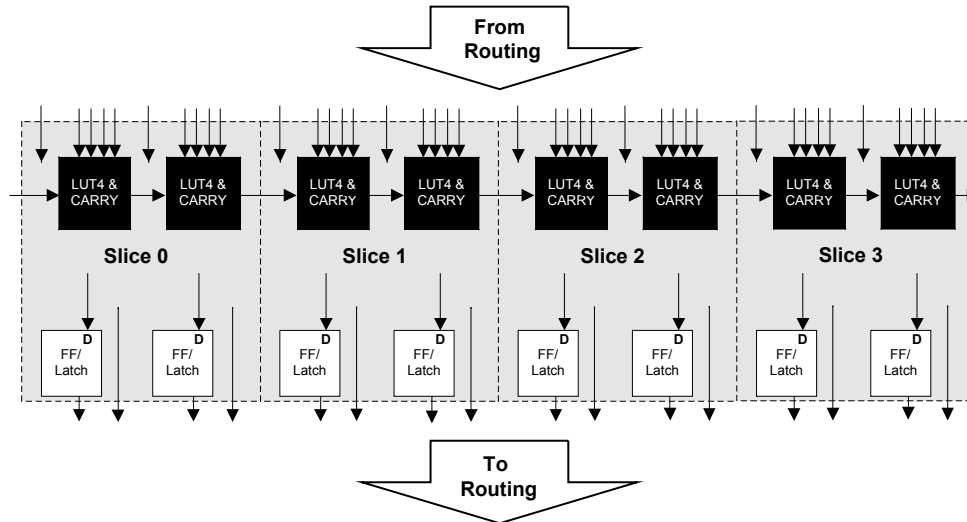
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	19700
Total RAM Bits	434176
Number of I/O	400
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec20e-4fn672i

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-8. Per Quadrant Primary Clock Selection

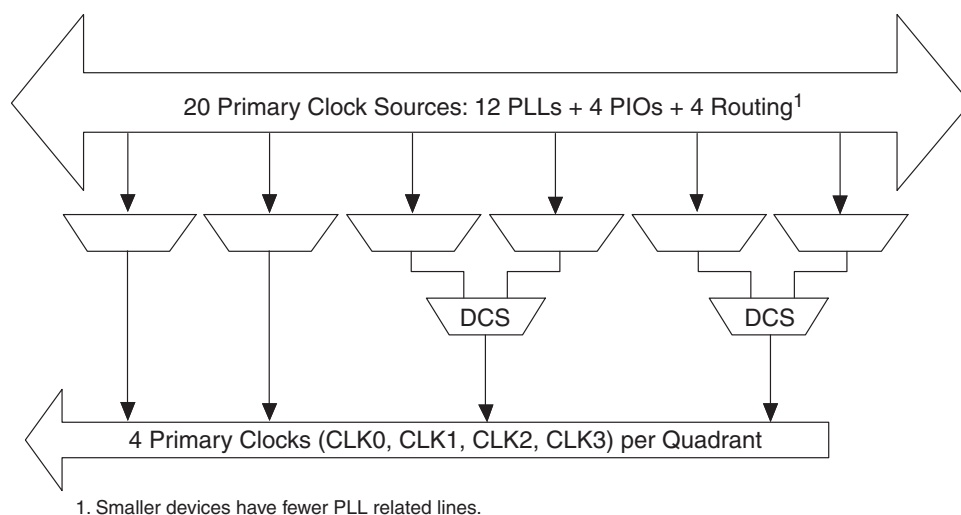


Figure 2-9. Per Quadrant Secondary Clock Selection

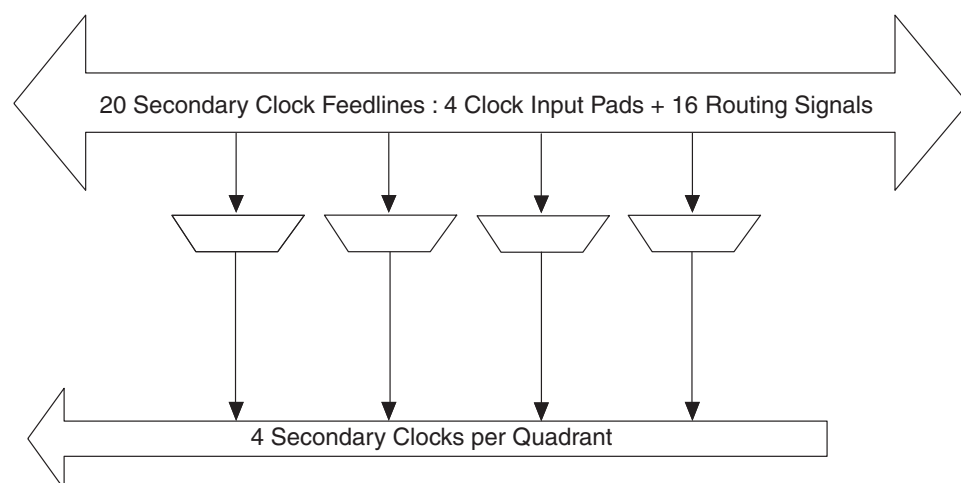
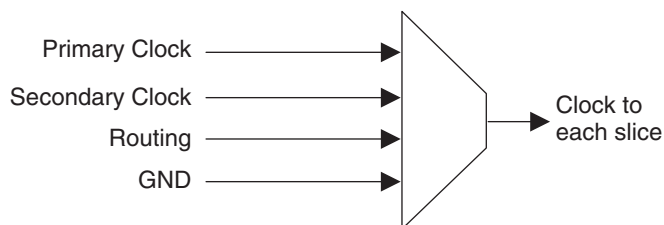


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-27 shows the input register waveforms for DDR operation and Figure 2-28 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Diagram

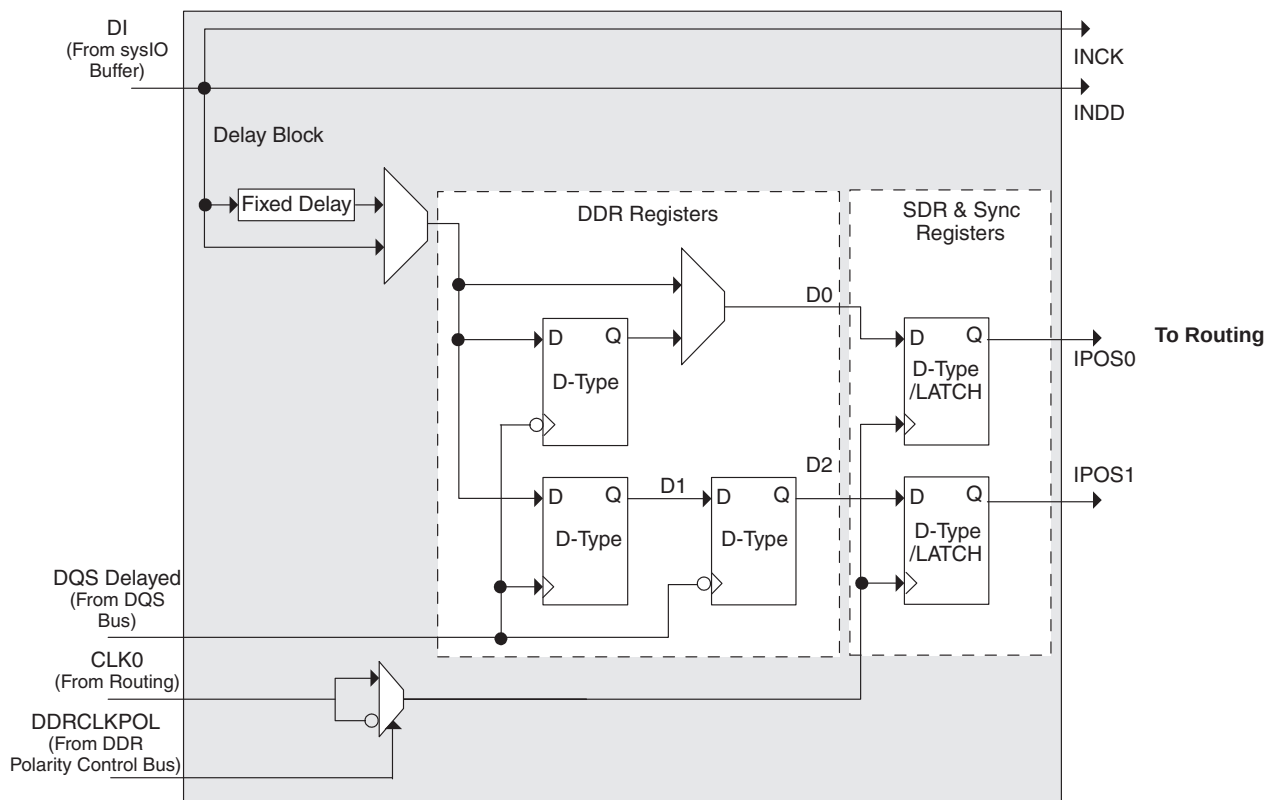


Figure 2-29. Output Register Block

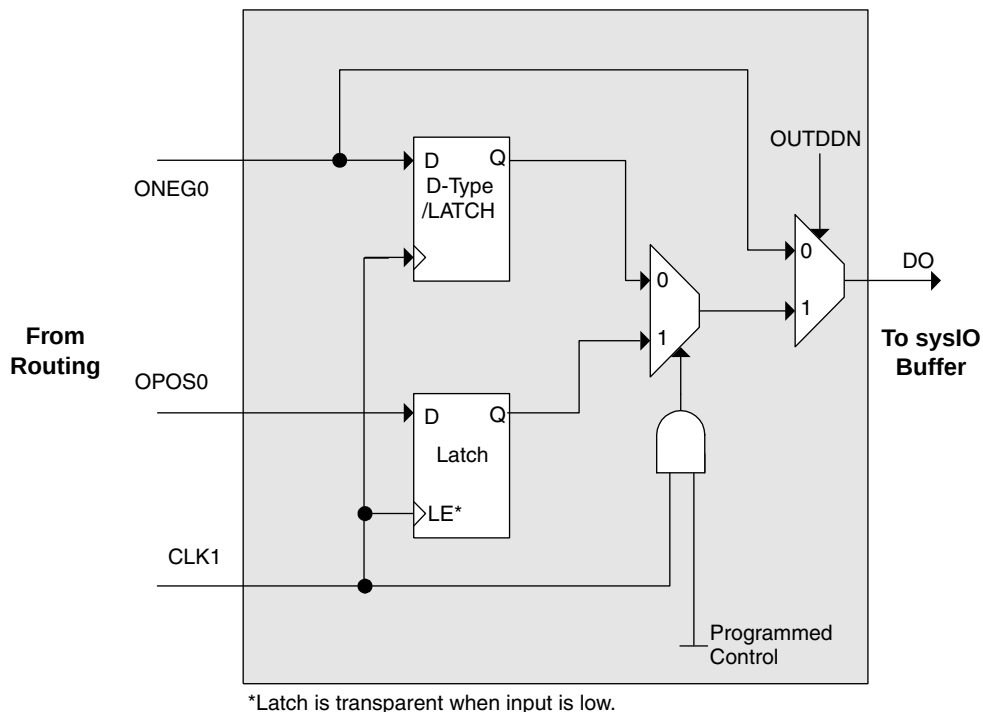
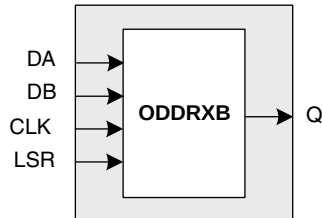


Figure 2-30. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Initialization Supply Current^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Symbol	Parameter	Devices	Typ. ⁶	Units
I _{CC}	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFEC6/LFEC6	50	mA
		LFEC10/LFEC10	60	mA
		LFEC15/LFEC15	70	mA
		LFEC20/LFEC20	150	mA
		LFEC33/LFEC33	220	mA
I _{CCAUX}	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFEC6/LFEC6	30	mA
		LFEC10/LFEC10	35	mA
		LFEC15/LFEC15	35	mA
		LFEC20/LFEC20	40	mA
		LFEC33/LFEC33	40	mA
I _{CCPLL}	PLL Power Supply Current		12	mA
I _{CCIO}	Bank Power Supply Current ⁷	LFEC1	4	mA
		LFEC3	5	mA
		LFEC6/LFEC6	6	mA
		LFEC10/LFEC10	6	mA
		LFEC15/LFEC15	7	mA
		LFEC20/LFEC20	8	mA
		LFEC33/LFEC33	8	mA
I _{CCJ}	V _{CCJ} Power Supply Current		20	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.

6. T_J=25°C, power supplies at nominal voltage.

7. Per bank.

Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables: T_J °C.

Table 3-5. Delay Derating Table for Internal Blocks

T_J °C Commercial	T_J °C Industrial	Power Supply Voltage		
		1.14V	1.2V	1.26V
—	-40	0.82	0.77	0.71
—	-25	0.82	0.76	0.71
0	20	0.89	0.83	0.78
25	45	0.93	0.87	0.81
85	105	1.00	0.94	0.89

LatticeECP/EC External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	200	95	166	95	133	MHz
Primary and Secondary Clock⁶									
$f_{MAX_PRI}^2$	Frequency for Primary Clock Tree	All	—	420	—	378	—	340	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	All	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA. Loading of 0 pF.

2. Using LVDS I/O standard.

3. DDR timing numbers based on SSTL I/O.

4. DDR specifications are characterized but not tested.

5. UI is average bit period.

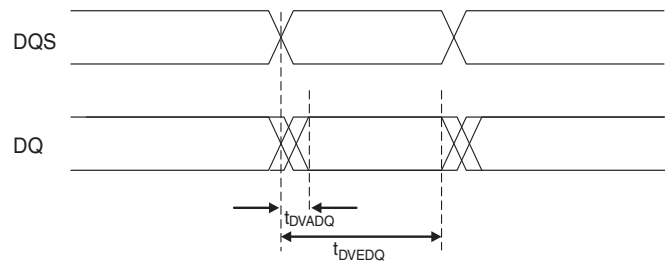
6. Based on a single primary clock.

7. These timing numbers were generated using ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

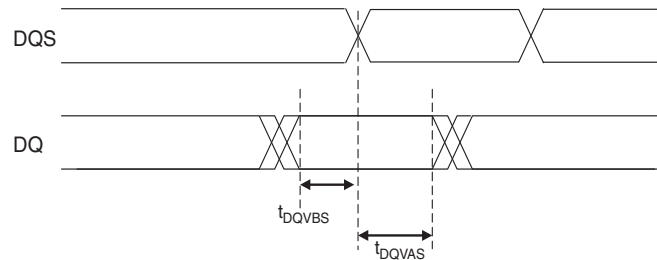
Timing v.G 0.30

Figure 3-5. DDR Timings

DQ and DQS Read Timings



DQ and DQS Write Timings



LatticeECP/EC Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_II	HSTL_15 class II	0.10	0.12	0.14	ns
HSTL15_III	HSTL_15 class III	0.10	0.12	0.14	ns
HSTL15D_I	Differential HSTL 15 class I	0.08	0.10	0.11	ns
HSTL15D_III	Differential HSTL 15 class III	0.10	0.12	0.14	ns
SSTL33_I	SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33_II	SSTL_3 class II	0.40	0.48	0.56	ns
SSTL33D_I	Differential SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33D_II	Differential SSTL_3 class II	0.40	0.48	0.56	ns
SSTL25_I	SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25_II	SSTL_2 class II	0.25	0.30	0.35	ns
SSTL25D_I	Differential SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25D_II	Differential SSTL_2 class II	0.25	0.30	0.35	ns
SSTL18_I	SSTL_1.8 class I	0.01	0.01	0.01	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.01	0.01	0.01	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.09	0.11	0.13	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.07	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.03	-0.04	-0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.36	0.43	0.51	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.28	0.33	0.39	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.09	0.11	0.13	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.07	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	-0.03	-0.04	-0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.36	0.43	0.51	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.28	0.33	0.39	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.18	0.21	0.25	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.10	0.12	0.14	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.22	0.26	0.31	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.14	0.16	0.19	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.15	0.18	0.21	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.06	0.08	0.09	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.01	0.01	0.01	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.16	0.19	0.22	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.26	0.31	0.36	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.04	0.04	0.05	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.36	0.43	0.50	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.08	0.10	0.11	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	0.36	0.43	0.50	ns
PCI33	PCI33	1.05	1.26	1.46	ns

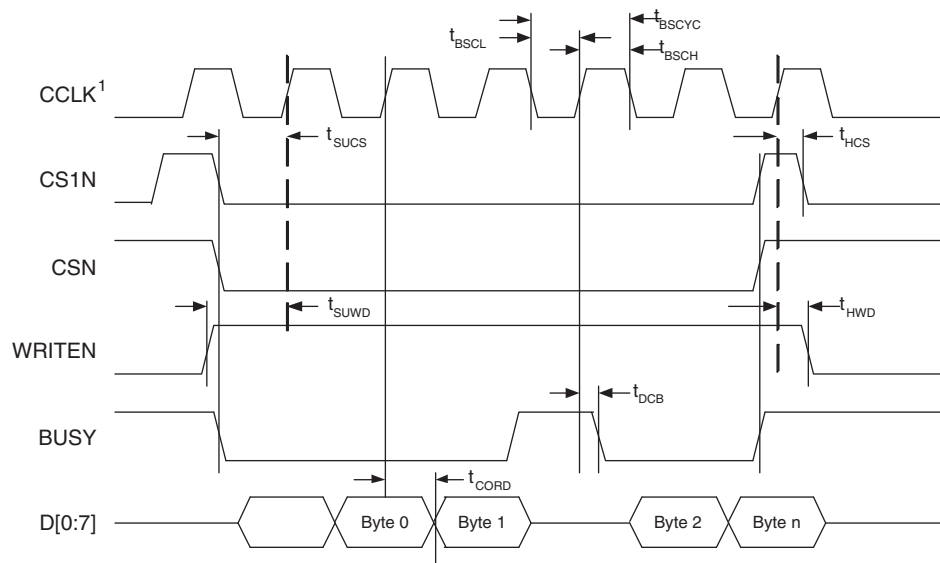
1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Conditions table of this document.

3. All other standards according to the appropriate specification.

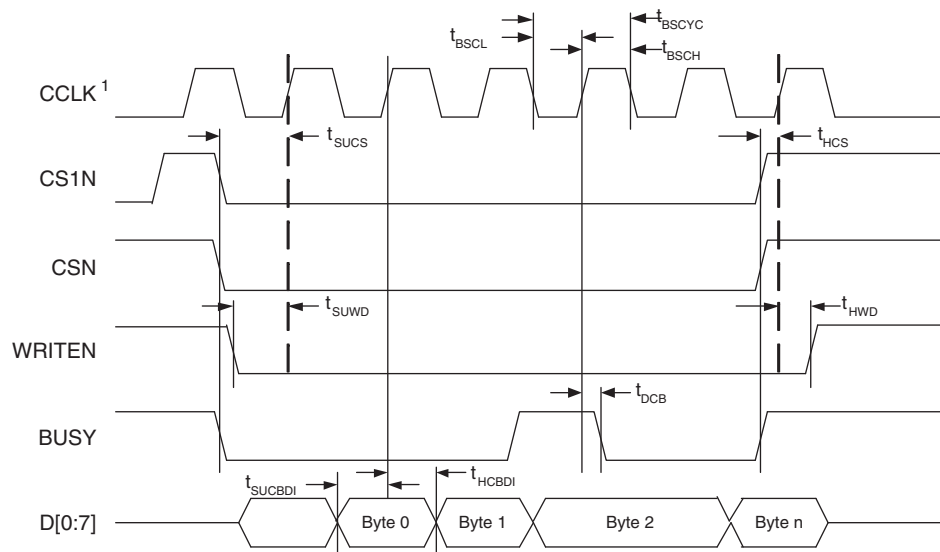
Timing v.G 0.30

Figure 3-12. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-13. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			NC	-		
6	NC	-			NC	-		
7	NC	-			PL3B	7		
8	NC	-			PL4A	7	T	
9	NC	-			PL4B	7	C	
10	NC	-			PL5A	7	T	
11	NC	-			PL5B	7	C	
12	NC	-			PL6A	7	T	LDQS6
13	NC	-			VCCIO7	7		
14	NC	-			PL6B	7	C	
15	PL3A	7	T		PL7A	7	T	
16	PL3B	7	C		PL7B	7	C	
17	PL4A	7	T		PL8A	7	T	
18	NC	-			NC	-		
19	PL4B	7	C		PL8B	7	C	
20	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
21	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
22	NC	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	NC	-			NC	-		
25	NC	-			NC	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LLM0_PLLT_IN_A
34	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LLM0_PLLC_IN_A
35	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LLM0_PLLT_FB_A
36	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL9A	6	T		PL13A	6	T	
39	PL9B	6	C		PL13B	6	C	
40	PL10A	6	T		PL14A	6	T	
41	GND6	6			GND6	6		
42	PL10B	6	C		PL14B	6	C	

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
43	PL11A	6	T	LDQS11	PL15A	6	T	LDQS15
44	PL11B	6	C		PL15B	6	C	
45	PL12A	6	T		PL16A	6	T	
46	PL12B	6	C		PL16B	6	C	
47	PL13A	6	T		PL17A	6	T	
48	PL13B	6	C		PL17B	6	C	
49	PL14A	6	T	VREF1_6	PL18A	6	T	VREF1_6
50	PL14B	6	C	VREF2_6	PL18B	6	C	VREF2_6
51	VCCIO6	6			VCCIO6	6		
52*	GND5 GND6	-			GND5 GND6	-		
53	VCCIO5	5			VCCIO5	5		
54	NC	-			PB2A	5	T	
55	NC	-			PB2B	5	C	
56	NC	-			PB3A	5	T	
57	NC	-			PB3B	5	C	
58	NC	-			PB4A	5	T	
59	NC	-			PB4B	5	C	
60	NC	-			PB5A	5	T	
61	NC	-			PB5B	5	C	
62	NC	-			PB6A	5	T	BDQS6
63	NC	-			PB6B	5	C	
64	NC	-			VCCIO5	5		
65	PB2A	5	T		PB10A	5	T	
66	PB2B	5	C		PB10B	5	C	
67	PB3A	5	T		PB11A	5	T	
68	PB3B	5	C		PB11B	5	C	
69	PB4A	5	T		PB12A	5	T	
70	PB4B	5	C		PB12B	5	C	
71	PB5A	5	T		PB13A	5	T	
72	NC	-			GND5	5		
73	PB5B	5	C		PB13B	5	C	
74	VCCIO5	5			VCCIO5	5		
75	PB6A	5	T	BDQS6	PB14A	5	T	BDQS14
76	PB6B	5	C		PB14B	5	C	
77	PB7A	5	T		PB15A	5	T	
78	PB7B	5	C		PB15B	5	C	
79	PB8A	5	T	VREF2_5	PB16A	5	T	VREF2_5
80	PB8B	5	C	VREF1_5	PB16B	5	C	VREF1_5
81	PB9A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
82	GND5	5			GND5	5		
83	PB9B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
84	VCCAUX	-			VCCAUX	-		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
D7	PT11B	0	C		PT11B	0	C	
C7	PT11A	0	T		PT11A	0	T	
A7	PT10B	0	C		PT10B	0	C	
A6	PT10A	0	T		PT10A	0	T	
E7	PT9B	0	C		PT9B	0	C	
GND	GND0	0			GND0	0		
E6	PT9A	0	T		PT9A	0	T	
D6	PT8B	0	C		PT8B	0	C	
C6	PT8A	0	T		PT8A	0	T	
B6	PT7B	0	C		PT7B	0	C	
B5	PT7A	0	T		PT7A	0	T	
A5	PT6B	0	C		PT6B	0	C	
A4	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
A3	PT5B	0	C		PT5B	0	C	
A2	PT5A	0	T		PT5A	0	T	
B2	PT4B	0	C		PT4B	0	C	
B3	PT4A	0	T		PT4A	0	T	
D5	PT3B	0	C		PT3B	0	C	
C5	PT3A	0	T		PT3A	0	T	
C4	PT2B	0	C		PT2B	0	C	
B4	PT2A	0	T		PT2A	0	T	
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
A10	PT25B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT25A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
C9	PT24B	0	C	VREF1_0	PT24B	0	C	VREF1_0
B9	PT24A	0	T	VREF2_0	PT24A	0	T	VREF2_0
E9	PT23B	0	C		PT23B	0	C	
D9	PT23A	0	T		PT23A	0	T	
D8	PT22B	0	C		PT22B	0	C	
C8	PT22A	0	T	TDQS22	PT22A	0	T	TDQS22
A9	PT21B	0	C		PT21B	0	C	
GND	GND0	0			GND0	0		
A8	PT21A	0	T		PT21A	0	T	
B8	PT20B	0	C		PT20B	0	C	
B7	PT20A	0	T		PT20A	0	T	
D7	PT19B	0	C		PT19B	0	C	
C7	PT19A	0	T		PT19A	0	T	
A7	PT18B	0	C		PT18B	0	C	
A6	PT18A	0	T		PT18A	0	T	
E7	PT17B	0	C		PT17B	0	C	
GND	GND0	0			GND0	0		
E6	PT17A	0	T		PT17A	0	T	
D6	PT16B	0	C		PT16B	0	C	
C6	PT16A	0	T		PT16A	0	T	
B6	PT15B	0	C		PT15B	0	C	
B5	PT15A	0	T		PT15A	0	T	
A5	PT14B	0	C		PT14B	0	C	
A4	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A3	PT13B	0	C		PT13B	0	C	
-	GND0	0			GND0	0		
A2	PT13A	0	T		PT13A	0	T	
B2	PT12B	0	C		PT12B	0	C	
B3	PT12A	0	T		PT12A	0	T	
D5	PT11B	0	C		PT11B	0	C	
C5	PT11A	0	T		PT11A	0	T	
C4	PT10B	0	C		PT10B	0	C	
B4	PT10A	0	T		PT10A	0	T	
GND	GND0	0			GND0	0		
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		

LFECF/EC6, LFECF/EC10, LFECF/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECF/EC6					LFECF/EC10					LFECF/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND	GND5	5			GND	GND5	5		
V7	NC	-			V7	PB2A	5	T		V7	PB2A	5	T	
T6	NC	-			T6	PB2B	5	C		T6	PB2B	5	C	
V8	NC	-			V8	PB3A	5	T		V8	PB3A	5	T	
U7	NC	-			U7	PB3B	5	C		U7	PB3B	5	C	
W5	NC	-			W5	PB4A	5	T		W5	PB4A	5	T	
U6	NC	-			U6	PB4B	5	C		U6	PB4B	5	C	
AA3	NC	-			AA3	PB5A	5	T		AA3	PB5A	5	T	
AB3	NC	-			AB3	PB5B	5	C		AB3	PB5B	5	C	
Y6	NC	-			Y6	PB6A	5	T	BDQS6	Y6	PB6A	5	T	BDQS6
V6	NC	-			V6	PB6B	5	C		V6	PB6B	5	C	
AA5	NC	-			AA5	PB7A	5	T		AA5	PB7A	5	T	
W6	NC	-			W6	PB7B	5	C		W6	PB7B	5	C	
Y5	NC	-			Y5	PB8A	5	T		Y5	PB8A	5	T	
Y4	NC	-			Y4	PB8B	5	C		Y4	PB8B	5	C	
AA4	NC	-			AA4	PB9A	5	T		AA4	PB9A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
AB4	NC	-			AB4	PB9B	5	C		AB4	PB9B	5	C	
Y7	PB2A	5	T		Y7	PB10A	5	T		Y7	PB10A	5	T	
W8	PB2B	5	C		W8	PB10B	5	C		W8	PB10B	5	C	
W7	PB3A	5	T		W7	PB11A	5	T		W7	PB11A	5	T	
U8	PB3B	5	C		U8	PB11B	5	C		U8	PB11B	5	C	
W9	PB4A	5	T		W9	PB12A	5	T		W9	PB12A	5	T	
U9	PB4B	5	C		U9	PB12B	5	C		U9	PB12B	5	C	
Y8	PB5A	5	T		Y8	PB13A	5	T		Y8	PB13A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
Y9	PB5B	5	C		Y9	PB13B	5	C		Y9	PB13B	5	C	
V9	PB6A	5	T	BDQS6	V9	PB14A	5	T	BDQS14	V9	PB14A	5	T	BDQS14
T9	PB6B	5	C		T9	PB14B	5	C		T9	PB14B	5	C	
W10	PB7A	5	T		W10	PB15A	5	T		W10	PB15A	5	T	
U10	PB7B	5	C		U10	PB15B	5	C		U10	PB15B	5	C	
V10	PB8A	5	T		V10	PB16A	5	T		V10	PB16A	5	T	
T10	PB8B	5	C		T10	PB16B	5	C		T10	PB16B	5	C	
AA6	PB9A	5	T		AA6	PB17A	5	T		AA6	PB17A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB5	PB9B	5	C		AB5	PB17B	5	C		AB5	PB17B	5	C	
AA8	PB10A	5	T		AA8	PB18A	5	T		AA8	PB18A	5	T	
AA7	PB10B	5	C		AA7	PB18B	5	C		AA7	PB18B	5	C	
AB6	PB11A	5	T		AB6	PB19A	5	T		AB6	PB19A	5	T	
AB7	PB11B	5	C		AB7	PB19B	5	C		AB7	PB19B	5	C	
Y10	PB12A	5	T		Y10	PB20A	5	T		Y10	PB20A	5	T	
W11	PB12B	5	C		W11	PB20B	5	C		W11	PB20B	5	C	
AB8	PB13A	5	T		AB8	PB21A	5	T		AB8	PB21A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB9	PB13B	5	C		AB9	PB21B	5	C		AB9	PB21B	5	C	
AA10	PB14A	5	T	BDQS14	AA10	PB22A	5	T	BDQS22	AA10	PB22A	5	T	BDQS22
AA9	PB14B	5	C		AA9	PB22B	5	C		AA9	PB22B	5	C	
Y11	PB15A	5	T		Y11	PB23A	5	T		Y11	PB23A	5	T	
AA11	PB15B	5	C		AA11	PB23B	5	C		AA11	PB23B	5	C	
V11	PB16A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
K3	PL21A	7	T		K3	PL33A	7	T	
K2	PL21B	7	C		K2	PL33B	7	C	
J1	PL22A	7	T	PCLKT7_0	J1	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
K1	PL22B	7	C	PCLKC7_0	K1	PL34B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6		
L4	PL24A	6	T		L4	PL36A	6	T	
L5	PL24B	6	C		L5	PL36B	6	C	
L2	PL25A	6	T		L2	PL37A	6	T	
L1	PL25B	6	C		L1	PL37B	6	C	
M4	PL26A	6	T		M4	PL38A	6	T	
M5	PL26B	6	C		M5	PL38B	6	C	
M1	PL27A	6	T		M1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
M2	PL27B	6	C		M2	PL39B	6	C	
N3	PL28A	6	T	LDQS28	N3	PL40A	6	T	LDQS40
M3	PL28B	6	C		M3	PL40B	6	C	
N5	PL29A	6	T		N5	PL41A	6	T	
N4	PL29B	6	C		N4	PL41B	6	C	
N1	PL30A	6	T		N1	PL42A	6	T	
N2	PL30B	6	C		N2	PL42B	6	C	
P1	PL31A	6	T		P1	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
P2	PL31B	6	C		P2	PL43B	6	C	
R6	PL32A	6	T		R6	PL44A	6	T	
P5	PL32B	6	C		P5	PL44B	6	C	
P3	PL33A	6	T		P3	PL45A	6	T	
P4	PL33B	6	C		P4	PL45B	6	C	
R1	PL34A	6	T		R1	PL46A	6	T	
R2	PL34B	6	C		R2	PL46B	6	C	
R5	PL35A	6	T		R5	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
R4	PL35B	6	C		R4	PL47B	6	C	
T1	PL36A	6	T	LDQS36	T1	PL48A	6	T	LDQS48
T2	PL36B	6	C		T2	PL48B	6	C	
R3	PL37A	6	T		R3	PL49A	6	T	
T3	PL37B	6	C		T3	PL49B	6	C	
GND	GND6	6			GND	GND6	6		
T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6		
V1	PL41A	6	T	LLM0_PLLT_IN_A	V1	PL53A	6	T	LLM0_PLLT_IN_A

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

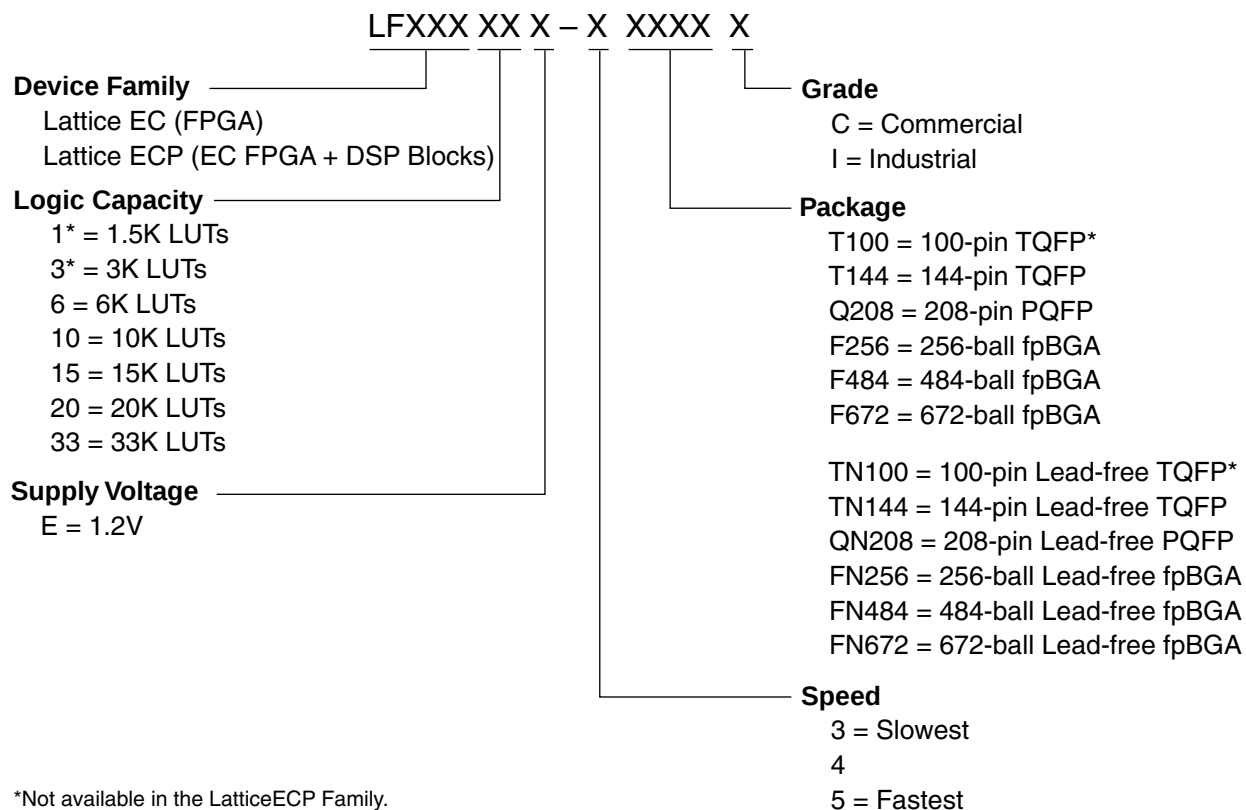
LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y6	NC	-			Y6	PL62A	6	T	
W7	NC	-			W7	PL62B	6	C	
AA4	NC	-			AA4	PL63A	6	T	
AB3	NC	-			AB3	PL63B	6	C	
AC2	NC	-			AC2	PL64A	6	T	
-	-	-			GND	GND6	6		
AC3	NC	-			AC3	PL64B	6	C	
AA5	NC	-			AA5	PL65A	6	T	LDQS65
AB5	NC	-			AB5	PL65B	6	C	
AD3	NC	-			AD3	PL66A	6	T	
AD2	NC	-			AD2	PL66B	6	C	
AE1	NC	-			AE1	PL67A	6	T	
AD1	NC	-			AD1	PL67B	6	C	
AB4	PL48A	6	T	VREF1_6	AB4	PL68A	6	T	VREF1_6
AC4	PL48B	6	C	VREF2_6	AC4	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND5	5		
AB6	PB2A	5	T		AB6	PB2A	5	T	
AA6	PB2B	5	C		AA6	PB2B	5	C	
AC7	PB3A	5	T		AC7	PB3A	5	T	
Y8	PB3B	5	C		Y8	PB3B	5	C	
AB7	PB4A	5	T		AB7	PB4A	5	T	
AA7	PB4B	5	C		AA7	PB4B	5	C	
AC6	PB5A	5	T		AC6	PB5A	5	T	
AC5	PB5B	5	C		AC5	PB5B	5	C	
AB8	PB6A	5	T	BDQS6	AB8	PB6A	5	T	BDQS6
AC8	PB6B	5	C		AC8	PB6B	5	C	
AE2	PB7A	5	T		AE2	PB7A	5	T	
AA8	PB7B	5	C		AA8	PB7B	5	C	
AF2	PB8A	5	T		AF2	PB8A	5	T	
Y9	PB8B	5	C		Y9	PB8B	5	C	
AD5	PB9A	5	T		AD5	PB9A	5	T	
GND	GND5	5			GND	GND5	5		
AD4	PB9B	5	C		AD4	PB9B	5	C	
AD8	PB10A	5	T		AD8	PB10A	5	T	
AC9	PB10B	5	C		AC9	PB10B	5	C	
AE3	PB11A	5	T		AE3	PB11A	5	T	
AB9	PB11B	5	C		AB9	PB11B	5	C	
AF3	PB12A	5	T		AF3	PB12A	5	T	
AD9	PB12B	5	C		AD9	PB12B	5	C	
AE4	PB13A	5	T		AE4	PB13A	5	T	
GND	GND5	5			GND	GND5	5		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

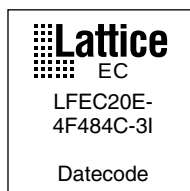
LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U12	GND	-			U12	GND	-		
U13	GND	-			U13	GND	-		
U14	GND	-			U14	GND	-		
U15	GND	-			U15	GND	-		
U16	GND	-			U16	GND	-		
U17	GND	-			U17	GND	-		
H10	VCC	-			H10	VCC	-		
H11	VCC	-			H11	VCC	-		
H16	VCC	-			H16	VCC	-		
H17	VCC	-			H17	VCC	-		
H18	VCC	-			H18	VCC	-		
H19	VCC	-			H19	VCC	-		
H8	VCC	-			H8	VCC	-		
H9	VCC	-			H9	VCC	-		
J18	VCC	-			J18	VCC	-		
J9	VCC	-			J9	VCC	-		
K8	VCC	-			K8	VCC	-		
L19	VCC	-			L19	VCC	-		
M19	VCC	-			M19	VCC	-		
N7	VCC	-			N7	VCC	-		
R20	VCC	-			R20	VCC	-		
R7	VCC	-			R7	VCC	-		
T19	VCC	-			T19	VCC	-		
V18	VCC	-			V18	VCC	-		
V8	VCC	-			V8	VCC	-		
V9	VCC	-			V9	VCC	-		
W10	VCC	-			W10	VCC	-		
W11	VCC	-			W11	VCC	-		
W16	VCC	-			W16	VCC	-		
W17	VCC	-			W17	VCC	-		
W18	VCC	-			W18	VCC	-		
W19	VCC	-			W19	VCC	-		
W8	VCC	-			W8	VCC	-		
W9	VCC	-			W9	VCC	-		
H12	VCCIO0	0			H12	VCCIO0	0		
H13	VCCIO0	0			H13	VCCIO0	0		
J10	VCCIO0	0			J10	VCCIO0	0		
J11	VCCIO0	0			J11	VCCIO0	0		
J12	VCCIO0	0			J12	VCCIO0	0		
J13	VCCIO0	0			J13	VCCIO0	0		
H14	VCCIO1	1			H14	VCCIO1	1		
H15	VCCIO1	1			H15	VCCIO1	1		

Part Number Description



Ordering Information

Note: LatticeECP/EC devices are dual marked. For example, the commercial speed grade LFEC20E-4F484C is also marked with industrial grade -3I (LFEC20E-3F484I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:





LatticeECP/EC Family Data Sheet

Revision History

September 2012

Data Sheet DS1000

Revision History

Date	Version	Section	Change Summary
June 2004	01.0	—	Initial release.
August 2004	01.1	Introduction	Added new device LFECP/LFEC33 in Table 1-1.
		Architecture	Added New device LFECP/LFEC33 in Tables 2-9, 2-10 and 2-11.
		DC & Switching Characteristics	Added New device LFECP/LFEC33 on Supply current (Standby) tables. Added New device LFECP/LFEC33 on Initialization Supply current tables.
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section. Added EC33, ECP33 device: Industrial and Commercial to Part Number table. Corrected I/O counts in the part number tables for 100/144 TQFP and 208 PQFP packages to match Table 1-1 on page 1.
November 2004	01.3	Introduction	Changed DDR333 (166MHz) to DDR400 (200MHz)
			Added “RSDS” offering to the Features list: Flexible I/O Buffer
		Architecture	Added information about Secondary Clock Sources
			Added information about DCS
			Added a section on “Recommended Power-up Sequence”
			Updated Figure 2-24 “DQS Routing”
			Added DSP Block performance numbers to Table 2-11
			Added another row for RSDS in Table 2-13 and Table 2-14
		DC & Switching Characteristics	Updated new timing numbers
			Added numbers to derating table
			Added DC conditions to RSDS table
			Changed LVDS Max. V_{CCIO} to 2.625
			Added a row for RSDS in “Operating Condition” table
			Updated standby and initialization current table
			Added figure 3-12: sysConfig SPI port sequence
			Added DDR Timing Table and DDR Timings Figure 3-6
		Pinout Information	Added LFECP/EC6 to Pin Information
			Added LFECP/EC6 to Power Supply and NC Connections
			Added LFECP/EC6 144 TQFP Logic Signal Connections
			Added LFECP/EC6 208 PQFP Logic Signal Connections
			Added LFECP/EC6 256 fpBGA Logic Signal Connections
			Added LFECP/EC6 484 fpBGA Logic Signal Connections
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section.
			Added Part Number table for Commercial EC33.
			Added Part Number table for Commercial ECP33.
			Added Part Number table for Industrial EC33.
			Added Part Number table for Industrial ECP33.