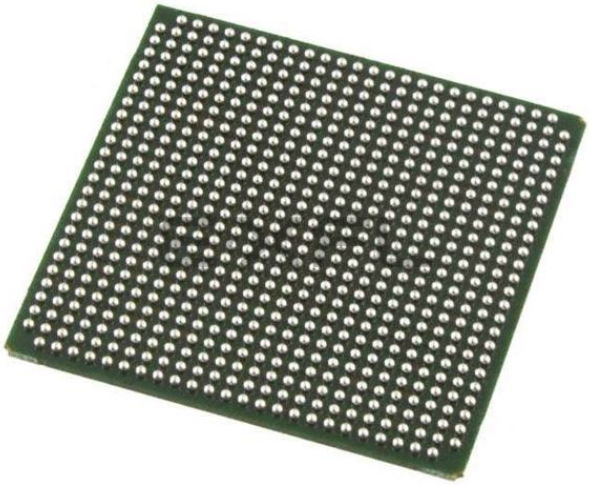

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	19700
Total RAM Bits	434176
Number of I/O	400
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec20e-5fn672c

LatticeECP/EC Family Data Sheet Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)

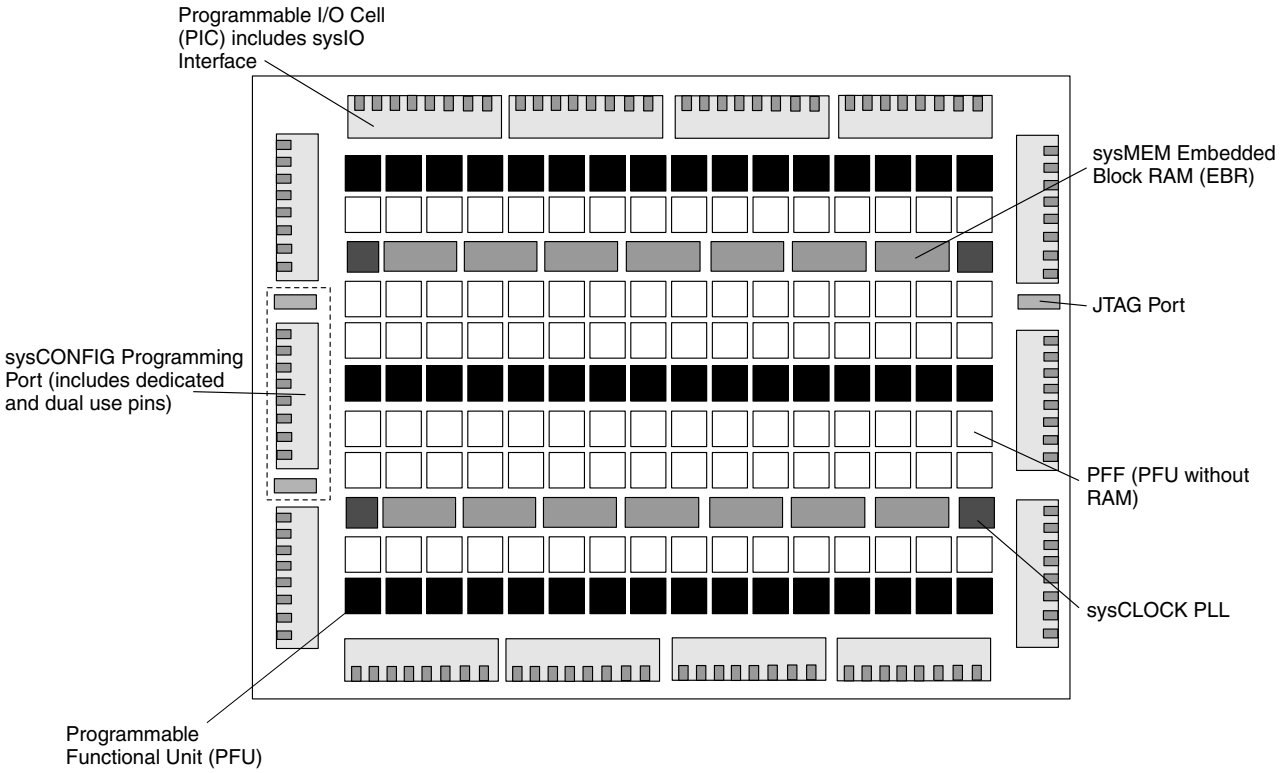


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)

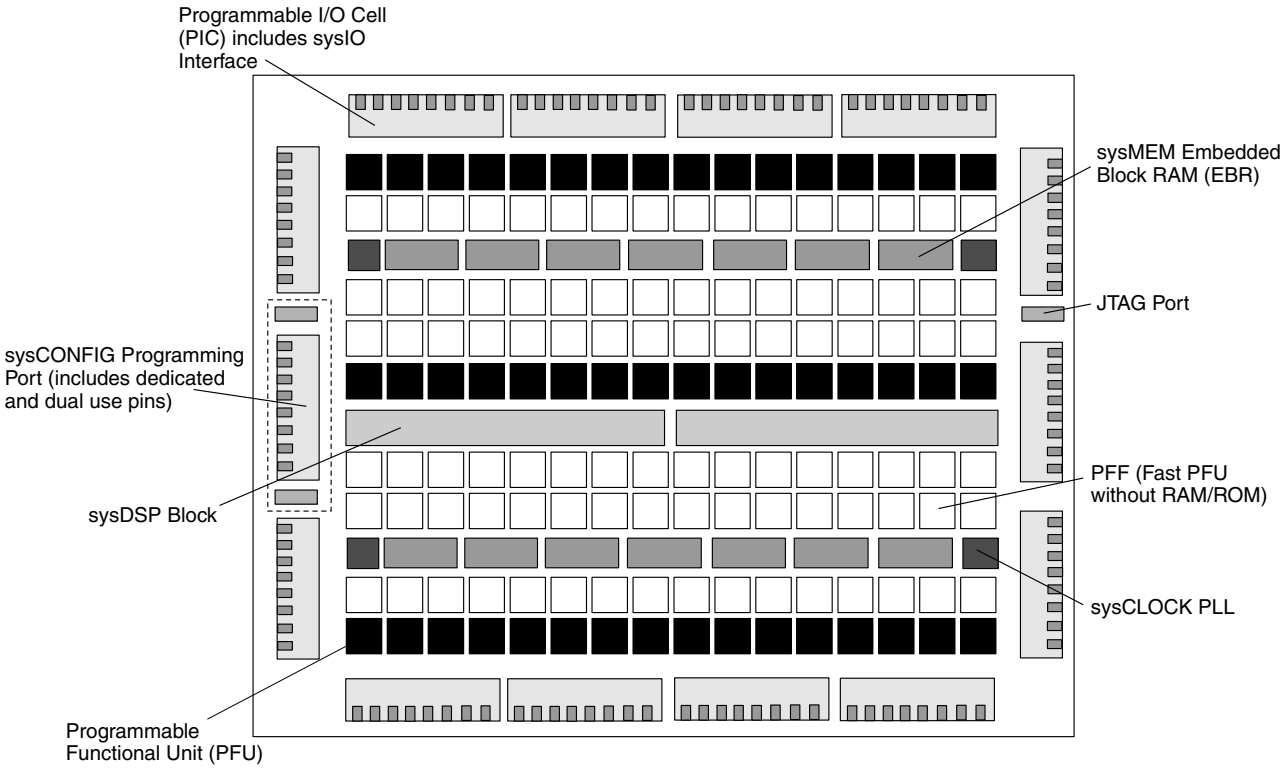
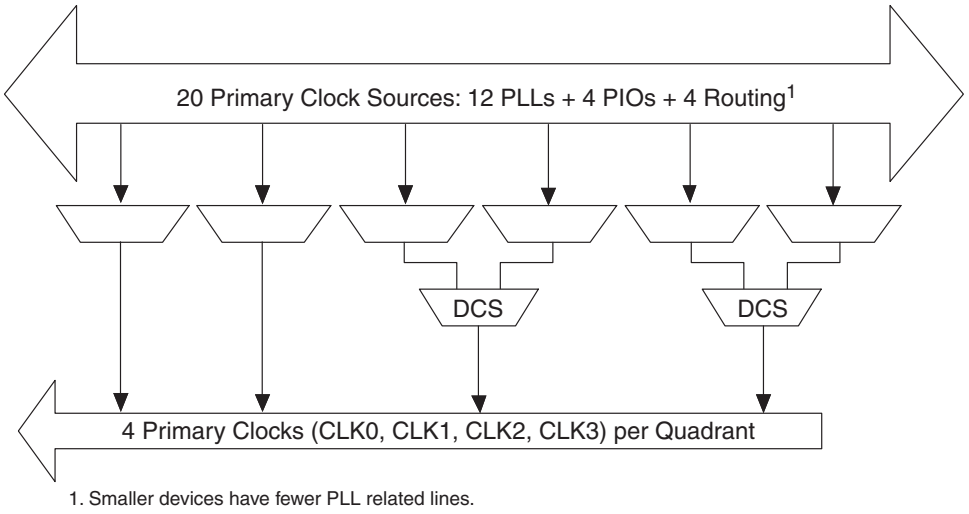


Figure 2-8. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-9. Per Quadrant Secondary Clock Selection

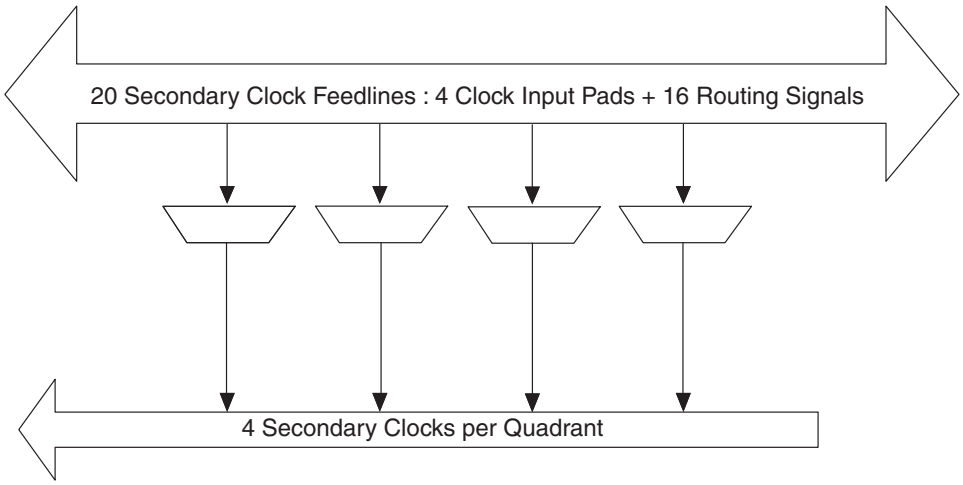
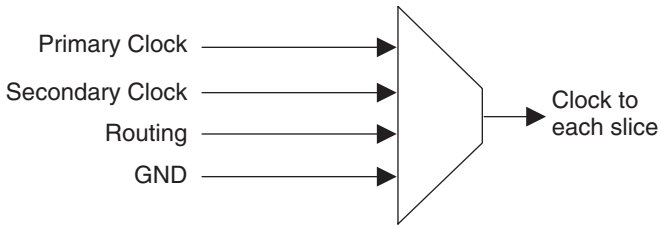


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

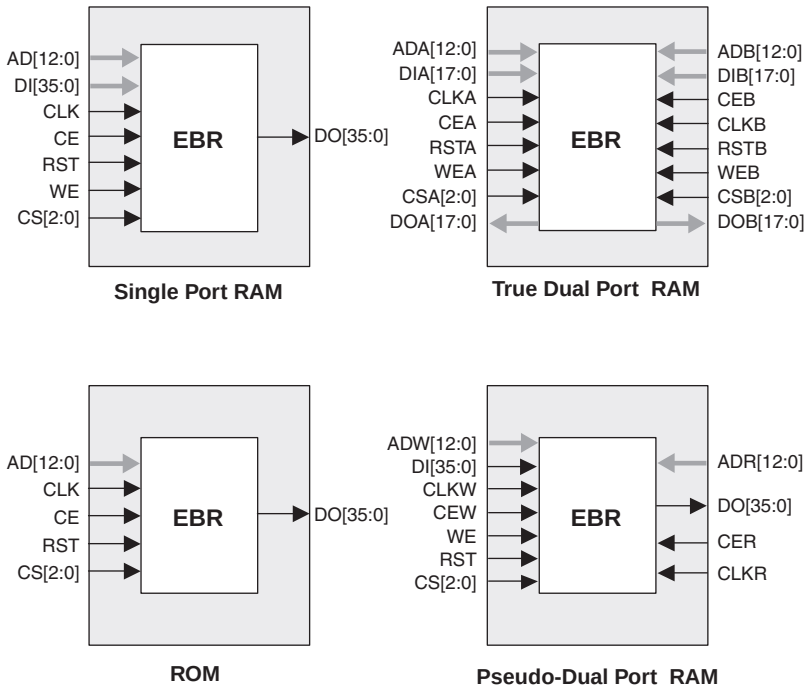
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeECP/EC family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysI/O Buffer Banks

LatticeECP/EC devices have eight sysI/O buffer banks; each is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-34 shows the eight banks and their associated supplies.

In the LatticeECP/EC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO.}$ LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold input independent of $V_{CCIO.}$ In addition to the bank V_{CCIO} supplies, the LatticeECP/EC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeECP/EC devices, some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

LatticeECP/EC External Switching Characteristics (Continued)

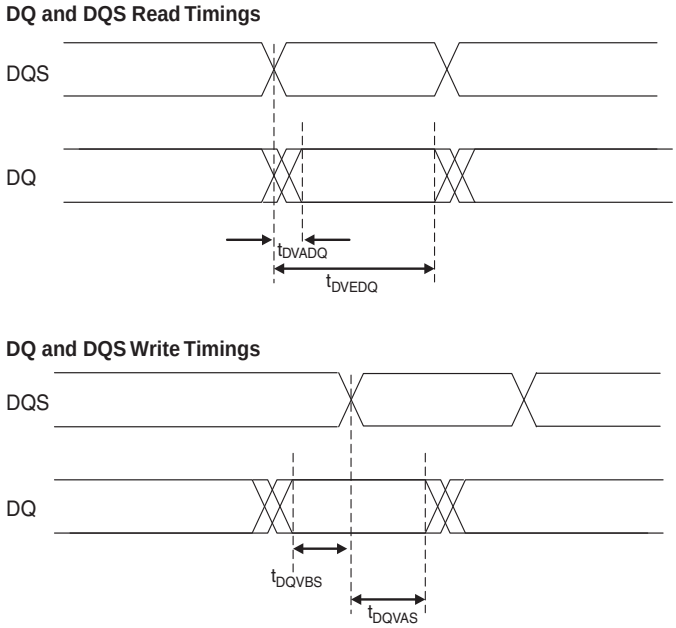
Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	200	95	166	95	133	MHz
Primary and Secondary Clock[6]									
f_{MAX_PRI}[2]	Frequency for Primary Clock Tree	All	—	420	—	378	—	340	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	All	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA. Loading of 0 pF.
2. Using LVDS I/O standard.
3. DDR timing numbers based on SSTL I/O.
4. DDR specifications are characterized but not tested.
5. UI is average bit period.
6. Based on a single primary clock.
7. These timing numbers were generated using ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.G 0.30

Figure 3-5. DDR Timings



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	210	MHz
f_{VCO}	PLL VCO Frequency		420	—	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Elected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	f_{OUT} >= 100MHz	—	—	+/- 125	ps
		f_{OUT} < 100MHz	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	—	150	µs
t_{PA}	Programmable Delay Unit		100	250	450	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

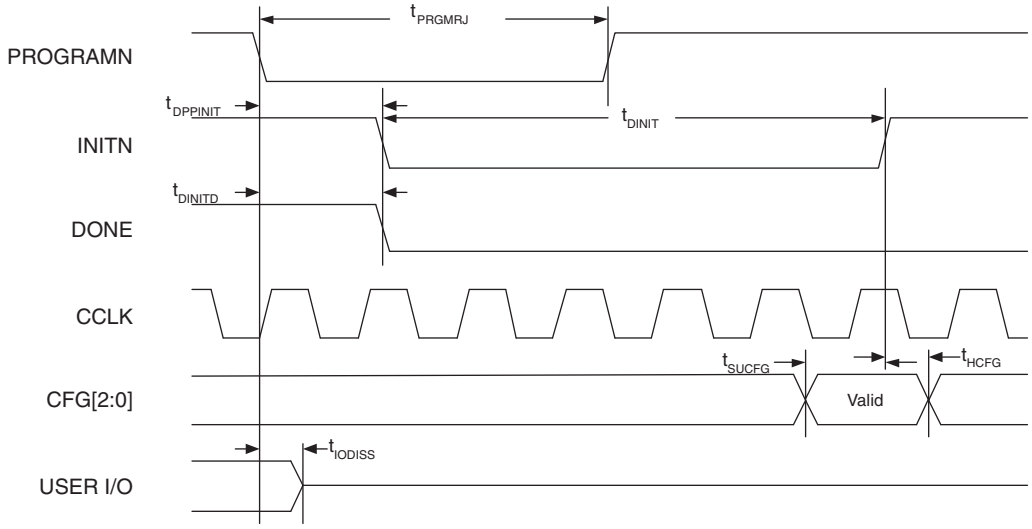
Timing v.G 0.30

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from tICFG to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

Figure 3-17. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-18. Wake-Up Timing

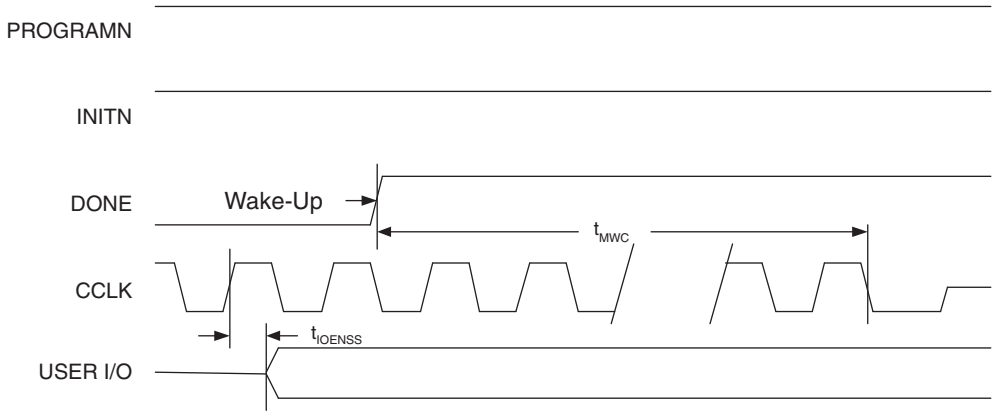
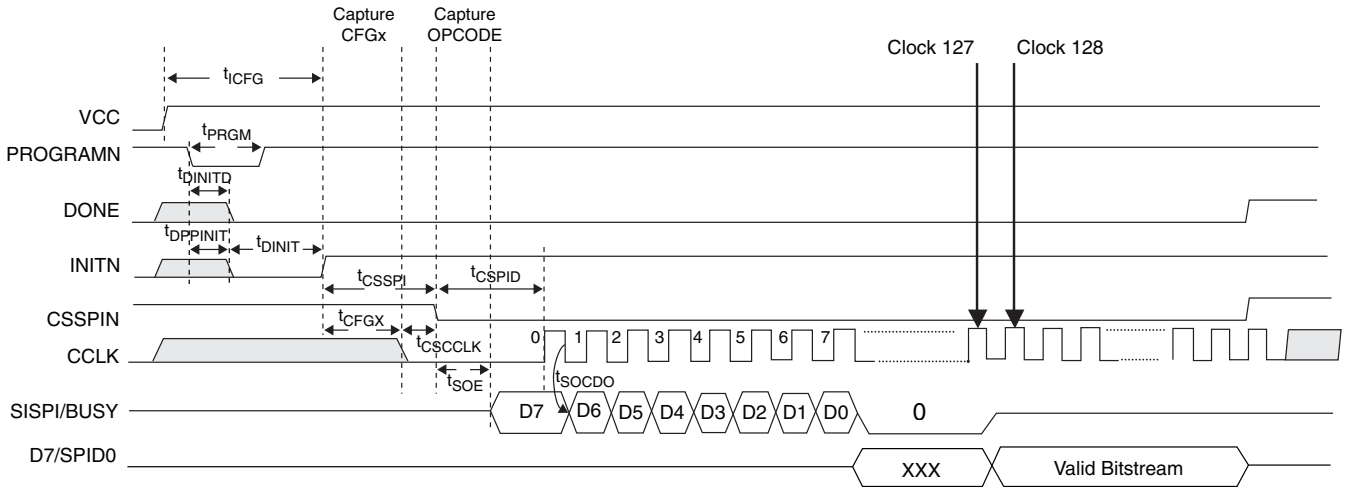


Figure 3-19. sysCONFIG SPI Port Sequence



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ

Notes:
1. “n” is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U9	PB20B	5	C		U9	PB20B	5	C	
Y8	PB21A	5	T		Y8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
Y9	PB21B	5	C		Y9	PB21B	5	C	
V9	PB22A	5	T	BDQS22	V9	PB22A	5	T	BDQS22
T9	PB22B	5	C		T9	PB22B	5	C	
W10	PB23A	5	T		W10	PB23A	5	T	
U10	PB23B	5	C		U10	PB23B	5	C	
V10	PB24A	5	T		V10	PB24A	5	T	
T10	PB24B	5	C		T10	PB24B	5	C	
AA6	PB25A	5	T		AA6	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AB5	PB25B	5	C		AB5	PB25B	5	C	
AA8	PB26A	5	T		AA8	PB26A	5	T	
AA7	PB26B	5	C		AA7	PB26B	5	C	
AB6	PB27A	5	T		AB6	PB27A	5	T	
AB7	PB27B	5	C		AB7	PB27B	5	C	
Y10	PB28A	5	T		Y10	PB28A	5	T	
W11	PB28B	5	C		W11	PB28B	5	C	
AB8	PB29A	5	T		AB8	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AB9	PB29B	5	C		AB9	PB29B	5	C	
AA10	PB30A	5	T	BDQS30	AA10	PB30A	5	T	BDQS30
AA9	PB30B	5	C		AA9	PB30B	5	C	
Y11	PB31A	5	T		Y11	PB31A	5	T	
AA11	PB31B	5	C		AA11	PB31B	5	C	
V11	PB32A	5	T	VREF2_5	V11	PB32A	5	T	VREF2_5
V12	PB32B	5	C	VREF1_5	V12	PB32B	5	C	VREF1_5
AB10	PB33A	5	T	PCLKT5_0	AB10	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AB11	PB33B	5	C	PCLKC5_0	AB11	PB33B	5	C	PCLKC5_0
Y12	PB34A	4	T	WRITEN	Y12	PB34A	4	T	WRITEN
U11	PB34B	4	C	CS1N	U11	PB34B	4	C	CS1N
W12	PB35A	4	T	VREF1_4	W12	PB35A	4	T	VREF1_4
U12	PB35B	4	C	CSN	U12	PB35B	4	C	CSN
W13	PB36A	4	T	VREF2_4	W13	PB36A	4	T	VREF2_4
U13	PB36B	4	C	D0/SPID7	U13	PB36B	4	C	D0/SPID7
AA12	PB37A	4	T	D2/SPID5	AA12	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AB12	PB37B	4	C	D1/SPID6	AB12	PB37B	4	C	D1/SPID6
T13	PB38A	4	T	BDQS38	T13	PB38A	4	T	BDQS38
V13	PB38B	4	C	D3/SPID4	V13	PB38B	4	C	D3/SPID4
W14	PB39A	4	T		W14	PB39A	4	T	
U14	PB39B	4	C	D4/SPID3	U14	PB39B	4	C	D4/SPID3

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A17	PT47A	1	T		A17	PT47A	1	T	
B15	PT46B	1	C		B15	PT46B	1	C	
A16	PT46A	1	T	TDQS46	A16	PT46A	1	T	TDQS46
A15	PT45B	1	C		A15	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
A14	PT45A	1	T		A14	PT45A	1	T	
G14	PT44B	1	C		G14	PT44B	1	C	
E15	PT44A	1	T		E15	PT44A	1	T	
D15	PT43B	1	C		D15	PT43B	1	C	
C15	PT43A	1	T		C15	PT43A	1	T	
C14	PT42B	1	C		C14	PT42B	1	C	
B14	PT42A	1	T		B14	PT42A	1	T	
A13	PT41B	1	C		A13	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
B13	PT41A	1	T		B13	PT41A	1	T	
E14	PT40B	1	C		E14	PT40B	1	C	
C13	PT40A	1	T		C13	PT40A	1	T	
F14	PT39B	1	C		F14	PT39B	1	C	
D14	PT39A	1	T		D14	PT39A	1	T	
E13	PT38B	1	C		E13	PT38B	1	C	
G13	PT38A	1	T	TDQS38	G13	PT38A	1	T	TDQS38
A12	PT37B	1	C		A12	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
B12	PT37A	1	T		B12	PT37A	1	T	
F13	PT36B	1	C		F13	PT36B	1	C	
D13	PT36A	1	T		D13	PT36A	1	T	
F12	PT35B	1	C	VREF2_1	F12	PT35B	1	C	VREF2_1
D12	PT35A	1	T	VREF1_1	D12	PT35A	1	T	VREF1_1
F11	PT34B	1	C		F11	PT34B	1	C	
C12	PT34A	1	T		C12	PT34A	1	T	
A11	PT33B	0	C	PCLKC0_0	A11	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A10	PT33A	0	T	PCLKT0_0	A10	PT33A	0	T	PCLKT0_0
E12	PT32B	0	C	VREF1_0	E12	PT32B	0	C	VREF1_0
E11	PT32A	0	T	VREF2_0	E11	PT32A	0	T	VREF2_0
B11	PT31B	0	C		B11	PT31B	0	C	
C11	PT31A	0	T		C11	PT31A	0	T	
B9	PT30B	0	C		B9	PT30B	0	C	
B10	PT30A	0	T	TDQS30	B10	PT30A	0	T	TDQS30
A9	PT29B	0	C		A9	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
A8	PT29A	0	T		A8	PT29A	0	T	
D11	PT28B	0	C		D11	PT28B	0	C	
C10	PT28A	0	T		C10	PT28A	0	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K16	VCC	-			K16	VCC	-		
K17	VCC	-			K17	VCC	-		
K6	VCC	-			K6	VCC	-		
K7	VCC	-			K7	VCC	-		
L17	VCC	-			L17	VCC	-		
L6	VCC	-			L6	VCC	-		
M17	VCC	-			M17	VCC	-		
M6	VCC	-			M6	VCC	-		
N16	VCC	-			N16	VCC	-		
N17	VCC	-			N17	VCC	-		
N6	VCC	-			N6	VCC	-		
N7	VCC	-			N7	VCC	-		
P16	VCC	-			P16	VCC	-		
P7	VCC	-			P7	VCC	-		
G11	VCCIO0	0			G11	VCCIO0	0		
H10	VCCIO0	0			H10	VCCIO0	0		
H11	VCCIO0	0			H11	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0		
G12	VCCIO1	1			G12	VCCIO1	1		
H12	VCCIO1	1			H12	VCCIO1	1		
H13	VCCIO1	1			H13	VCCIO1	1		
H14	VCCIO1	1			H14	VCCIO1	1		
J15	VCCIO2	2			J15	VCCIO2	2		
K15	VCCIO2	2			K15	VCCIO2	2		
L15	VCCIO2	2			L15	VCCIO2	2		
L16	VCCIO2	2			L16	VCCIO2	2		
M15	VCCIO3	3			M15	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3		
N15	VCCIO3	3			N15	VCCIO3	3		
P15	VCCIO3	3			P15	VCCIO3	3		
R12	VCCIO4	4			R12	VCCIO4	4		
R13	VCCIO4	4			R13	VCCIO4	4		
R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4		
R10	VCCIO5	5			R10	VCCIO5	5		
R11	VCCIO5	5			R11	VCCIO5	5		
R9	VCCIO5	5			R9	VCCIO5	5		
T11	VCCIO5	5			T11	VCCIO5	5		
M7	VCCIO6	6			M7	VCCIO6	6		
M8	VCCIO6	6			M8	VCCIO6	6		
N8	VCCIO6	6			N8	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6		
J8	VCCIO7	7			J8	VCCIO7	7		
K8	VCCIO7	7			K8	VCCIO7	7		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7		
E3	PL2A	7	T	VREF2_7	E3	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
E5	NC	-			E5	PL6A	7	T	LDQS6
D5	NC	-			D5	PL6B	7	C	
F4	NC	-			F4	PL7A	7	T	
F5	NC	-			F5	PL7B	7	C	
C3	NC	-			C3	PL8A	7	T	
D3	NC	-			D3	PL8B	7	C	
C2	NC	-			C2	PL9A	7	T	
-	-	-			GND	GND7	7		
B2	NC	-			B2	PL9B	7	C	
B1	PL3A	7	T		B1	PL10A	7	T	
C1	PL3B	7	C		C1	PL10B	7	C	
F3	PL4A	7	T		F3	PL11A	7	T	
G3	PL4B	7	C		G3	PL11B	7	C	
D2	PL5A	7	T		D2	PL12A	7	T	
E2	PL5B	7	C		E2	PL12B	7	C	
-	-	-			GND	GND7	7		
D1	PL6A	7	T	LDQS6	D1	PL14A	7	T	LDQS14
E1	PL6B	7	C		E1	PL14B	7	C	
F2	PL7A	7	T		F2	PL15A	7	T	
G2	PL7B	7	C		G2	PL15B	7	C	
F6	PL8A	7	T	LUM0_PLLT_IN_A	F6	PL16A	7	T	LUM0_PLLT_IN_A
G6	PL8B	7	C	LUM0_PLLC_IN_A	G6	PL16B	7	C	LUM0_PLLC_IN_A
H4	PL9A	7	T	LUM0_PLLT_FB_A	H4	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
G4	PL9B	7	C	LUM0_PLLC_FB_A	G4	PL17B	7	C	LUM0_PLLC_FB_A
H6	NC	-			H6	PL19A	7	T	
J7	NC	-			J7	PL19B	7	C	
G5	NC	-			G5	PL20A	7	T	
H5	NC	-			H5	PL20B	7	C	
H3	NC	-			H3	PL21A	7	T	
J3	NC	-			J3	PL21B	7	C	
H2	NC	-			H2	PL22A	7	T	
-	-	-			GND	GND7	7		
J2	NC	-			J2	PL22B	7	C	
J4	PL11A	7	T		J4	PL23A	7	T	LDQS23
J5	PL11B	7	C		J5	PL23B	7	C	
K4	PL12A	7	T		K4	PL24A	7	T	
K5	PL12B	7	C		K5	PL24B	7	C	
J6	PL13A	7	T		J6	PL25A	7	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF4	PB13B	5	C		AF4	PB13B	5	C	
AE5	PB14A	5	T	BDQS14	AE5	PB14A	5	T	BDQS14
AA9	PB14B	5	C		AA9	PB14B	5	C	
AF5	PB15A	5	T		AF5	PB15A	5	T	
Y10	PB15B	5	C		Y10	PB15B	5	C	
AD6	PB16A	5	T		AD6	PB16A	5	T	
AC10	PB16B	5	C		AC10	PB16B	5	C	
AF6	PB17A	5	T		AF6	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AE6	PB17B	5	C		AE6	PB17B	5	C	
AF7	PB18A	5	T		AF7	PB18A	5	T	
AB10	PB18B	5	C		AB10	PB18B	5	C	
AE7	PB19A	5	T		AE7	PB19A	5	T	
AD10	PB19B	5	C		AD10	PB19B	5	C	
AD7	PB20A	5	T		AD7	PB20A	5	T	
AA10	PB20B	5	C		AA10	PB20B	5	C	
AF8	PB21A	5	T		AF8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
AF9	PB21B	5	C		AF9	PB21B	5	C	
AD11	PB22A	5	T	BDQS22	AD11	PB22A	5	T	BDQS22
Y11	PB22B	5	C		Y11	PB22B	5	C	
AE8	PB23A	5	T		AE8	PB23A	5	T	
AC11	PB23B	5	C		AC11	PB23B	5	C	
AF10	PB24A	5	T		AF10	PB24A	5	T	
AB11	PB24B	5	C		AB11	PB24B	5	C	
AE10	PB25A	5	T		AE10	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AE9	PB25B	5	C		AE9	PB25B	5	C	
AA11	PB26A	5	T		AA11	PB26A	5	T	
Y12	PB26B	5	C		Y12	PB26B	5	C	
AE11	PB27A	5	T		AE11	PB27A	5	T	
AF11	PB27B	5	C		AF11	PB27B	5	C	
AF12	PB28A	5	T		AF12	PB28A	5	T	
AE12	PB28B	5	C		AE12	PB28B	5	C	
AD12	PB29A	5	T		AD12	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AC12	PB29B	5	C		AC12	PB29B	5	C	
AA12	PB30A	5	T	BDQS30	AA12	PB30A	5	T	BDQS30
AB12	PB30B	5	C		AB12	PB30B	5	C	
AE13	PB31A	5	T		AE13	PB31A	5	T	
AF13	PB31B	5	C		AF13	PB31B	5	C	
AD13	PB32A	5	T	VREF2_5	AD13	PB32A	5	T	VREF2_5

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFECP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFECP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFECP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFECP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFECP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFECP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFECP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFECP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFECP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFECP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFECP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFECP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFECP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFECP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFECP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFECP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFECP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFECP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFECP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFECP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFECP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFECP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFECP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFECP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFECP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFECP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFECP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFECP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFECP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFECP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFECP33E-5F672C	496	-5	fpBGA	672	COM	32.8K

LatticeECP/EC Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com

LatticeECP/EC Family Data Sheet Revision History

Revision History

Date	Version	Section	Change Summary
June 2004	01.0	—	Initial release.
August 2004	01.1	Introduction	Added new device LFECP/LFEC33 in Table 1-1.
		Architecture	Added New device LFECP/LFEC33 in Tables 2-9, 2-10 and 2-11.
		DC & Switching Characteristics	Added New device LFECP/LFEC33 on Supply current (Standby) tables.
			Added New device LFECP/LFEC33 on Initialization Supply current tables.
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section.
			Added EC33, ECP33 device: Industrial and Commercial to Part Number table.
			Corrected I/O counts in the part number tables for 100/144 TQFP and 208 PQFP packages to match Table 1-1 on page 1.
November 2004	01.3	Introduction	Changed DDR333 (166MHz) to DDR400 (200MHz)
			Added “RSDS” offering to the Features list: Flexible I/O Buffer
		Architecture	Added information about Secondary Clock Sources
			Added information about DCS
			Added a section on “Recommended Power-up Sequence”
			Updated Figure 2-24 “DQS Routing”
			Added DSP Block performance numbers to Table 2-11
			Added another row for RSDS in Table 2-13 and Table 2-14
		DC & Switching Characteristics	Updated new timing numbers
			Added numbers to derating table
			Added DC conditions to RSDS table
			Changed LVDS Max. V_{CCIO} to 2.625
			Added a row for RSDS in “Operating Condition” table
			Updated standby and initialization current table
			Added figure 3-12: sysConfig SPI port sequence
			Added DDR Timing Table and DDR Timings Figure 3-6
		Pinout Information	Added LFECP/EC6 to Pin Information
			Added LFECP/EC6 to Power Supply and NC Connections
			Added LFECP/EC6 144 TQFP Logic Signal Connections
			Added LFECP/EC6 208 PQFP Logic Signal Connections
			Added LFECP/EC6 256 fpBGA Logic Signal Connections
			Added LFECP/EC6 484 fpBGA Logic Signal Connections
		Ordering Information	Added 33K Logic Capacity Device in Part Number Description section.
			Added Part Number table for Commercial EC33.
			Added Part Number table for Commercial ECP33.
			Added Part Number table for Industrial EC33.
			Added Part Number table for Industrial ECP33.