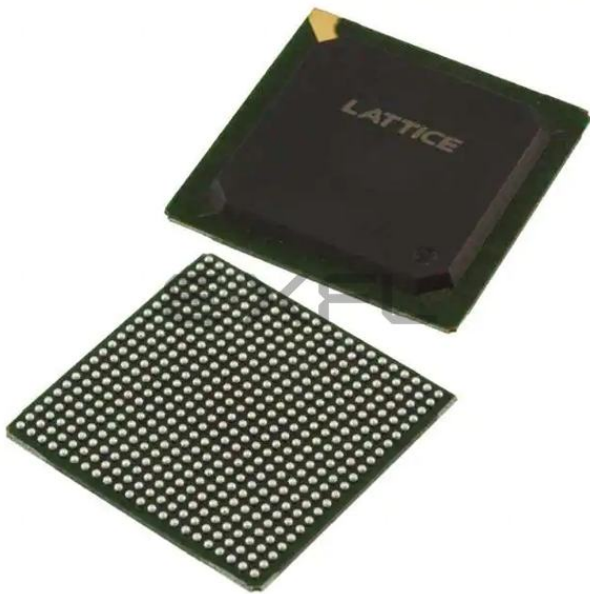




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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	32800
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec33e-3fn484c

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-8. Per Quadrant Primary Clock Selection

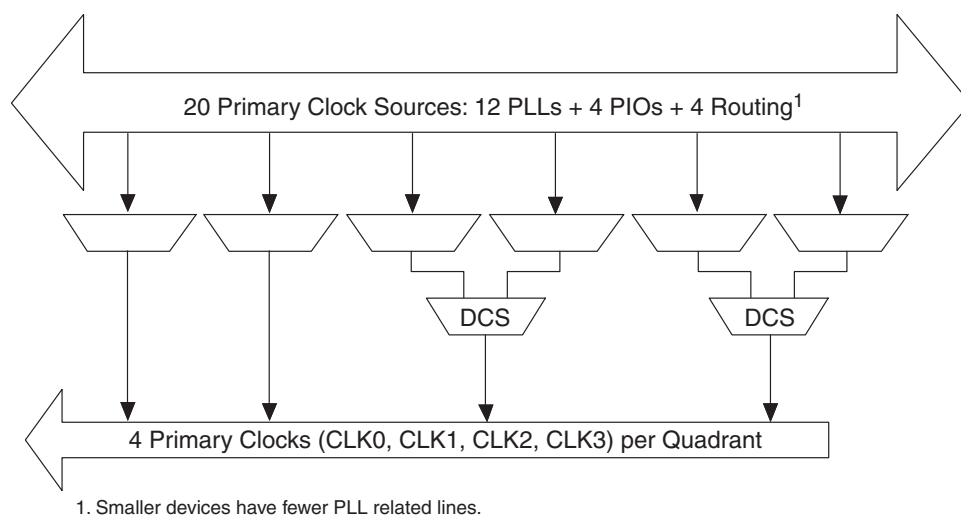


Figure 2-9. Per Quadrant Secondary Clock Selection

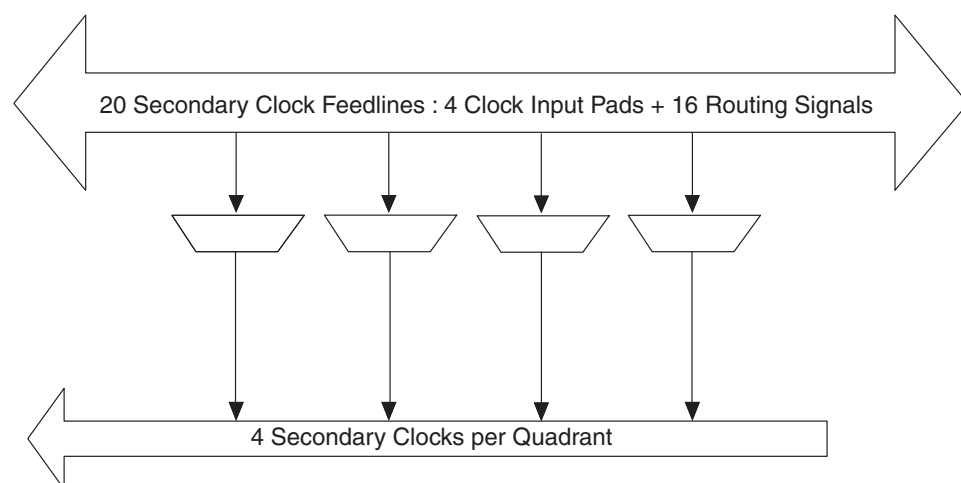
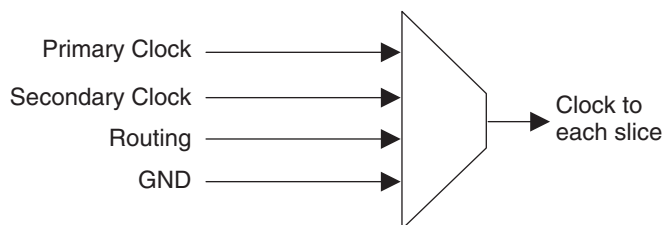


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

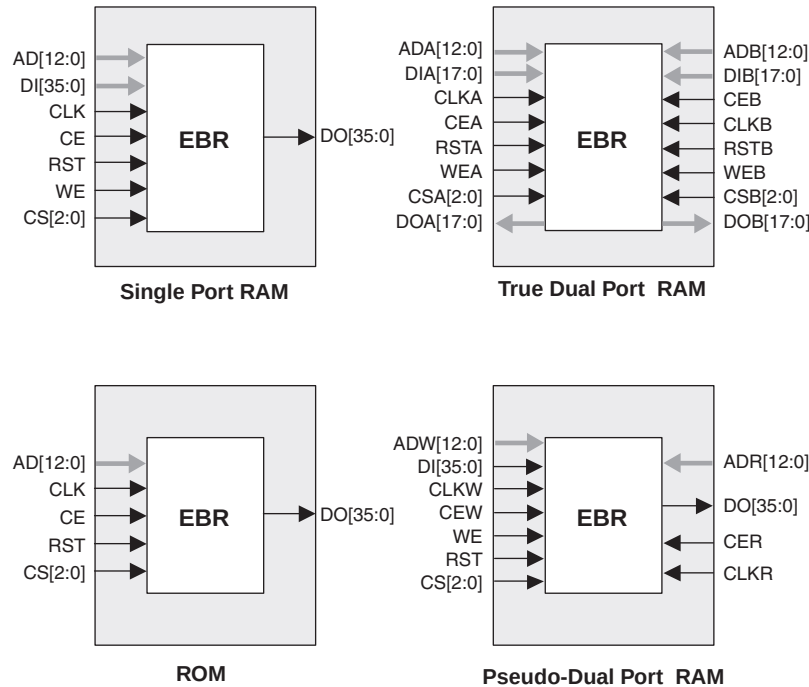
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-29. Output Register Block

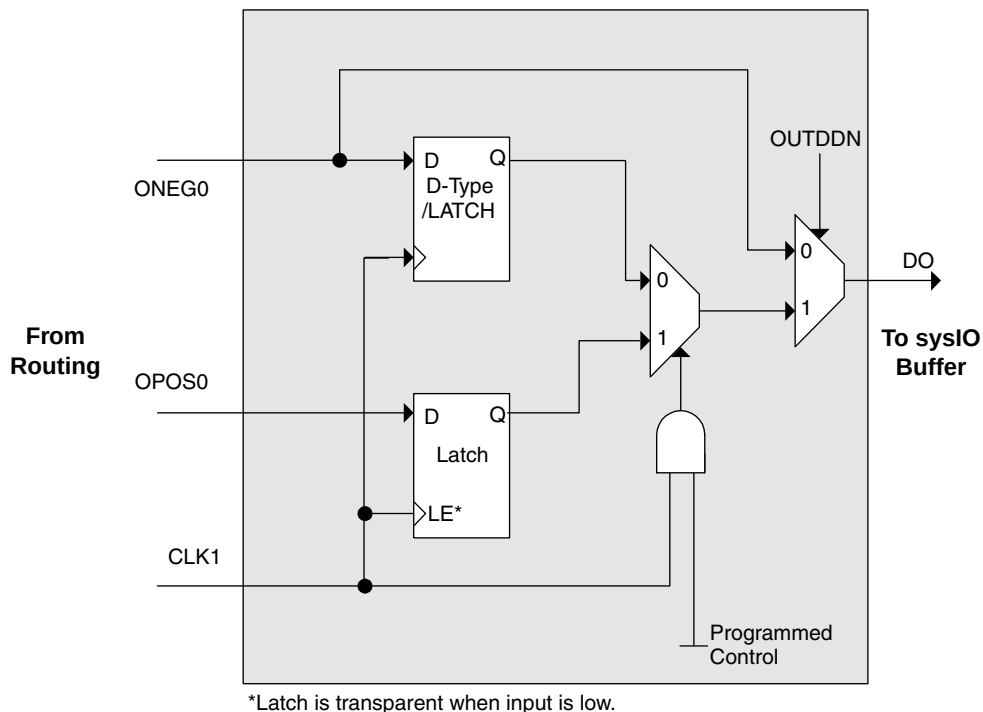
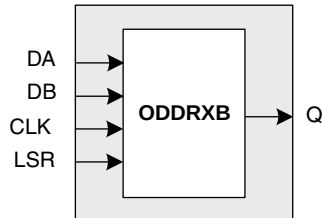


Figure 2-30. ODDRXB Primitive



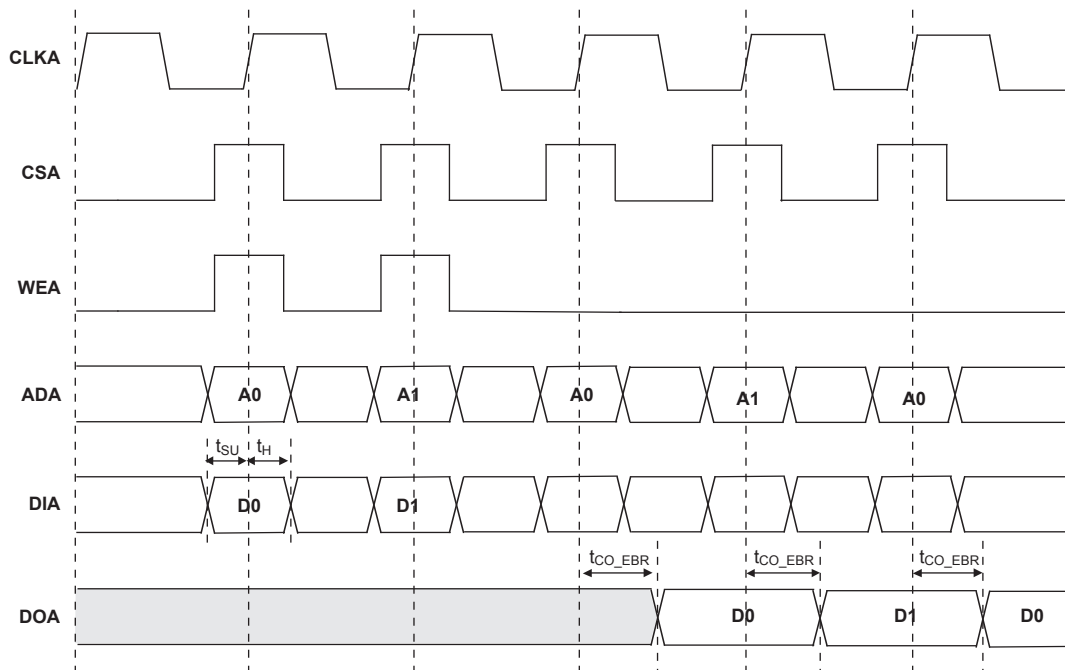
Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

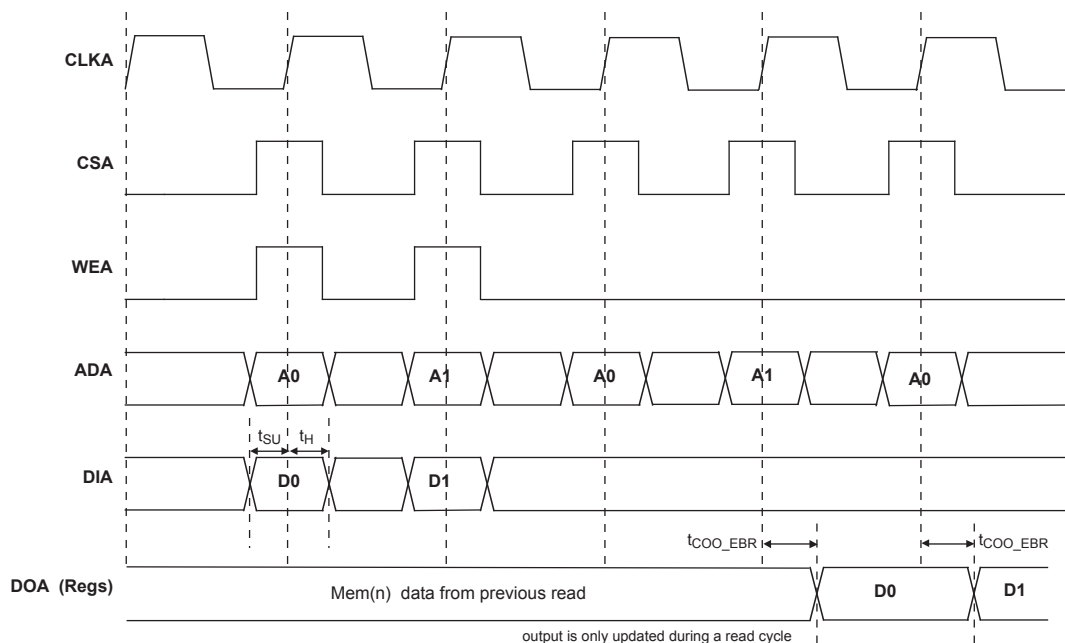
EBR Memory Timing Diagrams

Figure 3-8. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-9. Read/Write Mode with Input and Output Registers



LatticeECP/EC Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_II	HSTL_15 class II	0.10	0.12	0.14	ns
HSTL15_III	HSTL_15 class III	0.10	0.12	0.14	ns
HSTL15D_I	Differential HSTL 15 class I	0.08	0.10	0.11	ns
HSTL15D_III	Differential HSTL 15 class III	0.10	0.12	0.14	ns
SSTL33_I	SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33_II	SSTL_3 class II	0.40	0.48	0.56	ns
SSTL33D_I	Differential SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33D_II	Differential SSTL_3 class II	0.40	0.48	0.56	ns
SSTL25_I	SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25_II	SSTL_2 class II	0.25	0.30	0.35	ns
SSTL25D_I	Differential SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25D_II	Differential SSTL_2 class II	0.25	0.30	0.35	ns
SSTL18_I	SSTL_1.8 class I	0.01	0.01	0.01	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.01	0.01	0.01	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.09	0.11	0.13	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.07	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.03	-0.04	-0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.36	0.43	0.51	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.28	0.33	0.39	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.09	0.11	0.13	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.07	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	-0.03	-0.04	-0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.36	0.43	0.51	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.28	0.33	0.39	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.18	0.21	0.25	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.10	0.12	0.14	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.22	0.26	0.31	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.14	0.16	0.19	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.15	0.18	0.21	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.06	0.08	0.09	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.01	0.01	0.01	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.16	0.19	0.22	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.26	0.31	0.36	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.04	0.04	0.05	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.36	0.43	0.50	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.08	0.10	0.11	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	0.36	0.43	0.50	ns
PCI33	PCI33	1.05	1.26	1.46	ns

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Conditions table of this document.

3. All other standards according to the appropriate specification.

Timing v.G 0.30

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ

Notes:

1. "n" is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

Pin Information Summary

		LFEC1			LFEC3				LFEC6/EC6				LFEC6/EC10		
Pin Type		100-TQFP	144-TQFP	208-PQFP	100-TQFP	144-TQFP	208-PQFP	256-fpBGA	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	208-PQFP	256-fpBGA	484-fpBGA
Single Ended User I/O		67	97	112	67	97	145	160	97	147	195	224	147	195	288
Differential Pair User I/O		29	46	56	29	46	72	80	46	72	97	112	72	97	144
Configu-ration	Dedicated	13	13	13	13	13	13	13	13	13	13	13	13	13	13
	Muxed	48	48	48	48	48	48	48	48	48	48	48	56	56	56
TAP		5	5	5	5	5	5	5	5	5	5	5	5	5	5
Dedicated (total without supplies)		80	110	160	80	110	160	208	110	160	208	373	160	208	373
V _{CC}		2	3	3	2	3	3	10	4	4	10	20	6	10	20
V _{CCAUX}		2	2	2	4	4	4	4	2	4	2	12	4	2	12
V _{CCPLL}		0	0	0	0	0	0	0	0	0	0	0	0	0	0
V _{CCIO}	Bank0	1	2	2	1	2	3	2	2	3	2	4	3	2	4
	Bank1	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank2	1	1	1	2	2	2	2	1	2	2	4	2	2	4
	Bank3	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank4	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank5	1	2	2	1	2	2	2	2	3	2	4	3	2	4
	Bank6	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank7	1	1	1	2	2	2	2	1	2	2	4	2	2	4
GND, GND0-GND7		8	13	13	8	13	16	20	14	18	20	44	20	20	44
NC		0	2	51	0	2	9	35	0	4	0	139	0	0	75
Single Ended/Differential I/O Pair per Bank	Bank 0	11/5	14/7	16/8	11/5	14/7	26/13	32/16	14/7	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 1	11/5	13/6	16/8	11/5	13/6	16/8	16/8	13/6	17/8	18/9	32/16	17/8	18/9	32/16
	Bank 2	3/1	8/4	8/4	3/1	8/4	14/7	16/8	8/4	14/7	16/8	16/8	14/7	16/8	32/16
	Bank 3	8/4	13/6	16/8	8/4	13/6	16/8	16/8	13/6	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 4	12/4	14/6	16/8	12/4	14/6	16/8	16/8	14/6	17/8	17/8	32/16	17/8	17/8	32/16
	Bank 5	9/4	13/6	16/8	9/4	13/6	26/13	32/16	13/6	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 6	5/2	14/7	16/8	5/2	14/7	16/8	16/8	14/7	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 7	8/4	8/4	8/4	8/4	8/4	15/7	16/8	8/4	15/7	16/8	16/8	15/7	16/8	32/16
V _{CCJ}		1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

Power Supply and NC Connections (Cont.)

Signals	484 fpBGA	672 fpBGA
VCC	J16, J7, K16, K17, K6, K7, L17, L6, M17, M6, N16, N17, N6, N7, P16, P7, J6, J17, P6, P17	H10, H11, H16, H17, H18, H19, H8, H9, J18, J9, K8, L19, M19, N7, R20, R7, T19, V18, V8, V9, W10, W11, W16, W17, W18, W19, W8, W9, K19, L8, U19, U8
VCCIO0	G11, H10, H11, H9	H12, H13, J10, J11, J12, J13
VCCIO1	G12, H12, H13, H14	H14, H15, J14, J15, J16, J17
VCCIO2	J15, K15, L15, L16	K17, K18, L18, M18, N18, N19
VCCIO3	M15, M16, N15, P15	P18, P19, R18, R19, T18, U18
VCCIO4	R12, R13, R14, T12	V14, V15, V16, V17, W14, W15
VCCIO5	R10, R11, R9, T11	V10, V11, V12, V13, W12, W13
VCCIO6	M7, M8, N8, P8	P8, P9, R8, R9, T9, U9
VCCIO7	J8, K8, L7, L8	K9, L9, M8, M9, N8, N9
VCCJ	U2	U6
VCCAUX	G15, G16, G7, G8, H16, H7, R16, R7, T15, T16, T7, T8	G13, H20, H7, J19, J8, K7, L20, M20, M7, N20, P20, P7, T20, T7, T8, V19, V7, W20, Y13, Y7
VCCPLL	ECP/EC20: None ECP/EC33: J6, J17, P6, P17	ECP/EC20: None ECP/EC33: K19, L8, U19, U8
GND, GND0-GND7	A1, A22, AB1, AB22, H15, H8, J10, J11, J12, J13, J14, J9, K10, K11, K12, K13, K14, K9, L10, L11, L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R15, R8	K10, K11, K12, K13, K14, K15, K16, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17
NC	ECP/EC6: C3, B2, E5, F5, D3, C2, F4, G4, E3, D2, B1, C1, F3, E2, G5, H6, G3, H4, J5, H5, F2, F1, E1, D1, R6, P5, P3, P4, R1, R2, R5, R4, T1, T2, R3, T3, V7, T6, V8, U7, W5, U6, AA3, AB3, Y6, V6, AA5, W6, Y5, Y4, AA4, AB4, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, E21, D22, G21, G20, J18, H19, J19, H20, H17, H18, D21, C22, G19, G18, F20, F19, E20, D20, C21, C20, F18, E18, B22, B21, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A4, B4, C4, C5, D6, B5, E6, C6, A3, B3, F6, D5, F7, E8, G6, E7, A2, AB2, A21 ECP/EC10: G5, H6, G3, H4, J5, H5, F2, F1, R6, P5, P3, P4, R2, R1, R5, R4, T1, T2, R3, T3, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, G21, G20, J18, H19, J19, H20, H17, H18, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A2, AB2, A21 ECP/EC15: T1, T2, R3, T3, T18, R17, R19, R18, A2, AB2, A21 ECP/EC20: A2, AB2, A21 ECP/EC33: A2, AB2, A21	ECP/EC20: E5, D5, F4, F5, C3, D3, C2, B2, H6, J7, G5, H5, H3, J3, H2, J2, AA2, AA3, W5, Y5, Y6, W7, AA4, AB3, AC2, AC3, AA5, AB5, AD3, AD2, AE1, AD1, AD19, AD20, AC19, AB19, AD21, AC20, AF25, AE25, AB21, AB20, AE24, AD23, AD22, AC21, AC22, AB22, AD24, AD25, AE26, AD26, Y20, Y19, AA23, AA22, AB23, AB24, Y21, AA21, Y23, Y22, AA24, Y24, J21, J22, J23, H22, G26, F26, E26, E25, F24, F23, E24, D24, E22, F22, E21, D22, G20, F20, D21, C21, C23, C22, B23, C24, D20, E19, B25, B24, B26, A25, C20, C19 ECP/EC33: None

LFEC1, LFEC3, LFEC6/EC6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFEC1				LFEC3				LFEC6/EC6			
	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function
50	PB8B	5	C	VREF1_5	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
51	PB9A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
52	GND5	5			GND5	5			GND5	5		
53	PB9B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
54	VCCAUX	-			VCCAUX	-			VCCAUX	-		
55	VCCIO4	4			VCCIO4	4			VCCIO4	4		
56	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
57	PB10B	4	C	CS1N	PB18B	4	C	CS1N	PB18B	4	C	CS1N
58	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
59	PB11B	4	C	CSN	PB19B	4	C	CSN	PB19B	4	C	CSN
60	PB12A	4	T	VREF2_4	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
61	PB12B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
62	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
63	GND4	4			GND4	4			GND4	4		
64	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
65	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
66	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
67	PB15A	4	T		PB23A	4	T		PB23A	4	T	
68	PB15B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
69	PB16B	4		D5/SPID2	PB24B	4		D5/SPID2	PB24B	4		D5/SPID2
70	PB17B	4		D6/SPID1	PB25B	4		D6/SPID1	PB25B	4		D6/SPID1
71	VCCIO4	4			VCCIO4	4			VCCIO4	4		
72*	GND3 GND4	-			GND3 GND4	-			GND3 GND4	-		
73	VCCIO3	3			VCCIO3	3			VCCIO3	3		
74	PR14A	3		VREF1_3	PR18A	3		VREF1_3	PR27A	3		VREF1_3
75	PR12B	3	C		PR16B	3	C		PR25B	3	C	
76	PR12A	3	T		PR16A	3	T		PR25A	3	T	
77	PR11B	3	C		PR15B	3	C		PR24B	3	C	
78	PR11A	3	T	RDQS11	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
79	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
80	GND3	3			GND3	3			GND3	3		
81	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
82	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
83	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
84	VCCIO3	3			VCCIO3	3			VCCIO3	3		
85	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
86	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
87	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
88	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
89	CFG2	3			CFG2	3			CFG2	3		
90	CFG1	3			CFG1	3			CFG1	3		
91	CFG0	3			CFG0	3			CFG0	3		
92	VCC	-			VCC	-			VCC	-		
93	PROGRAMN	3			PROGRAMN	3			PROGRAMN	3		
94	CCLK	3			CCLK	3			CCLK	3		
95	INITN	3			INITN	3			INITN	3		
96	GND	-			GND	-			GND	-		
97	DONE	3			DONE	3			DONE	3		
98	GND	-			GND	-			GND	-		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W17	NC	-			W17	NC	-			W17	PB46B	4	C	
AA20	NC	-			AA20	NC	-			AA20	PB47A	4	T	
Y19	NC	-			Y19	NC	-			Y19	PB47B	4	C	
Y18	NC	-			Y18	NC	-			Y18	PB48A	4	T	
W18	NC	-			W18	NC	-			W18	PB48B	4	C	
T17	NC	-			T17	NC	-			T17	PB49A	4	T	
U17	NC	-			U17	NC	-			U17	PB49B	4	C	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3			GND	GND3	3		
W20	PR27B	3	C	VREF2_3	W20	PR36B	3	C	VREF2_3	W20	PR44B	3	C	VREF2_3
Y20	PR27A	3	T	VREF1_3	Y20	PR36A	3	T	VREF1_3	Y20	PR44A	3	T	VREF1_3
AA21	PR26B	3	C		AA21	PR35B	3	C		AA21	PR43B	3	C	
AB21	PR26A	3	T		AB21	PR35A	3	T		AB21	PR43A	3	T	
W19	PR25B	3	C		W19	PR34B	3	C		W19	PR42B	3	C	
V19	PR25A	3	T		V19	PR34A	3	T		V19	PR42A	3	T	
Y21	PR24B	3	C		Y21	PR33B	3	C		Y21	PR41B	3	C	
AA22	PR24A	3	T	RDQS24	AA22	PR33A	3	T	RDQS33	AA22	PR41A	3	T	RDQS41
V20	PR23B	3	C	RLM0_PLLC_FB_A	V20	PR32B	3	C	RLM0_PLLC_FB_A	V20	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND	GND3	3			GND	GND3	3		
U20	PR23A	3	T	RLM0_PLLT_FB_A	U20	PR32A	3	T	RLM0_PLLT_FB_A	U20	PR40A	3	T	RLM0_PLLT_FB_A
W21	PR22B	3	C	RLM0_PLLC_IN_A	W21	PR31B	3	C	RLM0_PLLC_IN_A	W21	PR39B	3	C	RLM0_PLLC_IN_A
Y22	PR22A	3	T	RLM0_PLLT_IN_A	Y22	PR31A	3	T	RLM0_PLLT_IN_A	Y22	PR39A	3	T	RLM0_PLLT_IN_A
V21	PR21B	3	C	DI/CSSPIN	V21	PR30B	3	C	DI/CSSPIN	V21	PR38B	3	C	DI/CSSPIN
W22	PR21A	3	T	DOUT/CSON	W22	PR30A	3	T	DOUT/CSON	W22	PR38A	3	T	DOUT/CSON
U21	PR20B	3	C	BUSY/SISPI	U21	PR29B	3	C	BUSY/SISPI	U21	PR37B	3	C	BUSY/SISPI
V22	PR20A	3	T	D7/SPID0	V22	PR29A	3	T	D7/SPID0	V22	PR37A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3			R20	DONE	3		
T18	NC	-			T18	NC	-			T18	NC	-		
R17	NC	-			R17	NC	-			R17	NC	-		
R19	NC	-			R19	NC	-			R19	NC	-		
R18	NC	-			R18	NC	-			R18	NC	-		
U22	NC	-			U22	NC	-			U22	PR35B	3	C	
GND	-	-			GND	-	-			GND	GND3	3		
T22	NC	-			T22	NC	-			T22	PR35A	3	T	
R21	NC	-			R21	NC	-			R21	PR34B	3	C	
R22	NC	-			R22	NC	-			R22	PR34A	3	T	
P20	NC	-			P20	NC	-			P20	PR33B	3	C	
N20	NC	-			N20	NC	-			N20	PR33A	3	T	
P19	NC	-			P19	NC	-			P19	PR32B	3	C	
P18	NC	-			P18	NC	-			P18	PR32A	3	T	
P21	PR18B	3	C		P21	PR27B	3	C		P21	PR31B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
P22	PR18A	3	T		P22	PR27A	3	T		P22	PR31A	3	T	
N21	PR17B	3	C		N21	PR26B	3	C		N21	PR30B	3	C	

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
N22	PR30A	3	T		N22	PR42A	3	T	
N19	PR29B	3	C		N19	PR41B	3	C	
N18	PR29A	3	T		N18	PR41A	3	T	
M21	PR28B	3	C		M21	PR40B	3	C	
L20	PR28A	3	T	RDQS28	L20	PR40A	3	T	RDQS40
L21	PR27B	3	C		L21	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M20	PR27A	3	T		M20	PR39A	3	T	
M18	PR26B	3	C		M18	PR38B	3	C	
M19	PR26A	3	T		M19	PR38A	3	T	
M22	PR25B	3	C		M22	PR37B	3	C	
L22	PR25A	3	T		L22	PR37A	3	T	
K22	PR24B	3	C		K22	PR36B	3	C	
K21	PR24A	3	T		K21	PR36A	3	T	
J22	PR22B	2	C	PCLKC2_0	J22	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
J21	PR22A	2	T	PCLKT2_0	J21	PR34A	2	T	PCLKT2_0
H22	PR21B	2	C		H22	PR33B	2	C	
H21	PR21A	2	T		H21	PR33A	2	T	
L19	PR20B	2	C		L19	PR32B	2	C	
L18	PR20A	2	T		L18	PR32A	2	T	
K20	PR19B	2	C		K20	PR31B	2	C	
J20	PR19A	2	T	RDQS19	J20	PR31A	2	T	RDQS31
K19	PR18B	2	C		K19	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
K18	PR18A	2	T		K18	PR30A	2	T	
G22	PR17B	2	C		G22	PR29B	2	C	
F22	PR17A	2	T		F22	PR29A	2	T	
F21	PR16B	2	C		F21	PR28B	2	C	
E22	PR16A	2	T		E22	PR28A	2	T	
E21	PR15B	2	C		E21	PR27B	2	C	
D22	PR15A	2	T		D22	PR27A	2	T	
G21	PR14B	2	C		G21	PR26B	2	C	
G20	PR14A	2	T		G20	PR26A	2	T	
GND	GND2	2			GND	GND2	2		
J18	PR13B	2	C		J18	PR25B	2	C	
H19	PR13A	2	T		H19	PR25A	2	T	
J19	PR12B	2	C		J19	PR24B	2	C	
H20	PR12A	2	T		H20	PR24A	2	T	
H17	PR11B	2	C		H17	PR23B	2	C	
H18	PR11A	2	T		H18	PR23A	2	T	RDQS23
D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
GND	-	-			GND	GND2	2		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
L24	PR17A	2	T		L24	PR29A	2	T	
K25	PR16B	2	C		K25	PR28B	2	C	
J25	PR16A	2	T		J25	PR28A	2	T	
J26	PR15B	2	C		J26	PR27B	2	C	
H26	PR15A	2	T		H26	PR27A	2	T	
H25	PR14B	2	C		H25	PR26B	2	C	
GND	GND2	2			GND	GND2	2		
J24	PR14A	2	T		J24	PR26A	2	T	
K21	PR13B	2	C		K21	PR25B	2	C	
K22	PR13A	2	T		K22	PR25A	2	T	
K20	PR12B	2	C		K20	PR24B	2	C	
J20	PR12A	2	T		J20	PR24A	2	T	
K23	PR11B	2	C		K23	PR23B	2	C	
K24	PR11A	2	T		K24	PR23A	2	T	RDQS23
J21	NC	-			J21	PR22B	2	C	
-	-	-			GND	GND2	2		
J22	NC	-			J22	PR22A	2	T	
J23	NC	-			J23	PR21B	2	C	
H22	NC	-			H22	PR21A	2	T	
G26	NC	-			G26	PR20B	2	C	
F26	NC	-			F26	PR20A	2	T	
E26	NC	-			E26	PR19B	2	C	
E25	NC	-			E25	PR19A	2	T	
F25	PR9B	2	C	RUM0_PLLC_FB_A	F25	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
G25	PR9A	2	T	RUM0_PLLT_FB_A	G25	PR17A	2	T	RUM0_PLLT_FB_A
H23	PR8B	2	C	RUM0_PLLC_IN_A	H23	PR16B	2	C	RUM0_PLLC_IN_A
H24	PR8A	2	T	RUM0_PLLT_IN_A	H24	PR16A	2	T	RUM0_PLLT_IN_A
H21	PR7B	2	C		H21	PR15B	2	C	
G21	PR7A	2	T		G21	PR15A	2	T	
D26	PR6B	2	C		D26	PR14B	2	C	
D25	PR6A	2	T	RDQS6	D25	PR14A	2	T	RDQS14
F21	PR5B	2	C		F21	PR13B	2	C	
-	-	-			GND	GND2	2		
G22	PR5A	2	T		G22	PR13A	2	T	
G24	PR4B	2	C		G24	PR12B	2	C	
G23	PR4A	2	T		G23	PR12A	2	T	
C26	PR3B	2	C		C26	PR11B	2	C	
C25	PR3A	2	T		C25	PR11A	2	T	
F24	NC	-			F24	PR9B	2	C	
-	-	-			GND	GND2	2		
F23	NC	-			F23	PR9A	2	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A5	PT13B	0	C		A5	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
A4	PT13A	0	T		A4	PT13A	0	T	
F9	PT12B	0	C		F9	PT12B	0	C	
B6	PT12A	0	T		B6	PT12A	0	T	
E9	PT11B	0	C		E9	PT11B	0	C	
C8	PT11A	0	T		C8	PT11A	0	T	
G8	PT10B	0	C		G8	PT10B	0	C	
B5	PT10A	0	T		B5	PT10A	0	T	
A3	PT9B	0	C		A3	PT9B	0	C	
GND	GND0	0			GND	GND0	0		
A2	PT9A	0	T		A2	PT9A	0	T	
F8	PT8B	0	C		F8	PT8B	0	C	
B4	PT8A	0	T		B4	PT8A	0	T	
E8	PT7B	0	C		E8	PT7B	0	C	
B3	PT7A	0	T		B3	PT7A	0	T	
D8	PT6B	0	C		D8	PT6B	0	C	
G7	PT6A	0	T	TDQS6	G7	PT6A	0	T	TDQS6
C4	PT5B	0	C		C4	PT5B	0	C	
C5	PT5A	0	T		C5	PT5A	0	T	
E7	PT4B	0	C		E7	PT4B	0	C	
D4	PT4A	0	T		D4	PT4A	0	T	
F7	PT3B	0	C		F7	PT3B	0	C	
D6	PT3A	0	T		D6	PT3A	0	T	
D7	PT2B	0	C		D7	PT2B	0	C	
E6	PT2A	0	T		E6	PT2A	0	T	
GND	GND0	0			GND	GND0	0		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K15	GND	-			K15	GND	-		
K16	GND	-			K16	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L15	GND	-			L15	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFCEP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFCEP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFCEP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFCEP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFCEP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFCEP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFCEP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFCEP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFCEP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFCEP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFCEP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFCEP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFCEP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFCEP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFCEP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFCEP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFCEP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFCEP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFCEP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFCEP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFCEP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFCEP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFCEP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFCEP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFCEP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFCEP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFCEP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFCEP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFCEP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFCEP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFCEP33E-5F672C	496	-5	fpBGA	672	COM	32.8K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672I	400	-3	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-4FN672I	400	-4	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-3FN484I	400	-3	Lead-Free fpBGA	484	IND	19.7K
LFEC20E-4FN484I	400	-4	Lead-Free fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672I	496	-3	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-4FN672I	496	-4	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-3FN484I	360	-3	Lead-Free fpBGA	484	IND	32.8K
LFEC33E-4FN484I	360	-4	Lead-Free fpBGA	484	IND	32.8K

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K