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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	32800
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec33e-4fn484i

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR16x2	ROM16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information about using RAM in LatticeECP/EC devices, please see the list of technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-8. Per Quadrant Primary Clock Selection

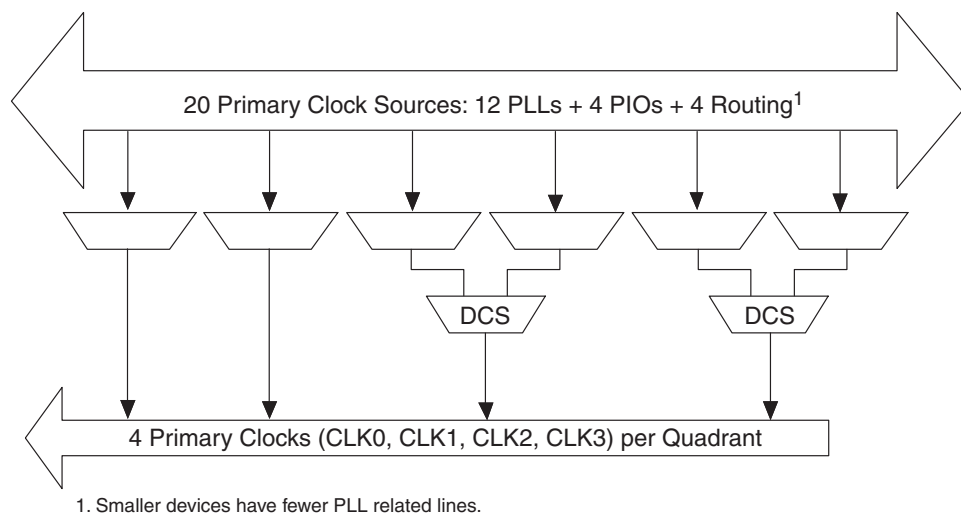


Figure 2-9. Per Quadrant Secondary Clock Selection

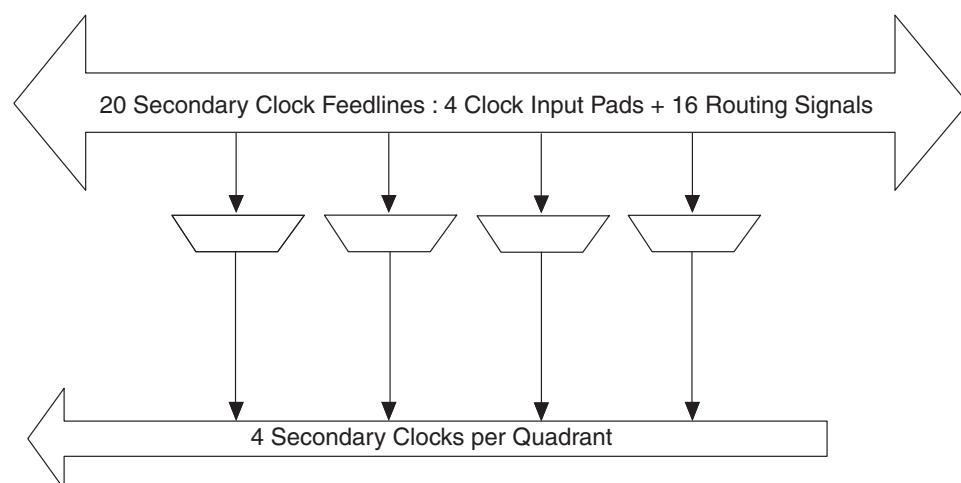
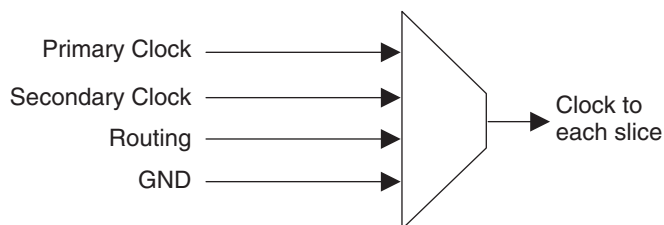


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Figure 2-27. Input Register DDR Waveforms

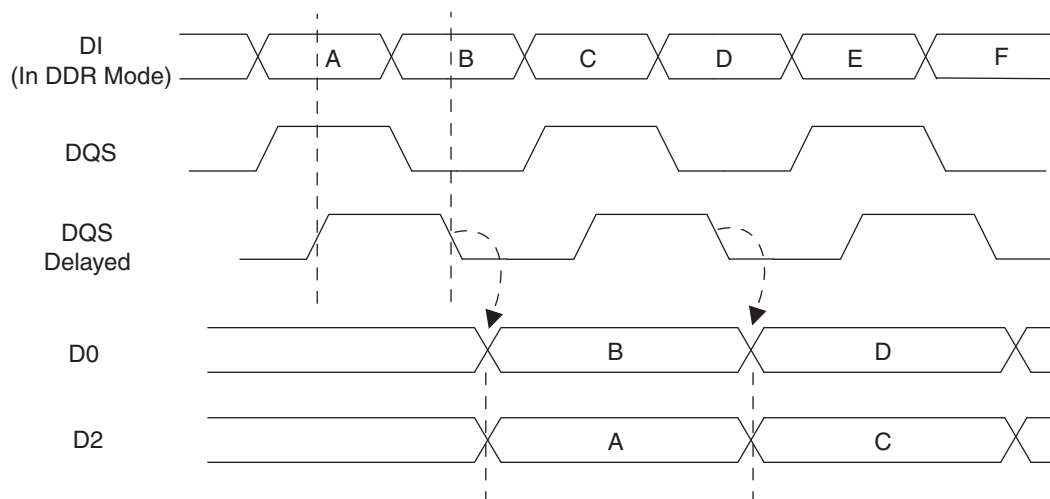
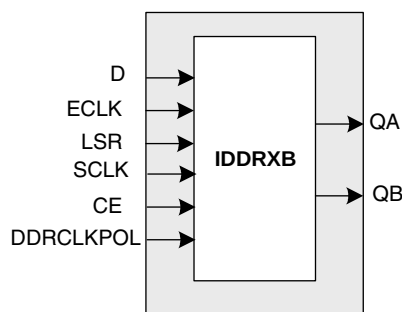


Figure 2-28. INDDRxB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sys/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-32. DQS Local Bus.

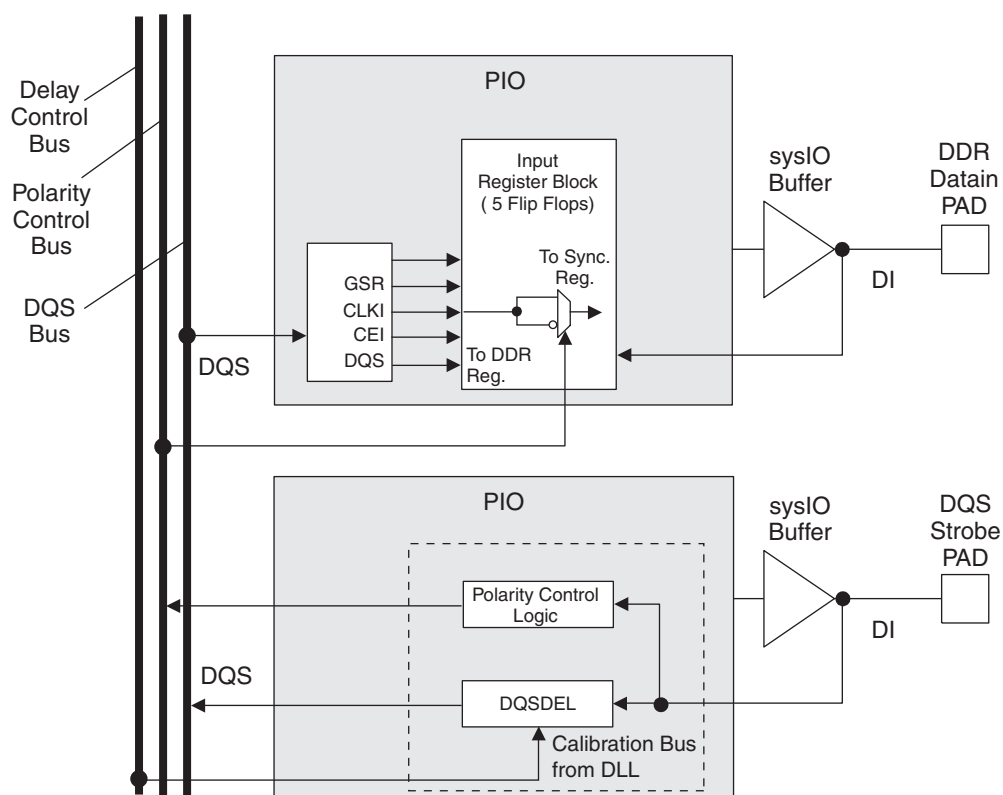


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution

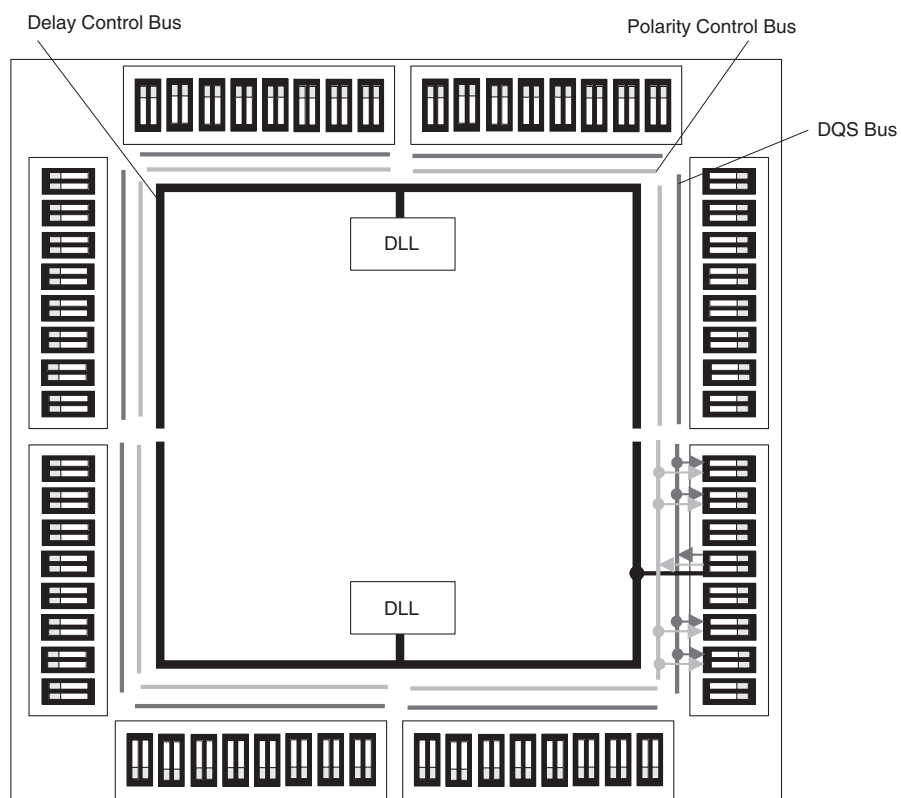


Table 2-14. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3
RSDS ¹	N/A	2.5

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

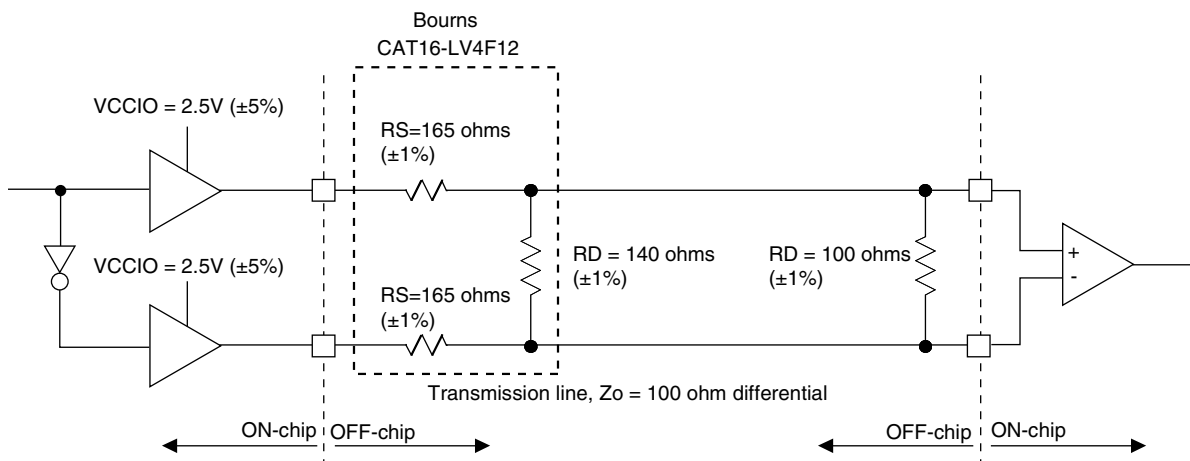


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.42	V
V_{OL}	Output low voltage	1.08	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	$\%$

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	210	MHz
f_{VCO}	PLL VCO Frequency		420	—	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Elected ³	45	50	55	%
t_{PH}^4	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	—	150	μs
t_{PA}	Programmable Delay Unit		100	250	450	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDL}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

Timing v.G 0.30

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
82	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
83	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
84	PT10B	1	C		PT18B	1	C	
85	PT10A	1	T		PT18A	1	T	
86	VCCIO1	1			VCCIO1	1		
87	VCCAUX	-			VCCAUX	-		
88	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
89	GND0	0			GND0	0		
90	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
91	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
92	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
93	PT7B	0			PT15B	0		
94	PT6B	0	C		PT14B	0	C	
95	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
96	PT4B	0	C		PT12B	0	C	
97	PT4A	0	T		PT12A	0	T	
98	PT2B	0	C		PT10B	0	C	
99	PT2A	0	T		PT10A	0	T	
100	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			NC	-		
6	NC	-			NC	-		
7	NC	-			PL3B	7		
8	NC	-			PL4A	7	T	
9	NC	-			PL4B	7	C	
10	NC	-			PL5A	7	T	
11	NC	-			PL5B	7	C	
12	NC	-			PL6A	7	T	LDQS6
13	NC	-			VCCIO7	7		
14	NC	-			PL6B	7	C	
15	PL3A	7	T		PL7A	7	T	
16	PL3B	7	C		PL7B	7	C	
17	PL4A	7	T		PL8A	7	T	
18	NC	-			NC	-		
19	PL4B	7	C		PL8B	7	C	
20	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
21	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
22	NC	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	NC	-			NC	-		
25	NC	-			NC	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LLM0_PLLT_IN_A
34	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LLM0_PLLC_IN_A
35	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LLM0_PLLT_FB_A
36	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL9A	6	T		PL13A	6	T	
39	PL9B	6	C		PL13B	6	C	
40	PL10A	6	T		PL14A	6	T	
41	GND6	6			GND6	6		
42	PL10B	6	C		PL14B	6	C	

LFEC3 and LFEC6/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFEC6/EC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
L3	TMS	6			TMS	6		
L5	TDO	6			TDO	6		
L4	VCCJ	6			VCCJ	6		
K2	PL29A	6	T	LLM0_PLLT_IN_A	PL37A	6	T	LLM0_PLLT_IN_A
K1	PL29B	6	C	LLM0_PLLC_IN_A	PL37B	6	C	LLM0_PLLC_IN_A
L2	PL30A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A
L1	PL30B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A
M2	PL31A	6	T		PL39A	6	T	
M1	PL31B	6	C		PL39B	6	C	
N1	PL32A	6	T		PL40A	6	T	
GND	GND6	6			GND6	6		
-	-	-			GND6	6		
N2	PL32B	6	C		PL40B	6	C	
M4	PL33A	6	T	LDQS33	PL41A	6	T	LDQS41
M3	PL33B	6	C		PL41B	6	C	
P1	PL34A	6	T		PL42A	6	T	
R1	PL34B	6	C		PL42B	6	C	
P2	PL35A	6	T		PL43A	6	T	
P3	PL35B	6	C		PL43B	6	C	
N3	PL36A	6	T	VREF1_6	PL44A	6	T	VREF1_6
N4	PL36B	6	C	VREF2_6	PL44B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
GND	GND5	5			GND5	5		
P4	PB10A	5	T		PB10A	5	T	
N5	PB10B	5	C		PB10B	5	C	
P5	PB11A	5	T		PB11A	5	T	
P6	PB11B	5	C		PB11B	5	C	
R4	PB12A	5	T		PB12A	5	T	
R3	PB12B	5	C		PB12B	5	C	
T2	PB13A	5	T		PB13A	5	T	
GND	GND5	5			GND5	5		
T3	PB13B	5	C		PB13B	5	C	
R5	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
R6	PB14B	5	C		PB14B	5	C	
T4	PB15A	5	T		PB15A	5	T	
T5	PB15B	5	C		PB15B	5	C	
N6	PB16A	5	T		PB16A	5	T	
M6	PB16B	5	C		PB16B	5	C	
T6	PB17A	5	T		PB17A	5	T	
GND	GND5	5			GND5	5		
T7	PB17B	5	C		PB17B	5	C	
P7	PB18A	5	T		PB18A	5	T	

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W17	NC	-			W17	NC	-			W17	PB46B	4	C	
AA20	NC	-			AA20	NC	-			AA20	PB47A	4	T	
Y19	NC	-			Y19	NC	-			Y19	PB47B	4	C	
Y18	NC	-			Y18	NC	-			Y18	PB48A	4	T	
W18	NC	-			W18	NC	-			W18	PB48B	4	C	
T17	NC	-			T17	NC	-			T17	PB49A	4	T	
U17	NC	-			U17	NC	-			U17	PB49B	4	C	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3			GND	GND3	3		
W20	PR27B	3	C	VREF2_3	W20	PR36B	3	C	VREF2_3	W20	PR44B	3	C	VREF2_3
Y20	PR27A	3	T	VREF1_3	Y20	PR36A	3	T	VREF1_3	Y20	PR44A	3	T	VREF1_3
AA21	PR26B	3	C		AA21	PR35B	3	C		AA21	PR43B	3	C	
AB21	PR26A	3	T		AB21	PR35A	3	T		AB21	PR43A	3	T	
W19	PR25B	3	C		W19	PR34B	3	C		W19	PR42B	3	C	
V19	PR25A	3	T		V19	PR34A	3	T		V19	PR42A	3	T	
Y21	PR24B	3	C		Y21	PR33B	3	C		Y21	PR41B	3	C	
AA22	PR24A	3	T	RDQS24	AA22	PR33A	3	T	RDQS33	AA22	PR41A	3	T	RDQS41
V20	PR23B	3	C	RLM0_PLLC_FB_A	V20	PR32B	3	C	RLM0_PLLC_FB_A	V20	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND	GND3	3			GND	GND3	3		
U20	PR23A	3	T	RLM0_PLLT_FB_A	U20	PR32A	3	T	RLM0_PLLT_FB_A	U20	PR40A	3	T	RLM0_PLLT_FB_A
W21	PR22B	3	C	RLM0_PLLC_IN_A	W21	PR31B	3	C	RLM0_PLLC_IN_A	W21	PR39B	3	C	RLM0_PLLC_IN_A
Y22	PR22A	3	T	RLM0_PLLT_IN_A	Y22	PR31A	3	T	RLM0_PLLT_IN_A	Y22	PR39A	3	T	RLM0_PLLT_IN_A
V21	PR21B	3	C	DI/CSSPIN	V21	PR30B	3	C	DI/CSSPIN	V21	PR38B	3	C	DI/CSSPIN
W22	PR21A	3	T	DOUT/CSON	W22	PR30A	3	T	DOUT/CSON	W22	PR38A	3	T	DOUT/CSON
U21	PR20B	3	C	BUSY/SISPI	U21	PR29B	3	C	BUSY/SISPI	U21	PR37B	3	C	BUSY/SISPI
V22	PR20A	3	T	D7/SPID0	V22	PR29A	3	T	D7/SPID0	V22	PR37A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3			R20	DONE	3		
T18	NC	-			T18	NC	-			T18	NC	-		
R17	NC	-			R17	NC	-			R17	NC	-		
R19	NC	-			R19	NC	-			R19	NC	-		
R18	NC	-			R18	NC	-			R18	NC	-		
U22	NC	-			U22	NC	-			U22	PR35B	3	C	
GND	-	-			GND	-	-			GND	GND3	3		
T22	NC	-			T22	NC	-			T22	PR35A	3	T	
R21	NC	-			R21	NC	-			R21	PR34B	3	C	
R22	NC	-			R22	NC	-			R22	PR34A	3	T	
P20	NC	-			P20	NC	-			P20	PR33B	3	C	
N20	NC	-			N20	NC	-			N20	PR33A	3	T	
P19	NC	-			P19	NC	-			P19	PR32B	3	C	
P18	NC	-			P18	NC	-			P18	PR32A	3	T	
P21	PR18B	3	C		P21	PR27B	3	C		P21	PR31B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
P22	PR18A	3	T		P22	PR27A	3	T		P22	PR31A	3	T	
N21	PR17B	3	C		N21	PR26B	3	C		N21	PR30B	3	C	

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A4	NC	-			A4	PT9B	0	C		A4	PT9B	0	C	
B4	NC	-			B4	PT9A	0	T		B4	PT9A	0	T	
C4	NC	-			C4	PT8B	0	C		C4	PT8B	0	C	
C5	NC	-			C5	PT8A	0	T		C5	PT8A	0	T	
D6	NC	-			D6	PT7B	0	C		D6	PT7B	0	C	
B5	NC	-			B5	PT7A	0	T		B5	PT7A	0	T	
E6	NC	-			E6	PT6B	0	C		E6	PT6B	0	C	
C6	NC	-			C6	PT6A	0	T	TDQS6	C6	PT6A	0	T	TDQS6
A3	NC	-			A3	PT5B	0	C		A3	PT5B	0	C	
B3	NC	-			B3	PT5A	0	T		B3	PT5A	0	T	
F6	NC	-			F6	PT4B	0	C		F6	PT4B	0	C	
D5	NC	-			D5	PT4A	0	T		D5	PT4A	0	T	
F7	NC	-			F7	PT3B	0	C		F7	PT3B	0	C	
E8	NC	-			E8	PT3A	0	T		E8	PT3A	0	T	
G6	NC	-			G6	PT2B	0	C		G6	PT2B	0	C	
E7	NC	-			E7	PT2A	0	T		E7	PT2A	0	T	
GND	-	-			GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-			A22	GND	-		
AB1	GND	-			AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-			N12	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
P5	PL32B	6	C		P5	PL44B	6	C	
P6	PL33A	6	T		P6	PL45A	6	T	
R5	PL33B	6	C		R5	PL45B	6	C	
U1	PL34A	6	T		U1	PL46A	6	T	
U2	PL34B	6	C		U2	PL46B	6	C	
T3	PL35A	6	T		T3	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
T4	PL35B	6	C		T4	PL47B	6	C	
R6	PL36A	6	T	LDQS36	R6	PL48A	6	T	LDQS48
T5	PL36B	6	C		T5	PL48B	6	C	
T6	PL37A	6	T		T6	PL49A	6	T	
U5	PL37B	6	C		U5	PL49B	6	C	
U3	PL38A	6	T		U3	PL50A	6	T	
U4	PL38B	6	C		U4	PL50B	6	C	
V1	PL39A	6	T		V1	PL51A	6	T	
GND	GND6	6			GND	GND6	6		
V2	PL39B	6	C		V2	PL51B	6	C	
U7	TCK	6			U7	TCK	6		
V4	TDI	6			V4	TDI	6		
V5	TMS	6			V5	TMS	6		
V3	TDO	6			V3	TDO	6		
U6	VCCJ	6			U6	VCCJ	6		
W1	PL41A	6	T	LLM0_PLLT_IN_A	W1	PL53A	6	T	LLM0_PLLT_IN_A
W2	PL41B	6	C	LLM0_PLLC_IN_A	W2	PL53B	6	C	LLM0_PLLC_IN_A
V6	PL42A	6	T	LLM0_PLLT_FB_A	V6	PL54A	6	T	LLM0_PLLT_FB_A
W6	PL42B	6	C	LLM0_PLLC_FB_A	W6	PL54B	6	C	LLM0_PLLC_FB_A
Y1	PL43A	6	T		Y1	PL55A	6	T	
Y2	PL43B	6	C		Y2	PL55B	6	C	
W3	PL44A	6	T		W3	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W4	PL44B	6	C		W4	PL56B	6	C	
AA1	PL45A	6	T	LDQS45	AA1	PL57A	6	T	LDQS57
AB1	PL45B	6	C		AB1	PL57B	6	C	
Y4	PL46A	6	T		Y4	PL58A	6	T	
Y3	PL46B	6	C		Y3	PL58B	6	C	
AC1	PL47A	6	T		AC1	PL59A	6	T	
AB2	PL47B	6	C		AB2	PL59B	6	C	
AA2	NC	-			AA2	PL60A	6	T	
-	-	-			GND	GND6	6		
AA3	NC	-			AA3	PL60B	6	C	
W5	NC	-			W5	PL61A	6	T	
Y5	NC	-			Y5	PL61B	6	C	

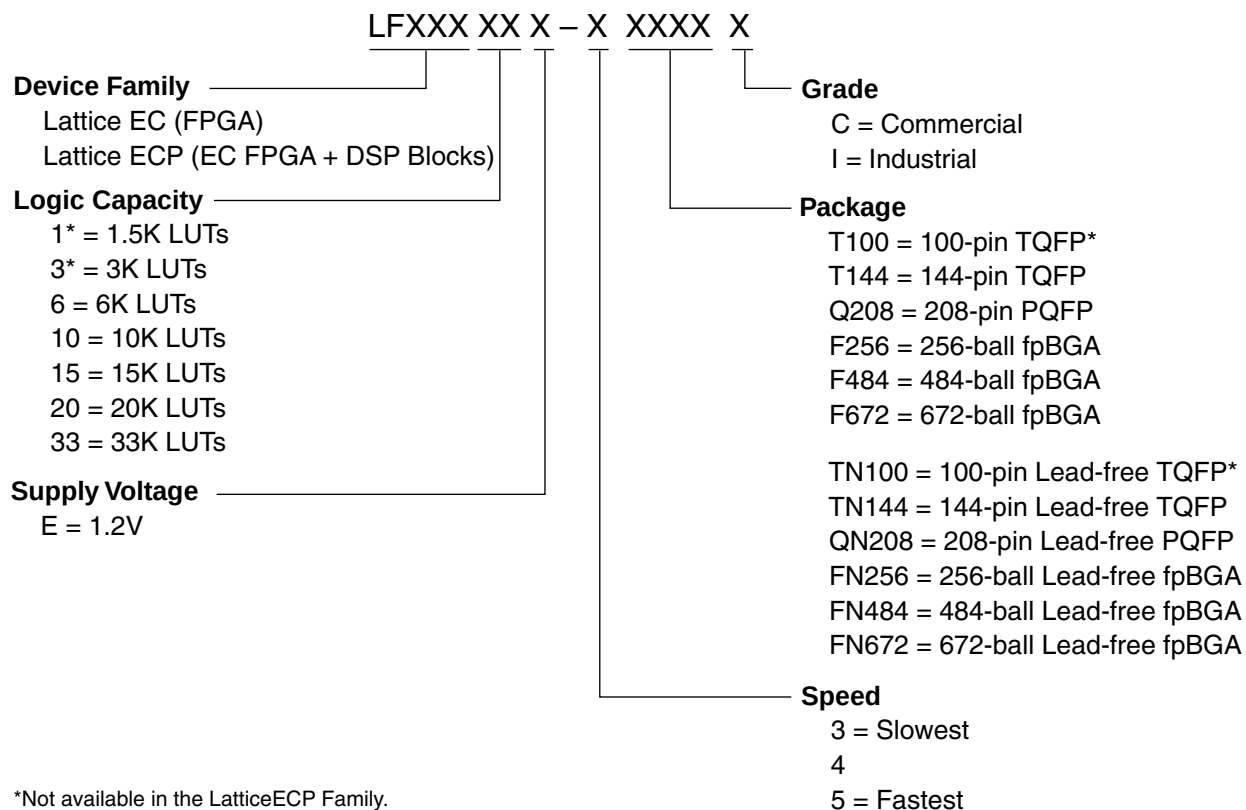
LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y6	NC	-			Y6	PL62A	6	T	
W7	NC	-			W7	PL62B	6	C	
AA4	NC	-			AA4	PL63A	6	T	
AB3	NC	-			AB3	PL63B	6	C	
AC2	NC	-			AC2	PL64A	6	T	
-	-	-			GND	GND6	6		
AC3	NC	-			AC3	PL64B	6	C	
AA5	NC	-			AA5	PL65A	6	T	LDQS65
AB5	NC	-			AB5	PL65B	6	C	
AD3	NC	-			AD3	PL66A	6	T	
AD2	NC	-			AD2	PL66B	6	C	
AE1	NC	-			AE1	PL67A	6	T	
AD1	NC	-			AD1	PL67B	6	C	
AB4	PL48A	6	T	VREF1_6	AB4	PL68A	6	T	VREF1_6
AC4	PL48B	6	C	VREF2_6	AC4	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND5	5		
AB6	PB2A	5	T		AB6	PB2A	5	T	
AA6	PB2B	5	C		AA6	PB2B	5	C	
AC7	PB3A	5	T		AC7	PB3A	5	T	
Y8	PB3B	5	C		Y8	PB3B	5	C	
AB7	PB4A	5	T		AB7	PB4A	5	T	
AA7	PB4B	5	C		AA7	PB4B	5	C	
AC6	PB5A	5	T		AC6	PB5A	5	T	
AC5	PB5B	5	C		AC5	PB5B	5	C	
AB8	PB6A	5	T	BDQS6	AB8	PB6A	5	T	BDQS6
AC8	PB6B	5	C		AC8	PB6B	5	C	
AE2	PB7A	5	T		AE2	PB7A	5	T	
AA8	PB7B	5	C		AA8	PB7B	5	C	
AF2	PB8A	5	T		AF2	PB8A	5	T	
Y9	PB8B	5	C		Y9	PB8B	5	C	
AD5	PB9A	5	T		AD5	PB9A	5	T	
GND	GND5	5			GND	GND5	5		
AD4	PB9B	5	C		AD4	PB9B	5	C	
AD8	PB10A	5	T		AD8	PB10A	5	T	
AC9	PB10B	5	C		AC9	PB10B	5	C	
AE3	PB11A	5	T		AE3	PB11A	5	T	
AB9	PB11B	5	C		AB9	PB11B	5	C	
AF3	PB12A	5	T		AF3	PB12A	5	T	
AD9	PB12B	5	C		AD9	PB12B	5	C	
AE4	PB13A	5	T		AE4	PB13A	5	T	
GND	GND5	5			GND	GND5	5		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

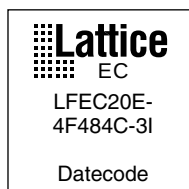
LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
D13	PT32B	0	C	VREF1_0	D13	PT32B	0	C	VREF1_0
C13	PT32A	0	T	VREF2_0	C13	PT32A	0	T	VREF2_0
A13	PT31B	0	C		A13	PT31B	0	C	
B13	PT31A	0	T		B13	PT31A	0	T	
F13	PT30B	0	C		F13	PT30B	0	C	
F12	PT30A	0	T	TDQS30	F12	PT30A	0	T	TDQS30
A12	PT29B	0	C		A12	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
B12	PT29A	0	T		B12	PT29A	0	T	
A11	PT28B	0	C		A11	PT28B	0	C	
B11	PT28A	0	T		B11	PT28A	0	T	
D12	PT27B	0	C		D12	PT27B	0	C	
C12	PT27A	0	T		C12	PT27A	0	T	
B10	PT26B	0	C		B10	PT26B	0	C	
A10	PT26A	0	T		A10	PT26A	0	T	
G12	PT25B	0	C		G12	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
A9	PT25A	0	T		A9	PT25A	0	T	
E12	PT24B	0	C		E12	PT24B	0	C	
B9	PT24A	0	T		B9	PT24A	0	T	
F11	PT23B	0	C		F11	PT23B	0	C	
A8	PT23A	0	T		A8	PT23A	0	T	
D11	PT22B	0	C		D11	PT22B	0	C	
C11	PT22A	0	T	TDQS22	C11	PT22A	0	T	TDQS22
B8	PT21B	0	C		B8	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
B7	PT21A	0	T		B7	PT21A	0	T	
E11	PT20B	0	C		E11	PT20B	0	C	
A7	PT20A	0	T		A7	PT20A	0	T	
G11	PT19B	0	C		G11	PT19B	0	C	
C7	PT19A	0	T		C7	PT19A	0	T	
G10	PT18B	0	C		G10	PT18B	0	C	
C6	PT18A	0	T		C6	PT18A	0	T	
C10	PT17B	0	C		C10	PT17B	0	C	
GND	GND0	0			GND	GND0	0		
D10	PT17A	0	T		D10	PT17A	0	T	
F10	PT16B	0	C		F10	PT16B	0	C	
A6	PT16A	0	T		A6	PT16A	0	T	
E10	PT15B	0	C		E10	PT15B	0	C	
C9	PT15A	0	T		C9	PT15A	0	T	
G9	PT14B	0	C		G9	PT14B	0	C	
D9	PT14A	0	T	TDQS14	D9	PT14A	0	T	TDQS14

Part Number Description



Ordering Information

Note: LatticeECP/EC devices are dual marked. For example, the commercial speed grade LFEC20E-4F484C is also marked with industrial grade -3I (LFEC20E-3F484I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672I	400	-3	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-4FN672I	400	-4	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-3FN484I	400	-3	Lead-Free fpBGA	484	IND	19.7K
LFEC20E-4FN484I	400	-4	Lead-Free fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672I	496	-3	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-4FN672I	496	-4	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-3FN484I	360	-3	Lead-Free fpBGA	484	IND	32.8K
LFEC33E-4FN484I	360	-4	Lead-Free fpBGA	484	IND	32.8K

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K