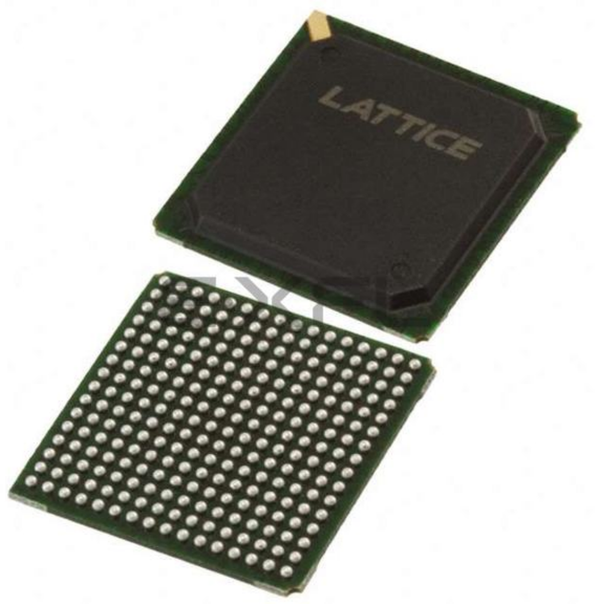

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec6e-3f256c

Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)

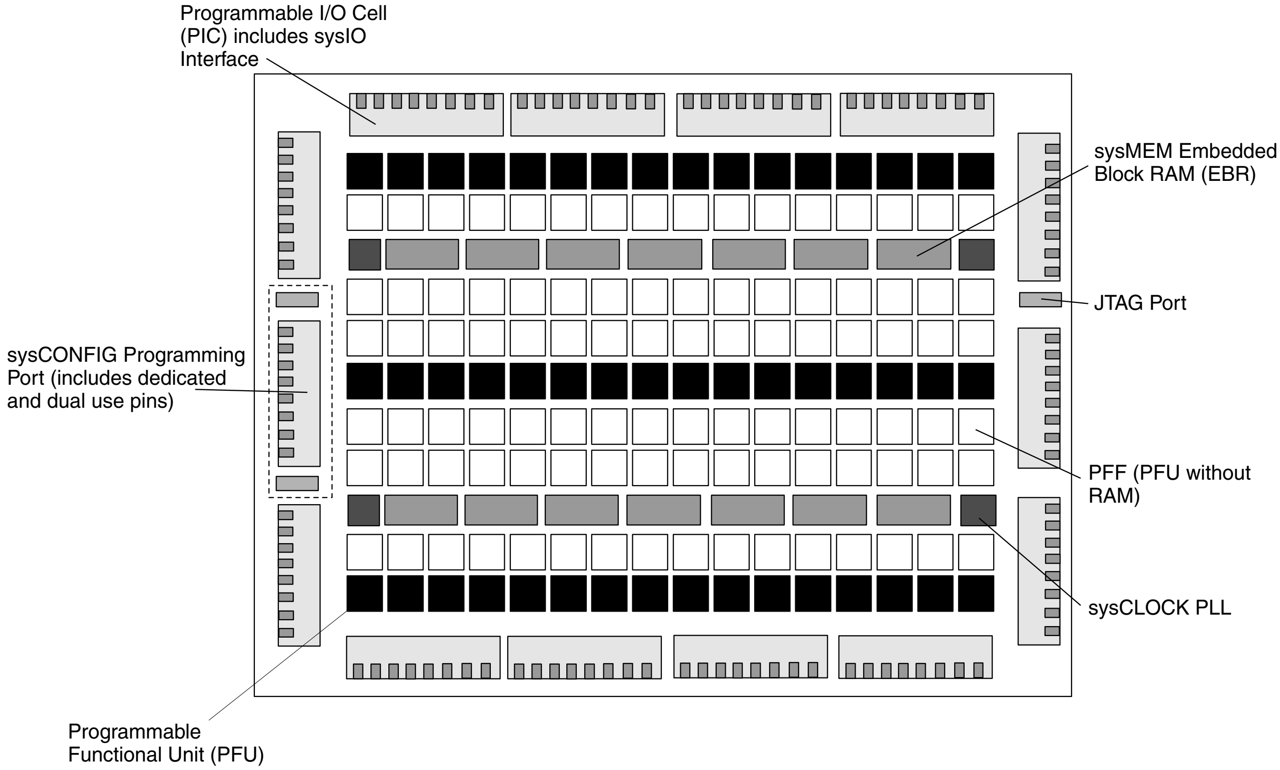
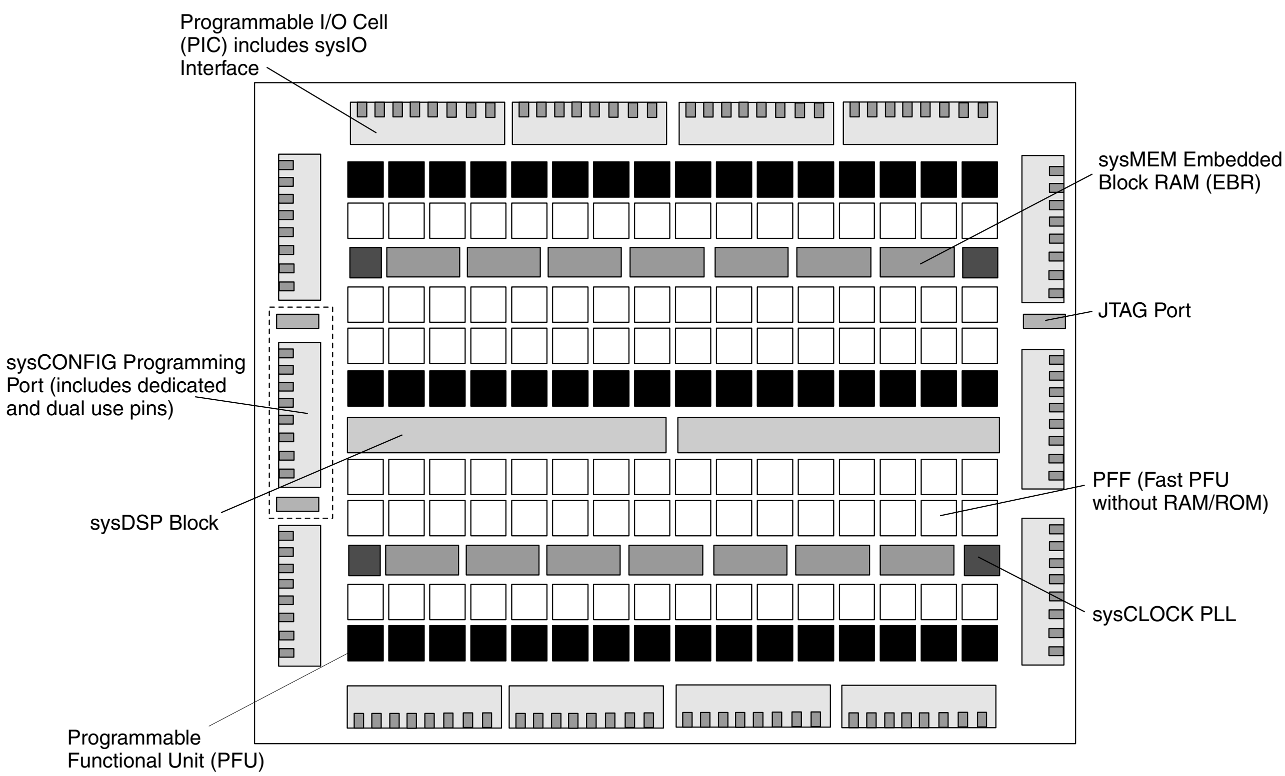


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)



Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, the routing of both short and long connections between PFUs.

The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

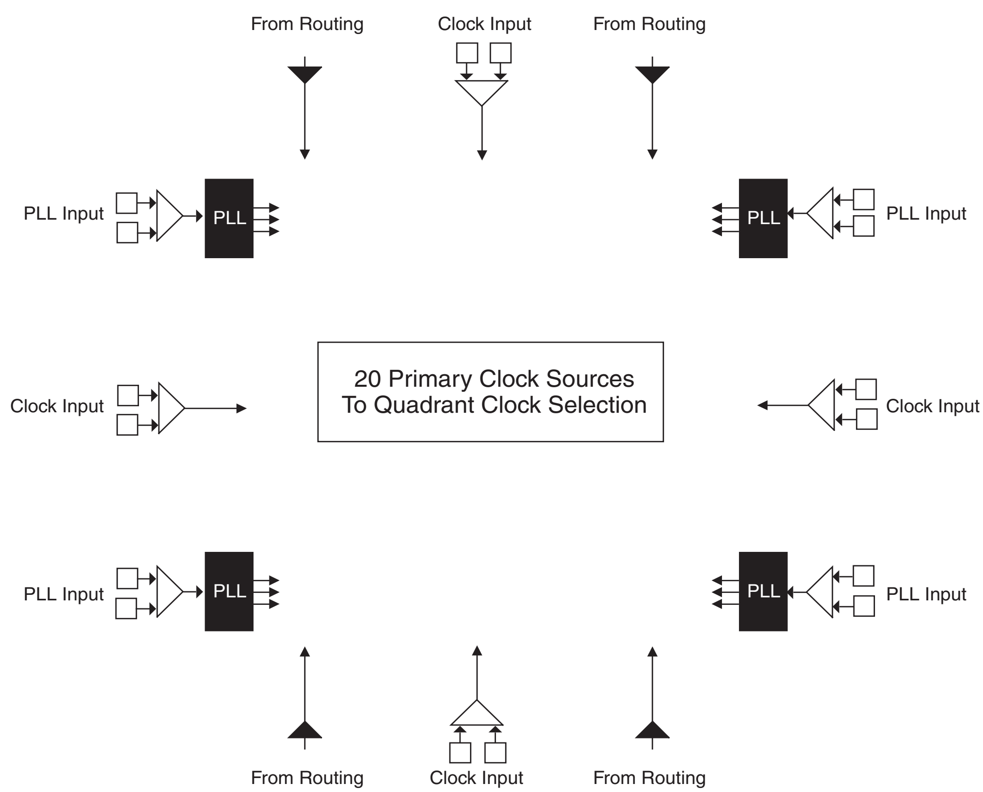
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

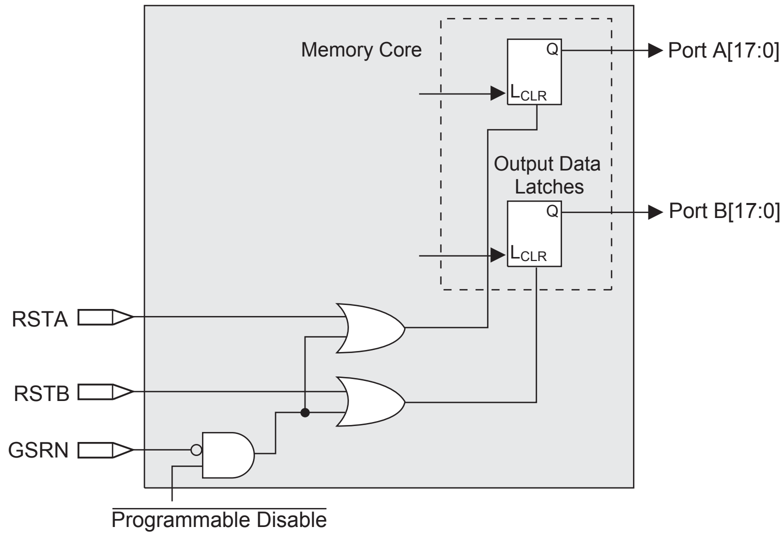
LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Primary Clock Sources



Note: Smaller devices have two PLLs.

Figure 2-16. Memory Core Reset

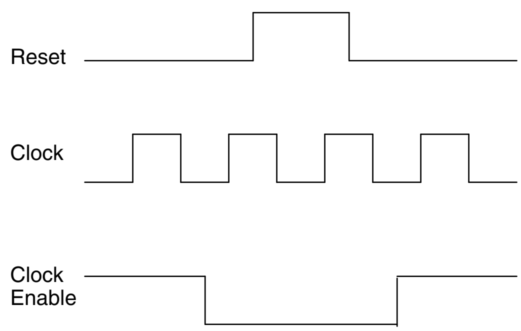


For further information about sysMEM EBR block, please see the the list of technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-17. The GSR input to the EBR is always asynchronous.

Figure 2-17. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

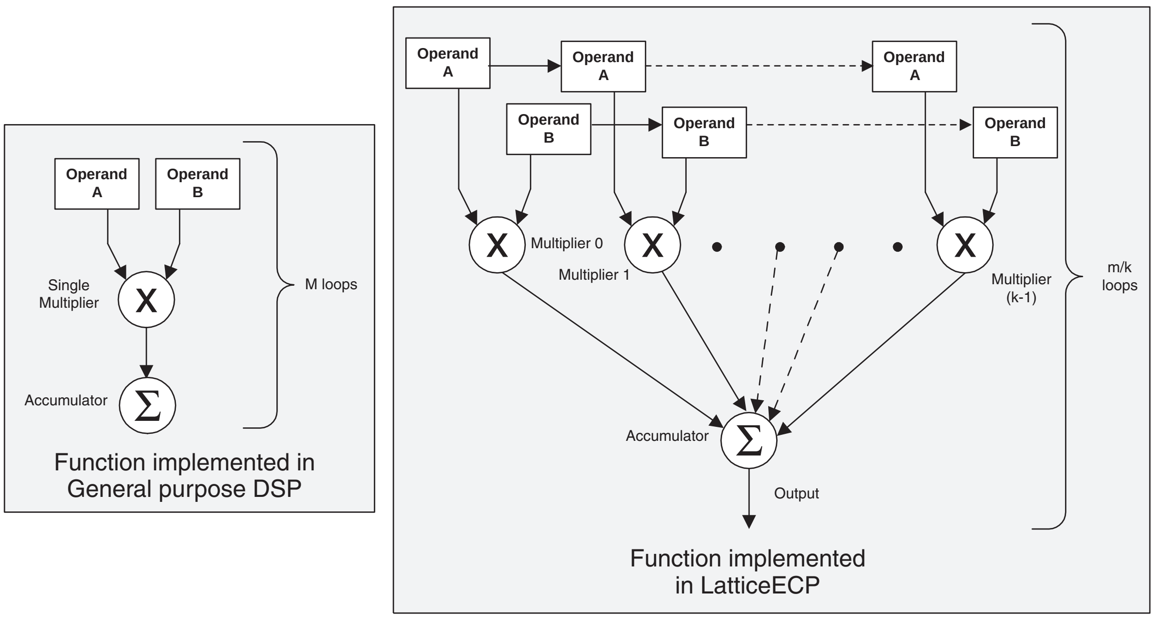
sysDSP Block

The LatticeECP-DSP family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-18 compares the serial and the parallel implementations.

Figure 2-18. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

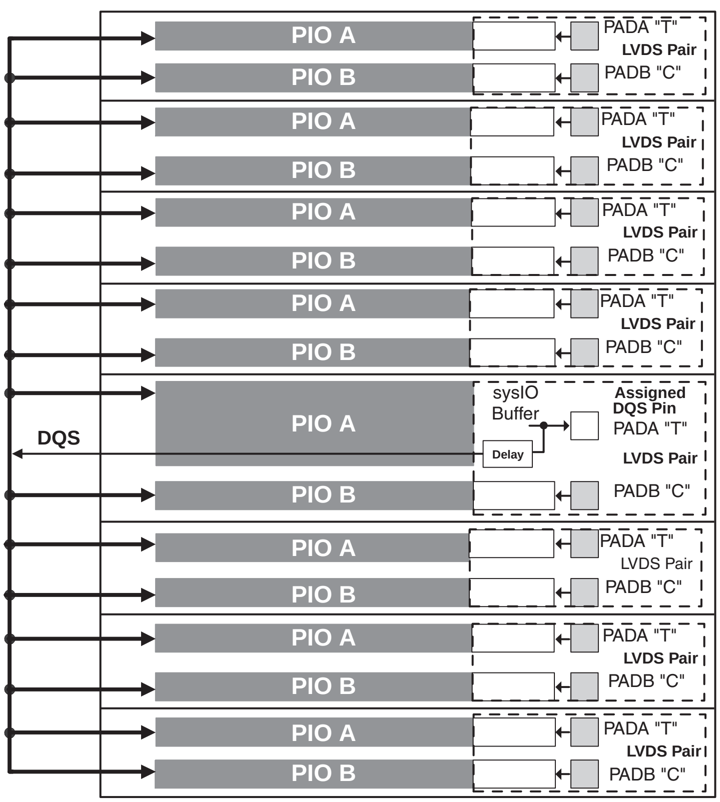
- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Figure 2-32. DQS Local Bus.

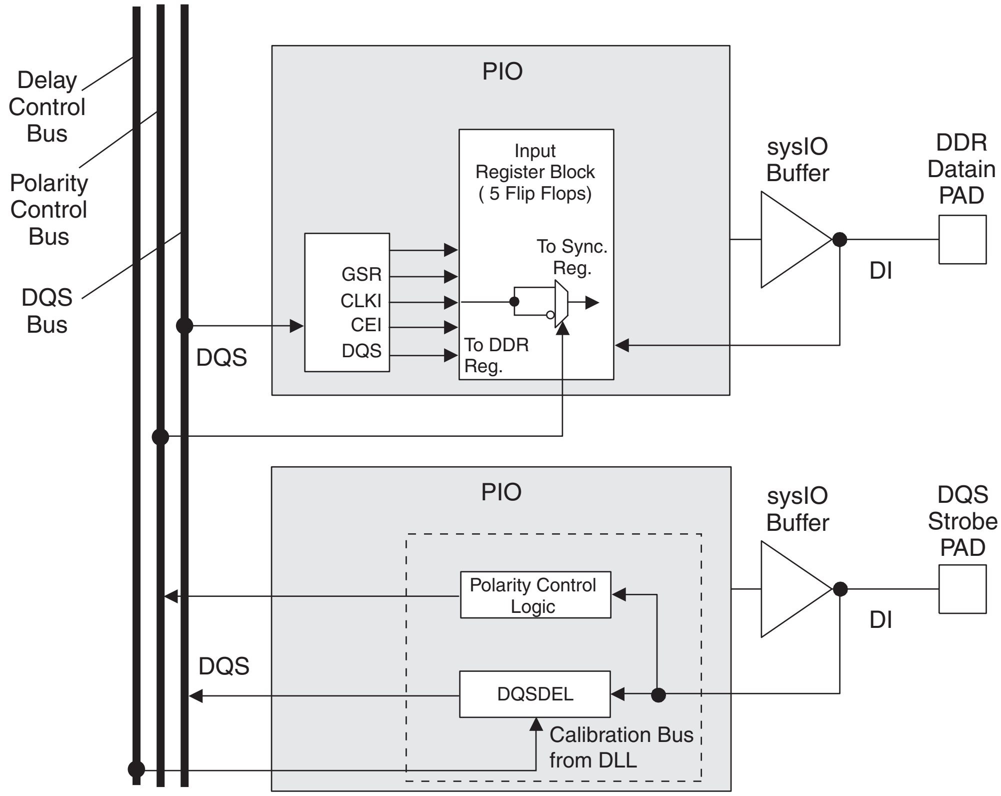
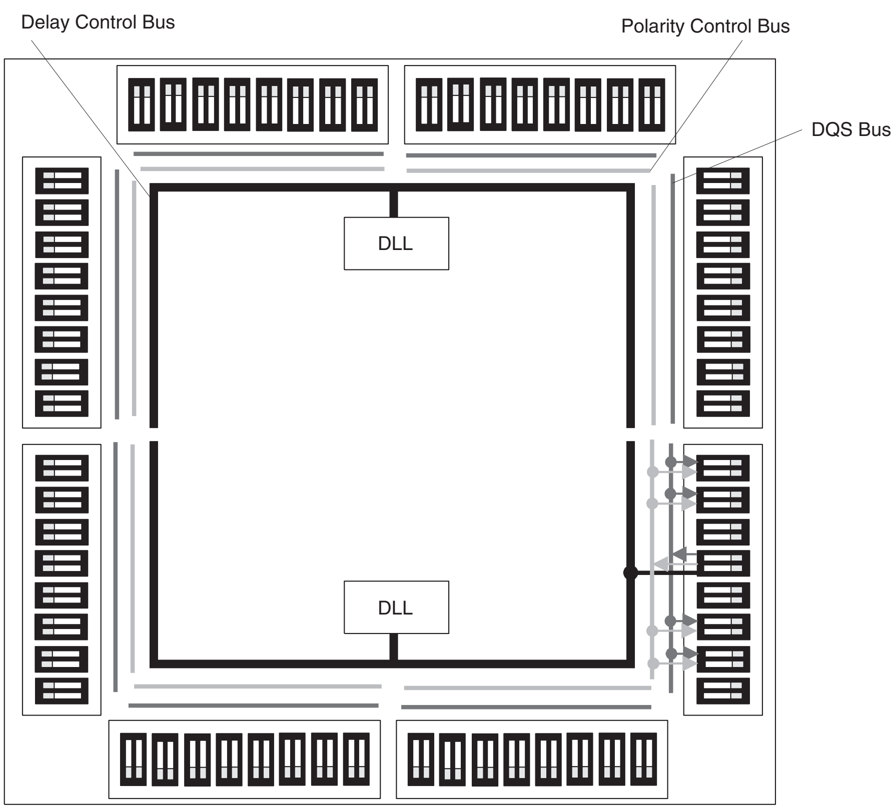


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution



Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master clock for configuration. The oscillator and the master clock run continuously. The default value of the master clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information about the use of this oscillator for configuration, please see the list of technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5*	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Devices	Typ.[6]	Units
I_{CC}	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFECP6/LFEC6	50	mA
		LFECP10/LFEC10	60	mA
		LFECP15/LFEC15	70	mA
		LFECP20/LFEC20	150	mA
		LFECP33/LFEC33	220	mA
I_{CCAUX}	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFECP6/LFEC6	30	mA
		LFECP10/LFEC10	35	mA
		LFECP15/LFEC15	35	mA
		LFECP20/LFEC20	40	mA
		LFECP33/LFEC33	40	mA
I_{CCPLL}	PLL Power Supply Current		12	mA
I_{CCIO}	Bank Power Supply Current[7]	LFEC1	4	mA
		LFEC3	5	mA
		LFECP6/LFEC6	6	mA
		LFECP10/LFEC10	6	mA
		LFECP15/LFEC15	7	mA
		LFECP20/LFEC20	8	mA
		LFECP33/LFEC33	8	mA
I_{CCJ}	V_{CCJ} Power Supply Current		20	mA

1. Until DONE signal is active.
2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.
6. T_J=25°C, power supplies at nominal voltage.
7. Per bank.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

LatticeECP/EC Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.14	—	-0.17	—	-0.20	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing[2, 3]								
t_{SUI_DSP}	Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HI_DSP}	Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.31	—	3.98	—	4.64	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUO_DSP}[4]	Output Register Setup Time	5.54	—	6.64	—	7.75	—	ns
t_{HO_DSP}[4]	Output Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{COI_DSP}[4]	Input Register Clock to Output Time	—	7.50	—	9.00	—	10.50	ns
t_{COP_DSP}[4]	Pipeline Register Clock to Output Time	—	4.66	—	5.60	—	6.53	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	1.47	—	1.77	—	2.06	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.
4. These parameters include the Adder Subtractor block in the path.

Timing v.G 0.30

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (Active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPIN	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP

	LFEC1				LFEC3			
Pin Number	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			NC	-		
6	NC	-			NC	-		
7	NC	-			PL3B	7		
8	NC	-			PL4A	7	T	
9	NC	-			PL4B	7	C	
10	NC	-			PL5A	7	T	
11	NC	-			PL5B	7	C	
12	NC	-			PL6A	7	T	LDQS6
13	NC	-			VCCIO7	7		
14	NC	-			PL6B	7	C	
15	PL3A	7	T		PL7A	7	T	
16	PL3B	7	C		PL7B	7	C	
17	PL4A	7	T		PL8A	7	T	
18	NC	-			NC	-		
19	PL4B	7	C		PL8B	7	C	
20	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
21	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
22	NC	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	NC	-			NC	-		
25	NC	-			NC	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LLM0_PLLT_IN_A
34	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LLM0_PLLC_IN_A
35	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LLM0_PLLT_FB_A
36	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL9A	6	T		PL13A	6	T	
39	PL9B	6	C		PL13B	6	C	
40	PL10A	6	T		PL14A	6	T	
41	GND6	6			GND6	6		
42	PL10B	6	C		PL14B	6	C	

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
43	PL24A	6	T	LDQS24	PL33A	6	T	LDQS33
44	PL24B	6	C		PL33B	6	C	
45	PL25A	6	T		PL34A	6	T	
46	PL25B	6	C		PL34B	6	C	
47	PL26A	6	T		PL35A	6	T	
48	PL26B	6	C		PL35B	6	C	
49	PL27A	6	T	VREF1_6	PL36A	6	T	VREF1_6
50	PL27B	6	C	VREF2_6	PL36B	6	C	VREF2_6
51	VCCIO6	6			VCCIO6	6		
52*	GND5 GND6	-			GND5 GND6	-		
53	VCCIO5	5			VCCIO5	5		
54	PB2A	5	T		PB2A	5	T	
55	PB2B	5	C		PB2B	5	C	
56	PB3A	5	T		PB3A	5	T	
57	PB3B	5	C		PB3B	5	C	
58	PB4A	5	T		PB4A	5	T	
59	PB4B	5	C		PB4B	5	C	
60	PB5A	5	T		PB5A	5	T	
61	PB5B	5	C		PB5B	5	C	
62	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
63	PB6B	5	C		PB6B	5	C	
64	VCCIO5	5			VCCIO5	5		
65	PB10A	5	T		PB18A	5	T	
66	PB10B	5	C		PB18B	5	C	
67	PB11A	5	T		PB19A	5	T	
68	PB11B	5	C		PB19B	5	C	
69	PB12A	5	T		PB20A	5	T	
70	PB12B	5	C		PB20B	5	C	
71	PB13A	5	T		PB21A	5	T	
72	GND5	5			GND5	5		
73	PB13B	5	C		PB21B	5	C	
74	VCCIO5	5			VCCIO5	5		
75	PB14A	5	T	BDQS14	PB22A	5	T	BDQS22
76	PB14B	5	C		PB22B	5	C	
77	PB15A	5	T		PB23A	5	T	
78	PB15B	5	C		PB23B	5	C	
79	PB16A	5	T	VREF2_5	PB24A	5	T	VREF2_5
80	PB16B	5	C	VREF1_5	PB24B	5	C	VREF1_5
81	PB17A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
82	GND5	5			GND5	5		
83	PB17B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
84	VCCAUX	-			VCCAUX	-		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
A10	PT25B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT25A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
C9	PT24B	0	C	VREF1_0	PT24B	0	C	VREF1_0
B9	PT24A	0	T	VREF2_0	PT24A	0	T	VREF2_0
E9	PT23B	0	C		PT23B	0	C	
D9	PT23A	0	T		PT23A	0	T	
D8	PT22B	0	C		PT22B	0	C	
C8	PT22A	0	T	TDQS22	PT22A	0	T	TDQS22
A9	PT21B	0	C		PT21B	0	C	
GND	GND0	0			GND0	0		
A8	PT21A	0	T		PT21A	0	T	
B8	PT20B	0	C		PT20B	0	C	
B7	PT20A	0	T		PT20A	0	T	
D7	PT19B	0	C		PT19B	0	C	
C7	PT19A	0	T		PT19A	0	T	
A7	PT18B	0	C		PT18B	0	C	
A6	PT18A	0	T		PT18A	0	T	
E7	PT17B	0	C		PT17B	0	C	
GND	GND0	0			GND0	0		
E6	PT17A	0	T		PT17A	0	T	
D6	PT16B	0	C		PT16B	0	C	
C6	PT16A	0	T		PT16A	0	T	
B6	PT15B	0	C		PT15B	0	C	
B5	PT15A	0	T		PT15A	0	T	
A5	PT14B	0	C		PT14B	0	C	
A4	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A3	PT13B	0	C		PT13B	0	C	
-	GND0	0			GND0	0		
A2	PT13A	0	T		PT13A	0	T	
B2	PT12B	0	C		PT12B	0	C	
B3	PT12A	0	T		PT12A	0	T	
D5	PT11B	0	C		PT11B	0	C	
C5	PT11A	0	T		PT11A	0	T	
C4	PT10B	0	C		PT10B	0	C	
B4	PT10A	0	T		PT10A	0	T	
GND	GND0	0			GND0	0		
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF4	PB13B	5	C		AF4	PB13B	5	C	
AE5	PB14A	5	T	BDQS14	AE5	PB14A	5	T	BDQS14
AA9	PB14B	5	C		AA9	PB14B	5	C	
AF5	PB15A	5	T		AF5	PB15A	5	T	
Y10	PB15B	5	C		Y10	PB15B	5	C	
AD6	PB16A	5	T		AD6	PB16A	5	T	
AC10	PB16B	5	C		AC10	PB16B	5	C	
AF6	PB17A	5	T		AF6	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AE6	PB17B	5	C		AE6	PB17B	5	C	
AF7	PB18A	5	T		AF7	PB18A	5	T	
AB10	PB18B	5	C		AB10	PB18B	5	C	
AE7	PB19A	5	T		AE7	PB19A	5	T	
AD10	PB19B	5	C		AD10	PB19B	5	C	
AD7	PB20A	5	T		AD7	PB20A	5	T	
AA10	PB20B	5	C		AA10	PB20B	5	C	
AF8	PB21A	5	T		AF8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
AF9	PB21B	5	C		AF9	PB21B	5	C	
AD11	PB22A	5	T	BDQS22	AD11	PB22A	5	T	BDQS22
Y11	PB22B	5	C		Y11	PB22B	5	C	
AE8	PB23A	5	T		AE8	PB23A	5	T	
AC11	PB23B	5	C		AC11	PB23B	5	C	
AF10	PB24A	5	T		AF10	PB24A	5	T	
AB11	PB24B	5	C		AB11	PB24B	5	C	
AE10	PB25A	5	T		AE10	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AE9	PB25B	5	C		AE9	PB25B	5	C	
AA11	PB26A	5	T		AA11	PB26A	5	T	
Y12	PB26B	5	C		Y12	PB26B	5	C	
AE11	PB27A	5	T		AE11	PB27A	5	T	
AF11	PB27B	5	C		AF11	PB27B	5	C	
AF12	PB28A	5	T		AF12	PB28A	5	T	
AE12	PB28B	5	C		AE12	PB28B	5	C	
AD12	PB29A	5	T		AD12	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AC12	PB29B	5	C		AC12	PB29B	5	C	
AA12	PB30A	5	T	BDQS30	AA12	PB30A	5	T	BDQS30
AB12	PB30B	5	C		AB12	PB30B	5	C	
AE13	PB31A	5	T		AE13	PB31A	5	T	
AF13	PB31B	5	C		AF13	PB31B	5	C	
AD13	PB32A	5	T	VREF2_5	AD13	PB32A	5	T	VREF2_5

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M15	GND	-			M15	GND	-		
M16	GND	-			M16	GND	-		
M17	GND	-			M17	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N16	GND	-			N16	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P16	GND	-			P16	GND	-		
P17	GND	-			P17	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
R15	GND	-			R15	GND	-		
R16	GND	-			R16	GND	-		
R17	GND	-			R17	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T12	GND	-			T12	GND	-		
T13	GND	-			T13	GND	-		
T14	GND	-			T14	GND	-		
T15	GND	-			T15	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFECP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFECP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFECP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFECP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFECP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFECP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFECP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFECP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFECP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFECP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFECP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFECP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFECP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFECP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFECP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFECP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFECP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFECP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFECP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFECP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFECP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFECP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFECP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFECP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFECP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFECP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFECP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFECP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFECP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFECP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFECP33E-5F672C	496	-5	fpBGA	672	COM	32.8K