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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	147
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec6e-4qn208c

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)

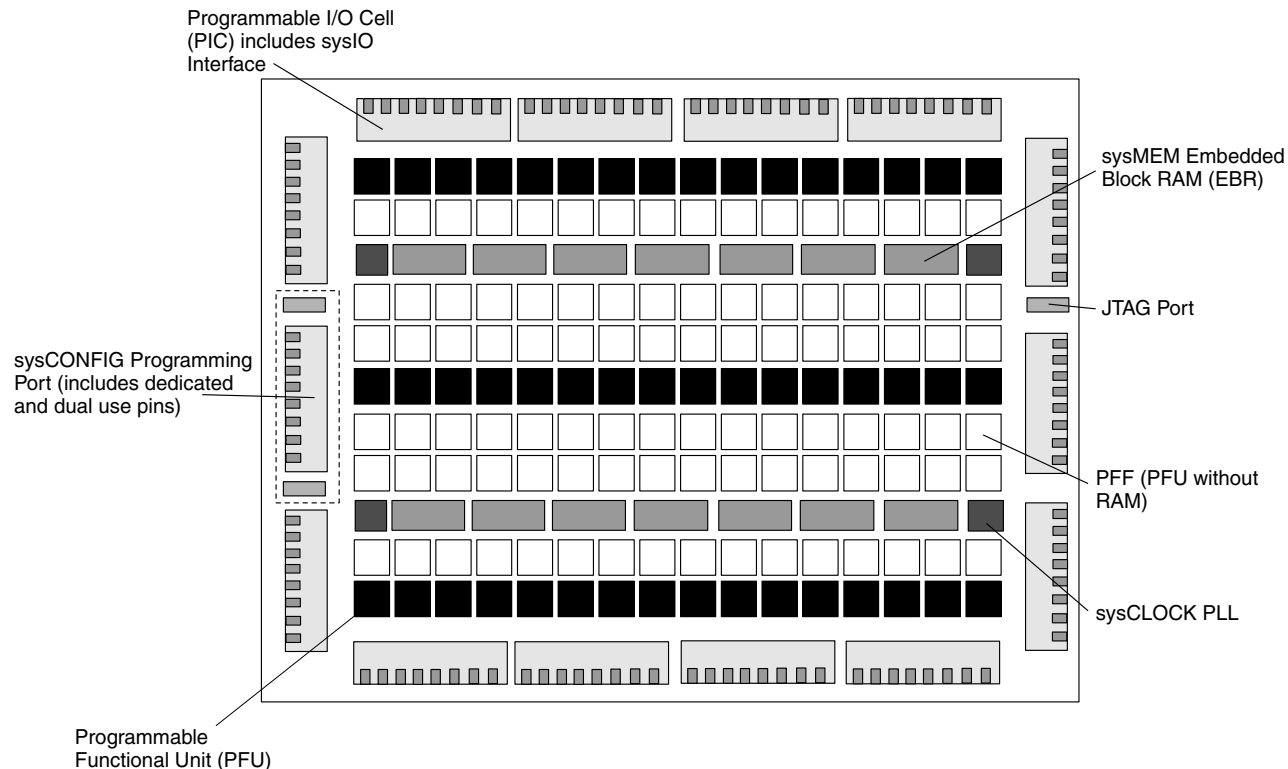


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)

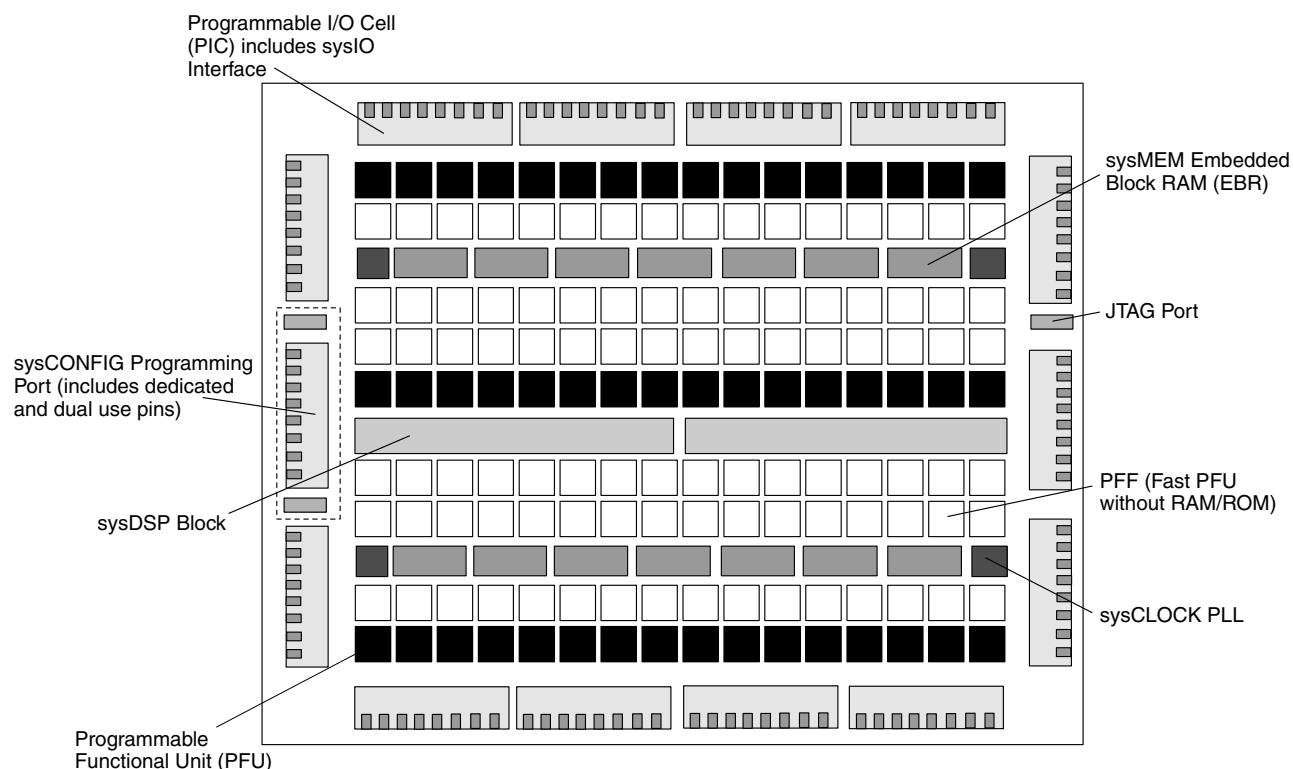
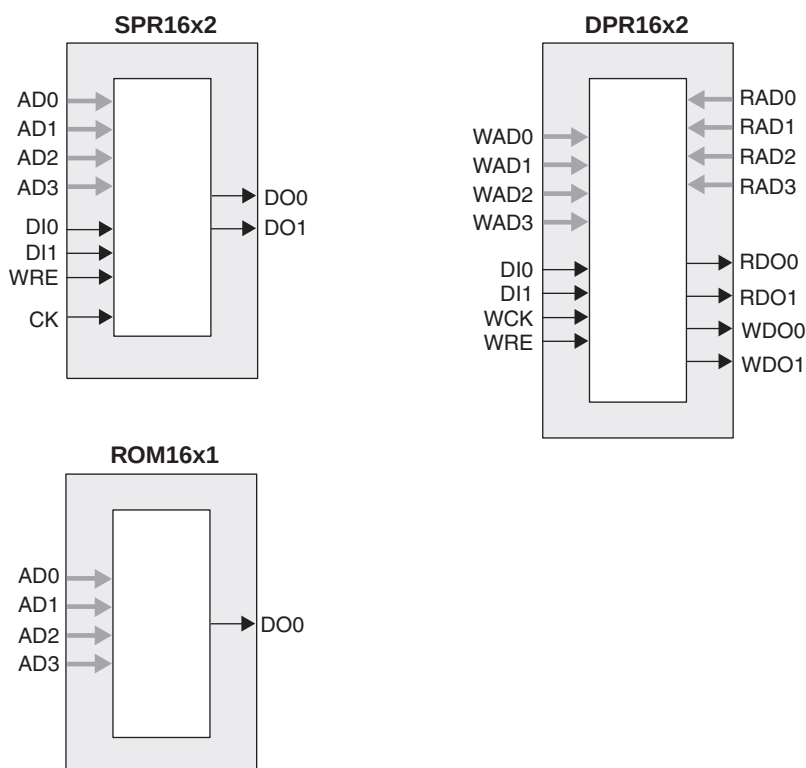


Figure 2-5. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM ¹	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

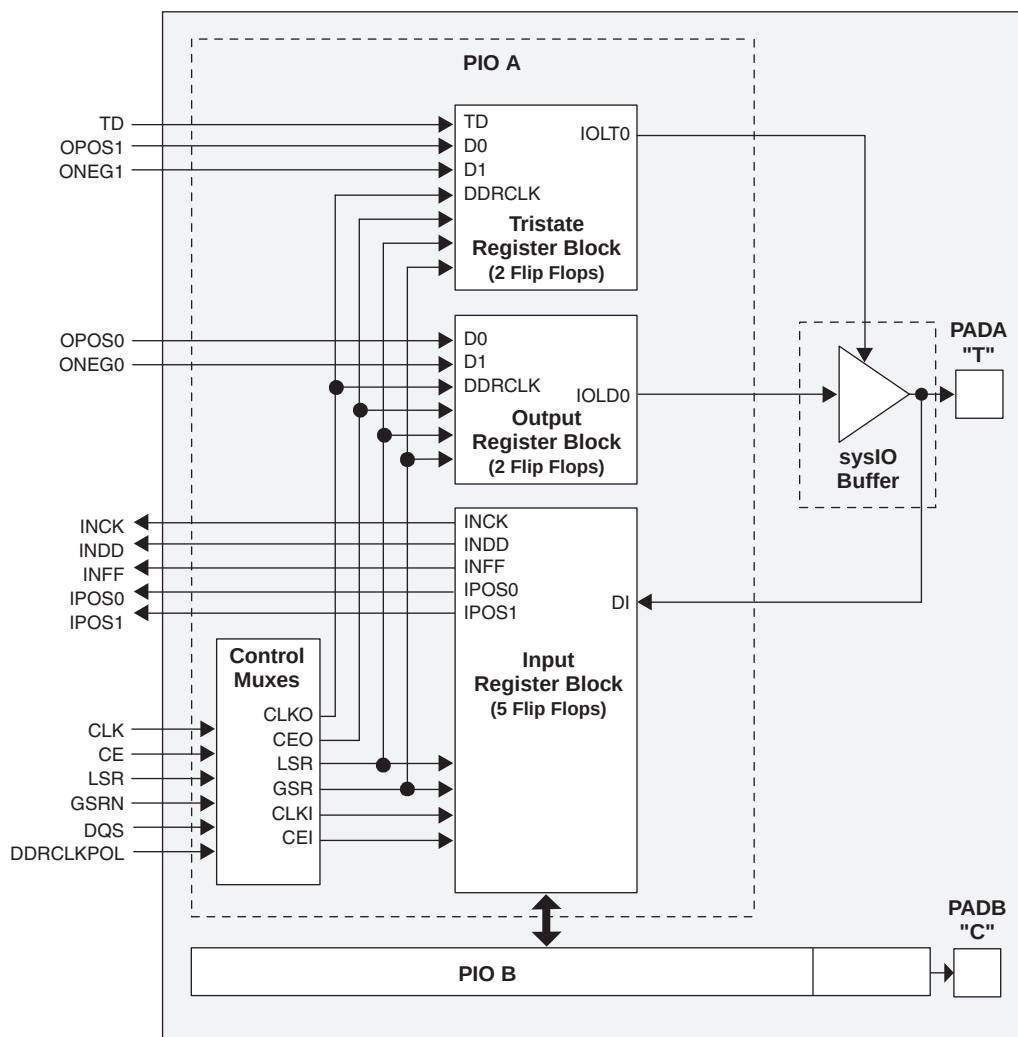
1. These modes are not available in PFF blocks

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

Figure 2-24. PIC Diagram



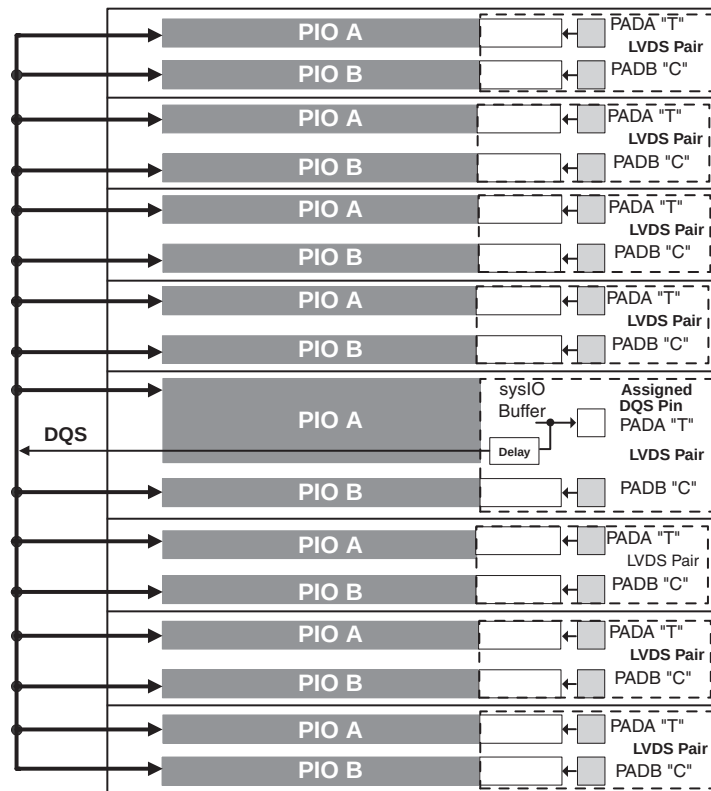
Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDR _X registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
SSTL18 class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
HSTL15 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL15 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8
HSTL18 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	9.6	-9.6
HSTL18 class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL18 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables: T_J °C.

Table 3-5. Delay Derating Table for Internal Blocks

T_J °C Commercial	T_J °C Industrial	Power Supply Voltage		
		1.14V	1.2V	1.26V
—	-40	0.82	0.77	0.71
—	-25	0.82	0.76	0.71
0	20	0.89	0.83	0.78
25	45	0.93	0.87	0.81
85	105	1.00	0.94	0.89

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL) ¹									
t _{CO} ⁷	Clock to Output - PIO Output Register	LFEC1	—	5.09	—	6.11	—	7.13	ns
		LFEC3	—	5.71	—	6.85	—	7.99	ns
		LFEC6	—	5.60	—	6.72	—	7.84	ns
		LFEC10	—	5.47	—	6.57	—	7.66	ns
		LFEC15	—	5.67	—	6.81	—	7.94	ns
		LFEC20	—	5.89	—	7.07	—	8.25	ns
		LFEC33	—	6.19	—	7.42	—	8.66	ns
t _{SU} ⁷	Clock to Data Setup - PIO Input Register	LFEC1	-0.08	—	-0.10	—	-0.12	—	ns
		LFEC3	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC6	-0.63	—	-0.76	—	-0.89	—	ns
		LFEC10	-0.43	—	-0.52	—	-0.61	—	ns
		LFEC15	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC20	-0.88	—	-1.06	—	-1.24	—	ns
		LFEC33	-1.12	—	-1.34	—	-1.56	—	ns
t _H ⁷	Clock to Data Hold - PIO Input Register	LFEC1	2.19	—	2.62	—	3.06	—	ns
		LFEC3	2.80	—	3.36	—	3.92	—	ns
		LFEC6	2.69	—	3.23	—	3.77	—	ns
		LFEC10	2.56	—	3.08	—	3.59	—	ns
		LFEC15	2.76	—	3.32	—	3.87	—	ns
		LFEC20	2.99	—	3.58	—	4.18	—	ns
		LFEC33	3.28	—	3.93	—	4.59	—	ns
t _{SU_DEL} ⁷	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC1	3.36	—	4.03	—	4.70	—	ns
		LFEC3	2.74	—	3.29	—	3.84	—	ns
		LFEC6	2.81	—	3.37	—	3.93	—	ns
		LFEC10	3.01	—	3.61	—	4.21	—	ns
		LFEC15	2.74	—	3.29	—	3.83	—	ns
		LFEC20	2.56	—	3.07	—	3.58	—	ns
		LFEC33	2.32	—	2.79	—	3.25	—	ns
t _{H_DEL} ⁷	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC1	-1.31	—	-1.57	—	-1.83	—	ns
		LFEC3	-0.70	—	-0.83	—	-0.97	—	ns
		LFEC6	-0.80	—	-0.96	—	-1.12	—	ns
		LFEC10	-0.93	—	-1.12	—	-1.30	—	ns
		LFEC15	-0.73	—	-0.88	—	-1.02	—	ns
		LFEC20	-0.51	—	-0.61	—	-0.71	—	ns
		LFEC33	-0.22	—	-0.26	—	-0.30	—	ns
f _{MAX_IO} ²	Clock Frequency of I/O and PFU Register	All	—	420	—	378	—	340	Mhz
DDR I/O Pin Parameters ^{3, 4, 5}									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI

LatticeECP/EC Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUC_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.14	—	-0.17	—	-0.20	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t_{SUI_DSP}	Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HI_DSP}	Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.31	—	3.98	—	4.64	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{SUO_DSP}^4$	Output Register Setup Time	5.54	—	6.64	—	7.75	—	ns
$t_{HO_DSP}^4$	Output Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{COI_DSP}^4$	Input Register Clock to Output Time	—	7.50	—	9.00	—	10.50	ns
$t_{COP_DSP}^4$	Pipeline Register Clock to Output Time	—	4.66	—	5.60	—	6.53	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	1.47	—	1.77	—	2.06	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.

4. These parameters include the Adder Subtractor block in the path.

Timing v.G 0.30

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

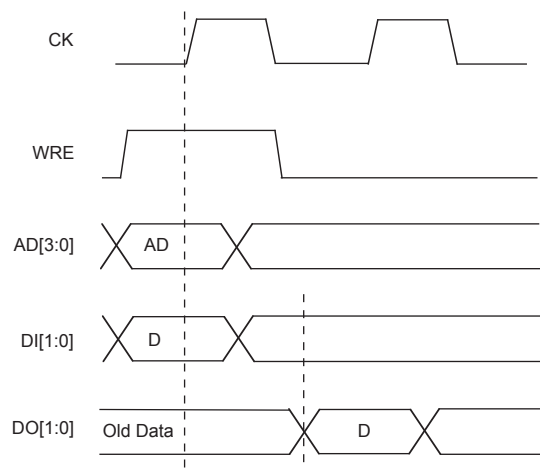
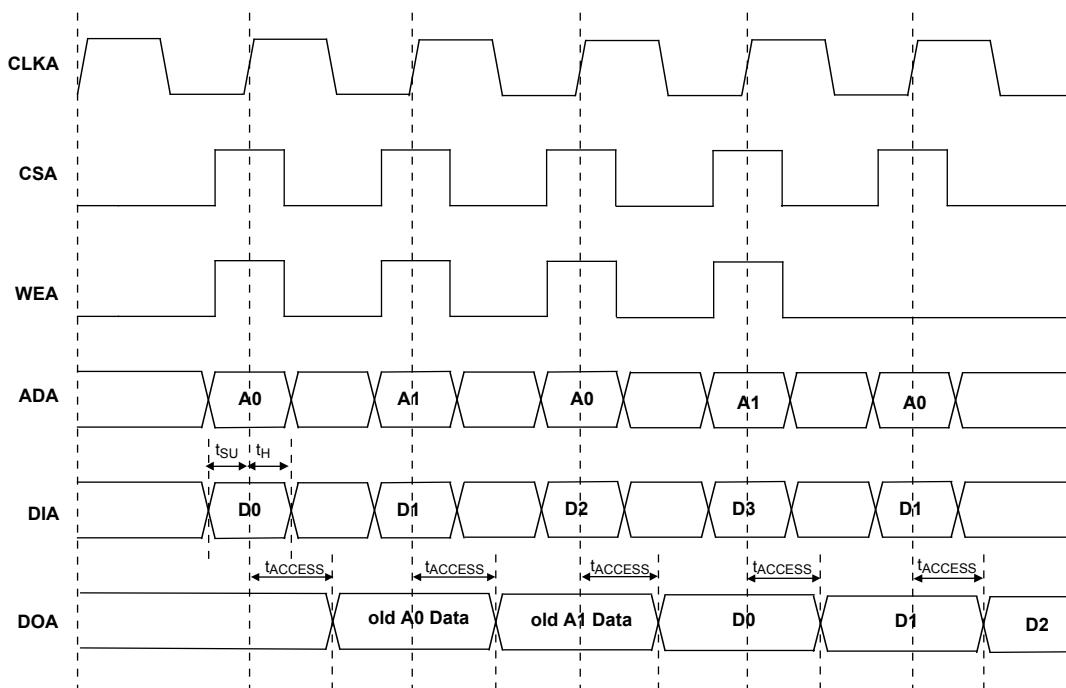


Figure 3-7. Slice Single /Dual Port Read Cycle Timing

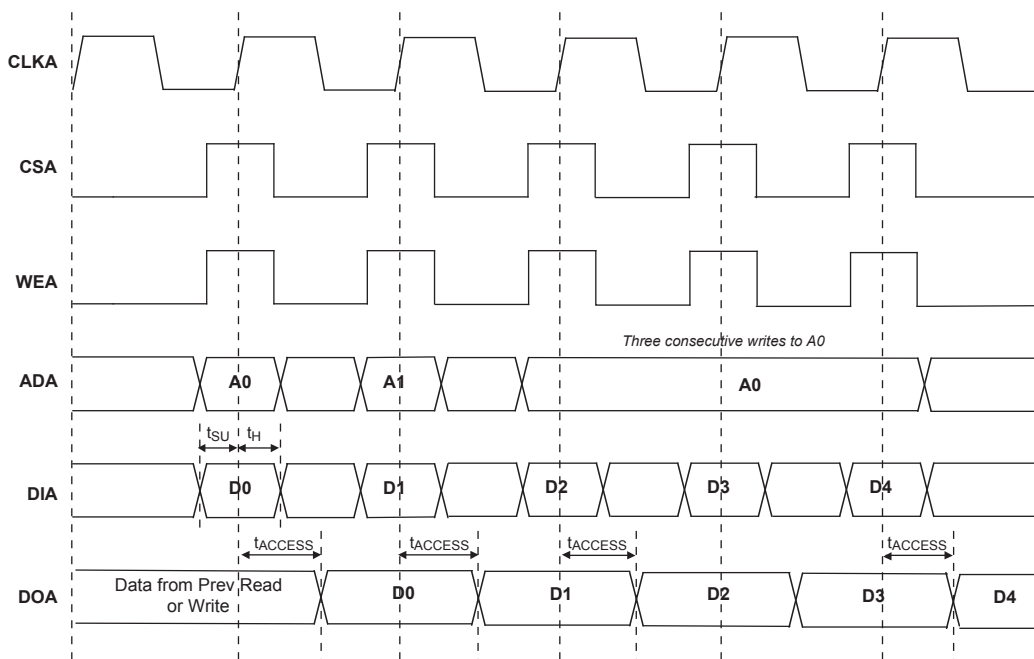


Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Pin Information Summary (Cont.)

		LFEC/EC15		LFEC/EC20		LFEC/EC33	
Pin Type		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V _{CC}		10	20	20	32	16	28
V _{CCAUX}		2	12	12	20	12	20
V _{CCPLL}		0	0	0	0	4	4
V _{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V _{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC3 and LFEC6/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFEC6/EC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFEC3 and LFEC6/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFEC6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
D7	PT11B	0	C		PT11B	0	C	
C7	PT11A	0	T		PT11A	0	T	
A7	PT10B	0	C		PT10B	0	C	
A6	PT10A	0	T		PT10A	0	T	
E7	PT9B	0	C		PT9B	0	C	
GND	GND0	0			GND0	0		
E6	PT9A	0	T		PT9A	0	T	
D6	PT8B	0	C		PT8B	0	C	
C6	PT8A	0	T		PT8A	0	T	
B6	PT7B	0	C		PT7B	0	C	
B5	PT7A	0	T		PT7A	0	T	
A5	PT6B	0	C		PT6B	0	C	
A4	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
A3	PT5B	0	C		PT5B	0	C	
A2	PT5A	0	T		PT5A	0	T	
B2	PT4B	0	C		PT4B	0	C	
B3	PT4A	0	T		PT4A	0	T	
D5	PT3B	0	C		PT3B	0	C	
C5	PT3A	0	T		PT3A	0	T	
C4	PT2B	0	C		PT2B	0	C	
B4	PT2A	0	T		PT2A	0	T	
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
Y13	PB40A	4	T		Y13	PB40A	4	T	
V14	PB40B	4	C	D5/SPID2	V14	PB40B	4	C	D5/SPID2
AA13	PB41A	4	T		AA13	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AB13	PB41B	4	C	D6/SPID1	AB13	PB41B	4	C	D6/SPID1
AA14	PB42A	4	T		AA14	PB42A	4	T	
Y14	PB42B	4	C		Y14	PB42B	4	C	
Y15	PB43A	4	T		Y15	PB43A	4	T	
W15	PB43B	4	C		W15	PB43B	4	C	
V15	PB44A	4	T		V15	PB44A	4	T	
T14	PB44B	4	C		T14	PB44B	4	C	
AB14	PB45A	4	T		AB14	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AB15	PB45B	4	C		AB15	PB45B	4	C	
AB16	PB46A	4	T	BDQS46	AB16	PB46A	4	T	BDQS46
AA15	PB46B	4	C		AA15	PB46B	4	C	
AB17	PB47A	4	T		AB17	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AB18	PB48A	4	T		AB18	PB48A	4	T	
AA17	PB48B	4	C		AA17	PB48B	4	C	
AB19	PB49A	4	T		AB19	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AA18	PB49B	4	C		AA18	PB49B	4	C	
W16	PB50A	4	T		W16	PB50A	4	T	
U15	PB50B	4	C		U15	PB50B	4	C	
V16	PB51A	4	T		V16	PB51A	4	T	
U16	PB51B	4	C		U16	PB51B	4	C	
Y17	PB52A	4	T		Y17	PB52A	4	T	
V17	PB52B	4	C		V17	PB52B	4	C	
AB20	PB53A	4	T		AB20	PB53A	4	T	
GND	GND4	4			GND	GND4	4		
AA19	PB53B	4	C		AA19	PB53B	4	C	
Y16	PB54A	4	T	BDQS54	Y16	PB54A	4	T	BDQS54
W17	PB54B	4	C		W17	PB54B	4	C	
AA20	PB55A	4	T		AA20	PB55A	4	T	
Y19	PB55B	4	C		Y19	PB55B	4	C	
Y18	PB56A	4	T		Y18	PB56A	4	T	
W18	PB56B	4	C		W18	PB56B	4	C	
T17	PB57A	4	T		T17	PB57A	4	T	
U17	PB57B	4	C		U17	PB57B	4	C	
GND	-	-			GND	GND4	4		
GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND4	4		
GND	-	-			GND	GND3	3		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
N22	PR30A	3	T		N22	PR42A	3	T	
N19	PR29B	3	C		N19	PR41B	3	C	
N18	PR29A	3	T		N18	PR41A	3	T	
M21	PR28B	3	C		M21	PR40B	3	C	
L20	PR28A	3	T	RDQS28	L20	PR40A	3	T	RDQS40
L21	PR27B	3	C		L21	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M20	PR27A	3	T		M20	PR39A	3	T	
M18	PR26B	3	C		M18	PR38B	3	C	
M19	PR26A	3	T		M19	PR38A	3	T	
M22	PR25B	3	C		M22	PR37B	3	C	
L22	PR25A	3	T		L22	PR37A	3	T	
K22	PR24B	3	C		K22	PR36B	3	C	
K21	PR24A	3	T		K21	PR36A	3	T	
J22	PR22B	2	C	PCLKC2_0	J22	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
J21	PR22A	2	T	PCLKT2_0	J21	PR34A	2	T	PCLKT2_0
H22	PR21B	2	C		H22	PR33B	2	C	
H21	PR21A	2	T		H21	PR33A	2	T	
L19	PR20B	2	C		L19	PR32B	2	C	
L18	PR20A	2	T		L18	PR32A	2	T	
K20	PR19B	2	C		K20	PR31B	2	C	
J20	PR19A	2	T	RDQS19	J20	PR31A	2	T	RDQS31
K19	PR18B	2	C		K19	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
K18	PR18A	2	T		K18	PR30A	2	T	
G22	PR17B	2	C		G22	PR29B	2	C	
F22	PR17A	2	T		F22	PR29A	2	T	
F21	PR16B	2	C		F21	PR28B	2	C	
E22	PR16A	2	T		E22	PR28A	2	T	
E21	PR15B	2	C		E21	PR27B	2	C	
D22	PR15A	2	T		D22	PR27A	2	T	
G21	PR14B	2	C		G21	PR26B	2	C	
G20	PR14A	2	T		G20	PR26A	2	T	
GND	GND2	2			GND	GND2	2		
J18	PR13B	2	C		J18	PR25B	2	C	
H19	PR13A	2	T		H19	PR25A	2	T	
J19	PR12B	2	C		J19	PR24B	2	C	
H20	PR12A	2	T		H20	PR24A	2	T	
H17	PR11B	2	C		H17	PR23B	2	C	
H18	PR11A	2	T		H18	PR23A	2	T	RDQS23
D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
GND	-	-			GND	GND2	2		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR17A	2	T	RUM0_PLLT_FB_A
G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR16B	2	C	RUM0_PLLC_IN_A
G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR16A	2	T	RUM0_PLLT_IN_A
F20	PR7B	2	C		F20	PR15B	2	C	
F19	PR7A	2	T		F19	PR15A	2	T	
E20	PR6B	2	C		E20	PR14B	2	C	
D20	PR6A	2	T	RDQS6	D20	PR14A	2	T	RDQS14
C21	PR5B	2	C		C21	PR13B	2	C	
GND	-	-			GND	GND2	2		
C20	PR5A	2	T		C20	PR13A	2	T	
F18	PR4B	2	C		F18	PR12B	2	C	
E18	PR4A	2	T		E18	PR12A	2	T	
B22	PR3B	2	C		B22	PR11B	2	C	
B21	PR3A	2	T		B21	PR11A	2	T	
GND	-	-			GND	GND2	2		
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
GND	-	-			GND	GND1	1		
G17	PT57B	1	C		G17	PT57B	1	C	
GND	-	-			GND	GND1	1		
F17	PT57A	1	T		F17	PT57A	1	T	
D18	PT56B	1	C		D18	PT56B	1	C	
C18	PT56A	1	T		C18	PT56A	1	T	
C19	PT55B	1	C		C19	PT55B	1	C	
B20	PT55A	1	T		B20	PT55A	1	T	
D17	PT54B	1	C		D17	PT54B	1	C	
C16	PT54A	1	T	TDQS54	C16	PT54A	1	T	TDQS54
B19	PT53B	1	C		B19	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
A20	PT53A	1	T		A20	PT53A	1	T	
E17	PT52B	1	C		E17	PT52B	1	C	
C17	PT52A	1	T		C17	PT52A	1	T	
F16	PT51B	1	C		F16	PT51B	1	C	
E16	PT51A	1	T		E16	PT51A	1	T	
F15	PT50B	1	C		F15	PT50B	1	C	
D16	PT50A	1	T		D16	PT50A	1	T	
B18	PT49B	1	C		B18	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
A19	PT49A	1	T		A19	PT49A	1	T	
B17	PT48B	1	C		B17	PT48B	1	C	
A18	PT48A	1	T		A18	PT48A	1	T	
B16	PT47B	1	C		B16	PT47B	1	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
H7	VCCAUX	-			H7	VCCAUX	-		
J19	VCCAUX	-			J19	VCCAUX	-		
J8	VCCAUX	-			J8	VCCAUX	-		
K7	VCCAUX	-			K7	VCCAUX	-		
L20	VCCAUX	-			L20	VCCAUX	-		
M20	VCCAUX	-			M20	VCCAUX	-		
M7	VCCAUX	-			M7	VCCAUX	-		
N20	VCCAUX	-			N20	VCCAUX	-		
P20	VCCAUX	-			P20	VCCAUX	-		
P7	VCCAUX	-			P7	VCCAUX	-		
T20	VCCAUX	-			T20	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
V19	VCCAUX	-			V19	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
W20	VCCAUX	-			W20	VCCAUX	-		
Y13	VCCAUX	-			Y13	VCCAUX	-		
Y7	VCCAUX	-			Y7	VCCAUX	-		
K19	VCC ¹	-			K19	VCCPLL	-		
L8	VCC ¹	-			L8	VCCPLL	-		
U19	VCC ¹	-			U19	VCCPLL	-		
U8	VCC ¹	-			U8	VCCPLL	-		

 1. Tied to V_{CCPLL}.

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K