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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec6e-5fn256c

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

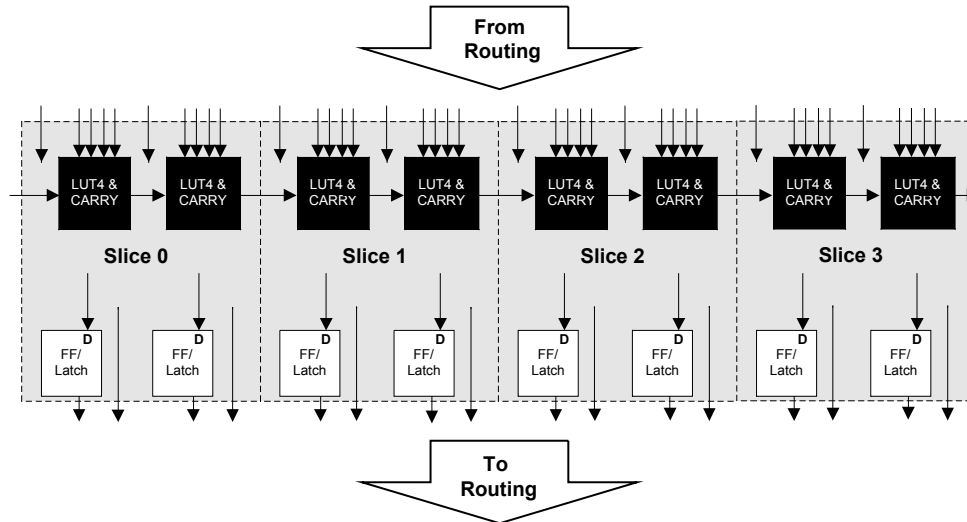
Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

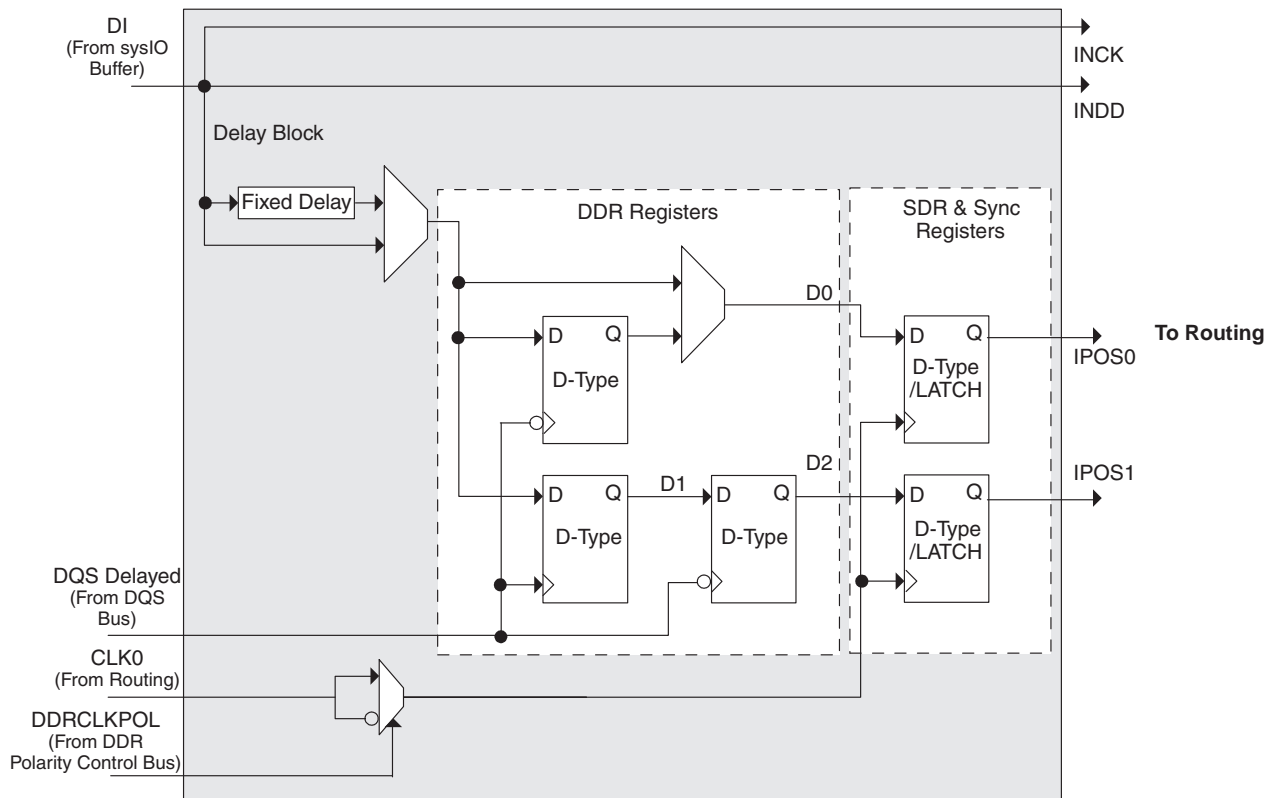
Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-27 shows the input register waveforms for DDR operation and Figure 2-28 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Diagram



Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

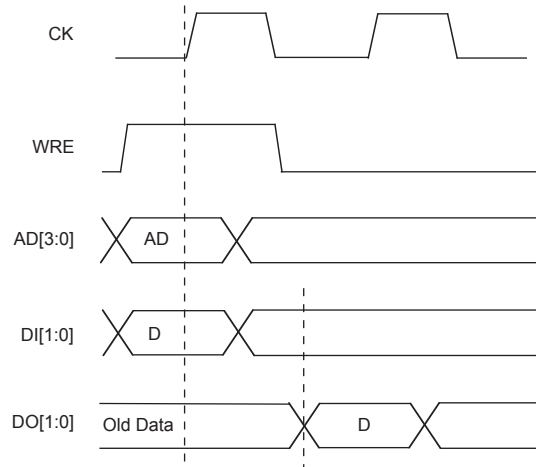


Figure 3-7. Slice Single /Dual Port Read Cycle Timing

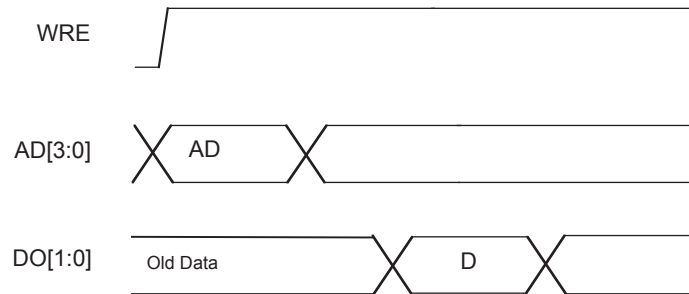
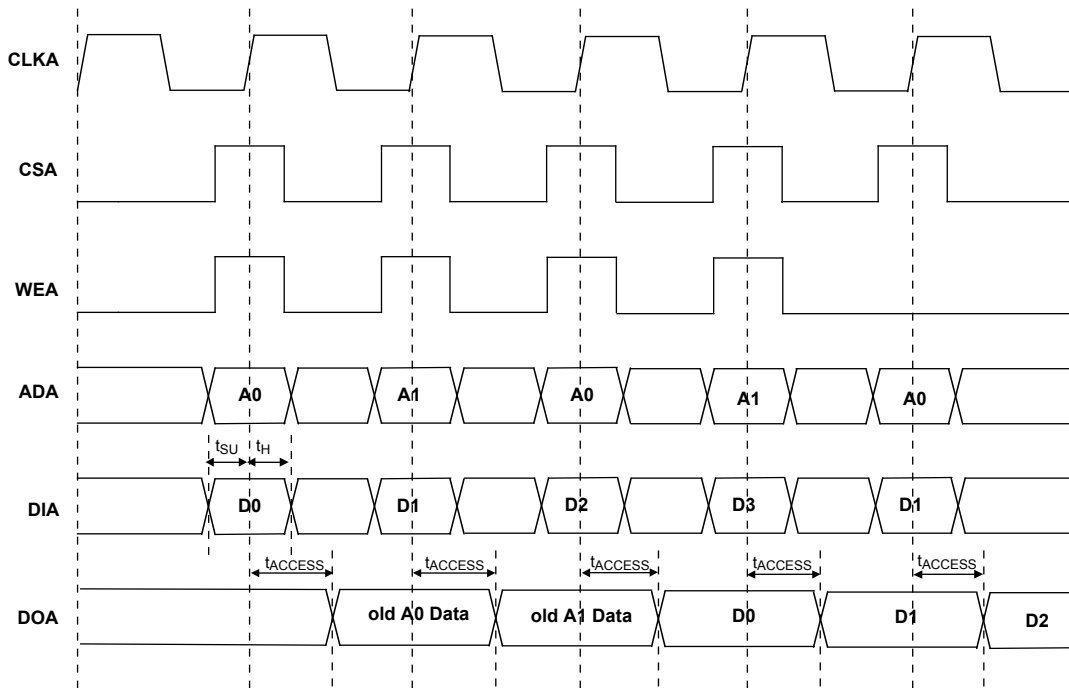
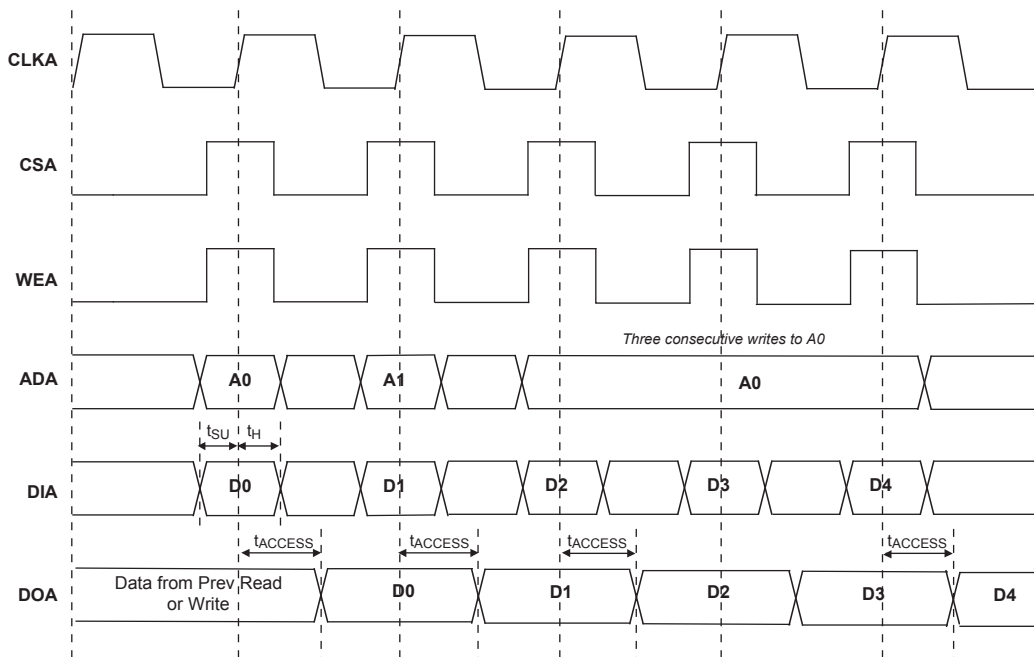


Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP/EC Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_II	HSTL_15 class II	0.10	0.12	0.14	ns
HSTL15_III	HSTL_15 class III	0.10	0.12	0.14	ns
HSTL15D_I	Differential HSTL 15 class I	0.08	0.10	0.11	ns
HSTL15D_III	Differential HSTL 15 class III	0.10	0.12	0.14	ns
SSTL33_I	SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33_II	SSTL_3 class II	0.40	0.48	0.56	ns
SSTL33D_I	Differential SSTL_3 class I	-0.05	-0.06	-0.07	ns
SSTL33D_II	Differential SSTL_3 class II	0.40	0.48	0.56	ns
SSTL25_I	SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25_II	SSTL_2 class II	0.25	0.30	0.35	ns
SSTL25D_I	Differential SSTL_2 class I	0.05	0.07	0.08	ns
SSTL25D_II	Differential SSTL_2 class II	0.25	0.30	0.35	ns
SSTL18_I	SSTL_1.8 class I	0.01	0.01	0.01	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.01	0.01	0.01	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.09	0.11	0.13	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.07	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.03	-0.04	-0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.36	0.43	0.51	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.28	0.33	0.39	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.09	0.11	0.13	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.07	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	-0.03	-0.04	-0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.36	0.43	0.51	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.28	0.33	0.39	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.18	0.21	0.25	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.10	0.12	0.14	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.22	0.26	0.31	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.14	0.16	0.19	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.15	0.18	0.21	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.06	0.08	0.09	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.01	0.01	0.01	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.16	0.19	0.22	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.26	0.31	0.36	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.04	0.04	0.05	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.36	0.43	0.50	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.08	0.10	0.11	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	0.36	0.43	0.50	ns
PCI33	PCI33	1.05	1.26	1.46	ns

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Conditions table of this document.

3. All other standards according to the appropriate specification.

Timing v.G 0.30

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t _{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t _{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t _{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t _{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t _{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t _{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t _{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t _{DCB}	CCLK to BUSY Delay Time	—		12	ns
t _{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t _{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t _{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t _{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t _{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t _{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t _{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t _{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t _{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t _{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t _{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t _{ICFG}	Minimum Vcc to INIT High	—		50	ms
t _{VMC}	Time from t _{ICFG} to Valid Master Clock	—		2	us
t _{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t _{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t _{DINIT}	INIT Low Time	—		1	ms
t _{DPPINIT}	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t _{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t _{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t _{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t _{SUCFG}	CFG to INITN Setup Time	100		—	ns
t _{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t _{CFGX}	Init High to CCLK Low	—		80	ns
t _{CSSPI}	Init High to CSSPIN Low	—		2	us
t _{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t _{SOCDO}	CCLK Low to Output Valid	—		15	ns

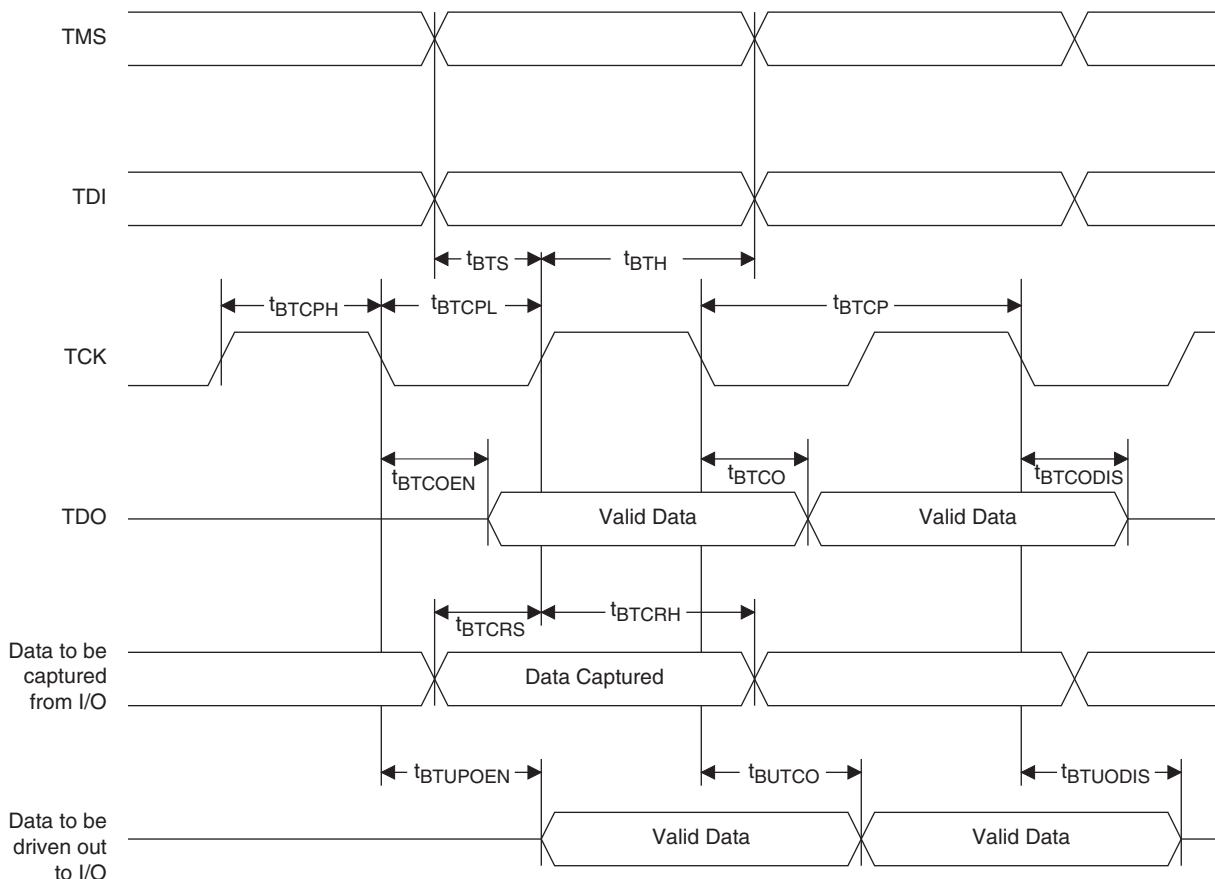
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.G 0.30

Figure 3-20. JTAG Port Timing Waveforms





LatticeECP/EC Family Data Sheet

Pinout Information

September 2012

Data Sheet

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.</p> <p>During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins.
V _{CCIOx}	—	Power supply pins for I/O bank x. Dedicated pins.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES	—	10K ohm +/-1% resistor must be connected between this pad and ground.
V _{CCPLL}	—	Power supply pin for PLL. Applicable to ECP/EC33 device.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	I	Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_PLL[T, C]_FB_A	I	Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.

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LFEC1, LFEC3, LFEC6/EC6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFEC1				LFEC3				LFEC6/EC6			
	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function
99	VCC	-			VCC	-			VCC	-		
100	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
101	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
102	PR4B	2	C		PR8B	2	C		PR8B	2	C	
103	PR4A	2	T		PR8A	2	T		PR8A	2	T	
104	PR3B	2	C		PR7B	2	C		PR7B	2	C	
105	PR3A	2	T		PR7A	2	T		PR7A	2	T	
106	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
107	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
108	VCCIO2	2			VCCIO2	2			VCCIO2	2		
109*	GND1 GND2	-			GND1 GND2	-			GND1 GND2	-		
110	VCCIO1	1			VCCIO1	1			VCCIO1	1		
111	PT17B	1	C		PT25B	1	C		PT25B	1	C	
112	PT17A	1	T		PT25A	1	T		PT25A	1	T	
113	PT15A	1			PT23A	1			PT23A	1		
114	PT14B	1	C		PT22B	1	C		PT22B	1	C	
115	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
116	PT13B	1	C		PT21B	1	C		PT21B	1	C	
117	GND1	1			GND1	1			GND1	1		
118	PT13A	1	T		PT21A	1	T		PT21A	1	T	
119	PT12B	1	C		PT20B	1	C		PT20B	1	C	
120	PT12A	1	T		PT20A	1	T		PT20A	1	T	
121	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
122	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
123	PT10B	1	C		PT18B	1	C		PT18B	1	C	
124	PT10A	1	T		PT18A	1	T		PT18A	1	T	
125	VCCIO1	1			VCCIO1	1			VCCIO1	1		
126	VCCAUX	-			VCCAUX	-			VCCAUX	-		
127	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
128	GND0	0			GND0	0			GND0	0		
129	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
130	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
131	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
132	PT7B	0	C		PT15B	0	C		PT15B	0	C	
133	PT7A	0	T		PT15A	0	T		PT15A	0	T	
134	PT6B	0	C		PT14B	0	C		PT14B	0	C	
135	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
136	VCCIO0	0			VCCIO0	0			VCCIO0	0		
137	PT5B	0	C		PT13B	0	C		PT13B	0	C	
138	PT5A	0	T		PT13A	0	T		PT13A	0	T	
139	PT4B	0	C		PT12B	0	C		PT12B	0	C	
140	PT4A	0	T		PT12A	0	T		PT12A	0	T	
141	PT2B	0	C		PT10B	0	C		PT10B	0	C	
142	PT2A	0	T		PT10A	0	T		PT10A	0	T	
143	VCCIO0	0			VCCIO0	0			VCCIO0	0		
144*	GND0 GND7	-			GND0 GND7	-			GND0 GND7	-		

*Double bonded to the pin.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
43	PL11A	6	T	LDQS11	PL15A	6	T	LDQS15
44	PL11B	6	C		PL15B	6	C	
45	PL12A	6	T		PL16A	6	T	
46	PL12B	6	C		PL16B	6	C	
47	PL13A	6	T		PL17A	6	T	
48	PL13B	6	C		PL17B	6	C	
49	PL14A	6	T	VREF1_6	PL18A	6	T	VREF1_6
50	PL14B	6	C	VREF2_6	PL18B	6	C	VREF2_6
51	VCCIO6	6			VCCIO6	6		
52*	GND5 GND6	-			GND5 GND6	-		
53	VCCIO5	5			VCCIO5	5		
54	NC	-			PB2A	5	T	
55	NC	-			PB2B	5	C	
56	NC	-			PB3A	5	T	
57	NC	-			PB3B	5	C	
58	NC	-			PB4A	5	T	
59	NC	-			PB4B	5	C	
60	NC	-			PB5A	5	T	
61	NC	-			PB5B	5	C	
62	NC	-			PB6A	5	T	BDQS6
63	NC	-			PB6B	5	C	
64	NC	-			VCCIO5	5		
65	PB2A	5	T		PB10A	5	T	
66	PB2B	5	C		PB10B	5	C	
67	PB3A	5	T		PB11A	5	T	
68	PB3B	5	C		PB11B	5	C	
69	PB4A	5	T		PB12A	5	T	
70	PB4B	5	C		PB12B	5	C	
71	PB5A	5	T		PB13A	5	T	
72	NC	-			GND5	5		
73	PB5B	5	C		PB13B	5	C	
74	VCCIO5	5			VCCIO5	5		
75	PB6A	5	T	BDQS6	PB14A	5	T	BDQS14
76	PB6B	5	C		PB14B	5	C	
77	PB7A	5	T		PB15A	5	T	
78	PB7B	5	C		PB15B	5	C	
79	PB8A	5	T	VREF2_5	PB16A	5	T	VREF2_5
80	PB8B	5	C	VREF1_5	PB16B	5	C	VREF1_5
81	PB9A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
82	GND5	5			GND5	5		
83	PB9B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
84	VCCAUX	-			VCCAUX	-		

LFEC6/EC6, LFEC6/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC6/LFEC6				LFEC10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
169	PT21A	1	T		PT29A	1	T	
170	PT20B	1	C		PT28B	1	C	
171	PT20A	1	T		PT28A	1	T	
172	PT19B	1	C	VREF2_1	PT27B	1	C	VREF2_1
173	PT19A	1	T	VREF1_1	PT27A	1	T	VREF1_1
174	PT18B	1	C		PT26B	1	C	
175	PT18A	1	T		PT26A	1	T	
176	VCCIO1	1			VCCIO1	1		
177	VCCAUX	-			VCCAUX	-		
178	PT17B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
179	GND0	0			GND0	0		
180	PT17A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
181	PT16B	0	C	VREF1_0	PT24B	0	C	VREF1_0
182	PT16A	0	T	VREF2_0	PT24A	0	T	VREF2_0
183	PT15B	0	C		PT23B	0	C	
184	PT15A	0	T		PT23A	0	T	
185	PT14B	0	C		PT22B	0	C	
186	PT14A	0	T	TDQS14	PT22A	0	T	TDQS22
187	VCCIO0	0			VCCIO0	0		
188	PT13B	0	C		PT21B	0	C	
189	GND0	0			GND0	0		
190	PT13A	0	T		PT21A	0	T	
191	PT12B	0	C		PT20B	0	C	
192	PT12A	0	T		PT20A	0	T	
193	PT11B	0	C		PT19B	0	C	
194	PT11A	0	T		PT19A	0	T	
195	PT10B	0	C		PT18B	0	C	
196	PT10A	0	T		PT18A	0	T	
197	VCCIO0	0			VCCIO0	0		
198	PT6B	0	C		PT6B	0	C	
199	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
200	PT5B	0	C		PT5B	0	C	
201	PT5A	0	T		PT5A	0	T	
202	PT4B	0	C		PT4B	0	C	
203	PT4A	0	T		PT4A	0	T	
204	PT3B	0	C		PT3B	0	C	
205	PT3A	0	T		PT3A	0	T	
206	PT2B	0	C		PT2B	0	C	
207	PT2A	0	T		PT2A	0	T	
208	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:
 484 fpBGA**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
C3	NC	-			C3	PL3A	7	T		C3	PL3A	7	T	
B2	NC	-			B2	PL3B	7	C		B2	PL3B	7	C	
E5	NC	-			E5	PL4A	7	T		E5	PL4A	7	T	
F5	NC	-			F5	PL4B	7	C		F5	PL4B	7	C	
D3	NC	-			D3	PL5A	7	T		D3	PL5A	7	T	
C2	NC	-			C2	PL5B	7	C		C2	PL5B	7	C	
F4	NC	-			F4	PL6A	7	T	LDQS6	F4	PL6A	7	T	LDQS6
G4	NC	-			G4	PL6B	7	C		G4	PL6B	7	C	
E3	NC	-			E3	PL7A	7	T		E3	PL7A	7	T	
D2	NC	-			D2	PL7B	7	C		D2	PL7B	7	C	
B1	NC	-			B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL8A	7	T	LUM0_PLLT_IN_A
C1	NC	-			C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL8B	7	C	LUM0_PLLC_IN_A
F3	NC	-			F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL9A	7	T	LUM0_PLLT_FB_A
GND	-	-			GND	GND7	7			GND	GND7	7		
E2	NC	-			E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL9B	7	C	LUM0_PLLC_FB_A
G5	NC	-			G5	NC	-			G5	PL11A	7	T	
H6	NC	-			H6	NC	-			H6	PL11B	7	C	
G3	NC	-			G3	NC	-			G3	PL12A	7	T	
H4	NC	-			H4	NC	-			H4	PL12B	7	C	
J5	NC	-			J5	NC	-			J5	PL13A	7	T	
H5	NC	-			H5	NC	-			H5	PL13B	7	C	
F2	NC	-			F2	NC	-			F2	PL14A	7	T	
GND	-	-			GND	-	-			GND	GND7	7		
F1	NC	-			F1	NC	-			F1	PL14B	7	C	
E1	NC	-			E1	PL11A	7	T		E1	PL15A	7	T	
D1	NC	-			D1	PL11B	7	C		D1	PL15B	7	C	
H3	PL3A	7	T		H3	PL12A	7	T		H3	PL16A	7	T	
G2	PL3B	7	C		G2	PL12B	7	C		G2	PL16B	7	C	
H2	PL4A	7	T		H2	PL13A	7	T		H2	PL17A	7	T	
G1	PL4B	7	C		G1	PL13B	7	C		G1	PL17B	7	C	
J4	PL5A	7	T		J4	PL14A	7	T		J4	PL18A	7	T	
GND	-	-			GND	GND7	7			GND	GND7	7		
J3	PL5B	7	C		J3	PL14B	7	C		J3	PL18B	7	C	
J2	PL6A	7	T	LDQS6	J2	PL15A	7	T	LDQS15	J2	PL19A	7	T	LDQS19
H1	PL6B	7	C		H1	PL15B	7	C		H1	PL19B	7	C	
K4	PL7A	7	T		K4	PL16A	7	T		K4	PL20A	7	T	
K5	PL7B	7	C		K5	PL16B	7	C		K5	PL20B	7	C	
K3	PL8A	7	T		K3	PL17A	7	T		K3	PL21A	7	T	
K2	PL8B	7	C		K2	PL17B	7	C		K2	PL21B	7	C	
J1	PL9A	7	T	PCLKT7_0	J1	PL18A	7	T	PCLKT7_0	J1	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7			GND	GND7	7		
K1	PL9B	7	C	PCLKC7_0	K1	PL18B	7	C	PCLKC7_0	K1	PL22B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6			L3	XRES	6		
L4	PL11A	6	T		L4	PL20A	6	T		L4	PL24A	6	T	
L5	PL11B	6	C		L5	PL20B	6	C		L5	PL24B	6	C	
L2	PL12A	6	T		L2	PL21A	6	T		L2	PL25A	6	T	
L1	PL12B	6	C		L1	PL21B	6	C		L1	PL25B	6	C	

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
T11	VCCIO5	5			T11	VCCIO5	5			T11	VCCIO5	5		
M7	VCCIO6	6			M7	VCCIO6	6			M7	VCCIO6	6		
M8	VCCIO6	6			M8	VCCIO6	6			M8	VCCIO6	6		
N8	VCCIO6	6			N8	VCCIO6	6			N8	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6			P8	VCCIO6	6		
J8	VCCIO7	7			J8	VCCIO7	7			J8	VCCIO7	7		
K8	VCCIO7	7			K8	VCCIO7	7			K8	VCCIO7	7		
L7	VCCIO7	7			L7	VCCIO7	7			L7	VCCIO7	7		
L8	VCCIO7	7			L8	VCCIO7	7			L8	VCCIO7	7		
G15	VCCAUX	-			G15	VCCAUX	-			G15	VCCAUX	-		
G16	VCCAUX	-			G16	VCCAUX	-			G16	VCCAUX	-		
G7	VCCAUX	-			G7	VCCAUX	-			G7	VCCAUX	-		
G8	VCCAUX	-			G8	VCCAUX	-			G8	VCCAUX	-		
H16	VCCAUX	-			H16	VCCAUX	-			H16	VCCAUX	-		
H7	VCCAUX	-			H7	VCCAUX	-			H7	VCCAUX	-		
R16	VCCAUX	-			R16	VCCAUX	-			R16	VCCAUX	-		
R7	VCCAUX	-			R7	VCCAUX	-			R7	VCCAUX	-		
T15	VCCAUX	-			T15	VCCAUX	-			T15	VCCAUX	-		
T16	VCCAUX	-			T16	VCCAUX	-			T16	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-			T8	VCCAUX	-		
J6	VCC	-			J6	VCC	-			J6	VCC	-		
J17	VCC	-			J17	VCC	-			J17	VCC	-		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
P17	VCC	-			P17	VCC	-			P17	VCC	-		
A2	NC	-			A2	NC	-			A2	NC	-		
AB2	NC	-			AB2	NC	-			AB2	NC	-		
A21	NC	-			A21	NC	-			A21	NC	-		

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
P5	PL32B	6	C		P5	PL44B	6	C	
P6	PL33A	6	T		P6	PL45A	6	T	
R5	PL33B	6	C		R5	PL45B	6	C	
U1	PL34A	6	T		U1	PL46A	6	T	
U2	PL34B	6	C		U2	PL46B	6	C	
T3	PL35A	6	T		T3	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
T4	PL35B	6	C		T4	PL47B	6	C	
R6	PL36A	6	T	LDQS36	R6	PL48A	6	T	LDQS48
T5	PL36B	6	C		T5	PL48B	6	C	
T6	PL37A	6	T		T6	PL49A	6	T	
U5	PL37B	6	C		U5	PL49B	6	C	
U3	PL38A	6	T		U3	PL50A	6	T	
U4	PL38B	6	C		U4	PL50B	6	C	
V1	PL39A	6	T		V1	PL51A	6	T	
GND	GND6	6			GND	GND6	6		
V2	PL39B	6	C		V2	PL51B	6	C	
U7	TCK	6			U7	TCK	6		
V4	TDI	6			V4	TDI	6		
V5	TMS	6			V5	TMS	6		
V3	TDO	6			V3	TDO	6		
U6	VCCJ	6			U6	VCCJ	6		
W1	PL41A	6	T	LLM0_PLLT_IN_A	W1	PL53A	6	T	LLM0_PLLT_IN_A
W2	PL41B	6	C	LLM0_PLLC_IN_A	W2	PL53B	6	C	LLM0_PLLC_IN_A
V6	PL42A	6	T	LLM0_PLLT_FB_A	V6	PL54A	6	T	LLM0_PLLT_FB_A
W6	PL42B	6	C	LLM0_PLLC_FB_A	W6	PL54B	6	C	LLM0_PLLC_FB_A
Y1	PL43A	6	T		Y1	PL55A	6	T	
Y2	PL43B	6	C		Y2	PL55B	6	C	
W3	PL44A	6	T		W3	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W4	PL44B	6	C		W4	PL56B	6	C	
AA1	PL45A	6	T	LDQS45	AA1	PL57A	6	T	LDQS57
AB1	PL45B	6	C		AB1	PL57B	6	C	
Y4	PL46A	6	T		Y4	PL58A	6	T	
Y3	PL46B	6	C		Y3	PL58B	6	C	
AC1	PL47A	6	T		AC1	PL59A	6	T	
AB2	PL47B	6	C		AB2	PL59B	6	C	
AA2	NC	-			AA2	PL60A	6	T	
-	-	-			GND	GND6	6		
AA3	NC	-			AA3	PL60B	6	C	
W5	NC	-			W5	PL61A	6	T	
Y5	NC	-			Y5	PL61B	6	C	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AC13	PB32B	5	C	VREF1_5	AC13	PB32B	5	C	VREF1_5
AF14	PB33A	5	T	PCLKT5_0	AF14	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AE14	PB33B	5	C	PCLKC5_0	AE14	PB33B	5	C	PCLKC5_0
AA13	PB34A	4	T	WRITEN	AA13	PB34A	4	T	WRITEN
AB13	PB34B	4	C	CS1N	AB13	PB34B	4	C	CS1N
AD14	PB35A	4	T	VREF1_4	AD14	PB35A	4	T	VREF1_4
AA14	PB35B	4	C	CSN	AA14	PB35B	4	C	CSN
AC14	PB36A	4	T	VREF2_4	AC14	PB36A	4	T	VREF2_4
AB14	PB36B	4	C	D0/SPID7	AB14	PB36B	4	C	D0/SPID7
AF15	PB37A	4	T	D2/SPID5	AF15	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AE15	PB37B	4	C	D1/SPID6	AE15	PB37B	4	C	D1/SPID6
AD15	PB38A	4	T	BDQS38	AD15	PB38A	4	T	BDQS38
AC15	PB38B	4	C	D3/SPID4	AC15	PB38B	4	C	D3/SPID4
AF16	PB39A	4	T		AF16	PB39A	4	T	
Y14	PB39B	4	C	D4/SPID3	Y14	PB39B	4	C	D4/SPID3
AE16	PB40A	4	T		AE16	PB40A	4	T	
AB15	PB40B	4	C	D5/SPID2	AB15	PB40B	4	C	D5/SPID2
AF17	PB41A	4	T		AF17	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AE17	PB41B	4	C	D6/SPID1	AE17	PB41B	4	C	D6/SPID1
Y15	PB42A	4	T		Y15	PB42A	4	T	
AA15	PB42B	4	C		AA15	PB42B	4	C	
AD17	PB43A	4	T		AD17	PB43A	4	T	
Y16	PB43B	4	C		Y16	PB43B	4	C	
AD18	PB44A	4	T		AD18	PB44A	4	T	
AC16	PB44B	4	C		AC16	PB44B	4	C	
AE18	PB45A	4	T		AE18	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AF18	PB45B	4	C		AF18	PB45B	4	C	
AD16	PB46A	4	T	BDQS46	AD16	PB46A	4	T	BDQS46
AB16	PB46B	4	C		AB16	PB46B	4	C	
AF19	PB47A	4	T		AF19	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AA17	PB48A	4	T		AA17	PB48A	4	T	
Y17	PB48B	4	C		Y17	PB48B	4	C	
AF21	PB49A	4	T		AF21	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AF20	PB49B	4	C		AF20	PB49B	4	C	
AE21	PB50A	4	T		AE21	PB50A	4	T	
AC17	PB50B	4	C		AC17	PB50B	4	C	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
E24	NC	-			E24	PR8B	2	C	
D24	NC	-			D24	PR8A	2	T	
E22	NC	-			E22	PR7B	2	C	
F22	NC	-			F22	PR7A	2	T	
E21	NC	-			E21	PR6B	2	C	
D22	NC	-			D22	PR6A	2	T	RDQS6
E23	PR2B	2	C	VREF1_2	E23	PR2B	2	C	VREF1_2
D23	PR2A	2	T	VREF2_2	D23	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
G20	NC	-			G20	PT65B	1	C	
F20	NC	-			F20	PT65A	1	T	
D21	NC	-			D21	PT64B	1	C	
C21	NC	-			C21	PT64A	1	T	
C23	NC	-			C23	PT63B	1	C	
C22	NC	-			C22	PT63A	1	T	
B23	NC	-			B23	PT62B	1	C	
C24	NC	-			C24	PT62A	1	T	TDQS62
D20	NC	-			D20	PT61B	1	C	
-	-	-			GND	GND1	1		
E19	NC	-			E19	PT61A	1	T	
B25	NC	-			B25	PT60B	1	C	
B24	NC	-			B24	PT60A	1	T	
B26	NC	-			B26	PT59B	1	C	
A25	NC	-			A25	PT59A	1	T	
C20	NC	-			C20	PT58B	1	C	
C19	NC	-			C19	PT58A	1	T	
A24	PT57B	1	C		A24	PT57B	1	C	
-	-	-			GND	GND1	1		
A23	PT57A	1	T		A23	PT57A	1	T	
E18	PT56B	1	C		E18	PT56B	1	C	
D19	PT56A	1	T		D19	PT56A	1	T	
F19	PT55B	1	C		F19	PT55B	1	C	
B22	PT55A	1	T		B22	PT55A	1	T	
G19	PT54B	1	C		G19	PT54B	1	C	
B21	PT54A	1	T	TDQS54	B21	PT54A	1	T	TDQS54
D18	PT53B	1	C		D18	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
C18	PT53A	1	T		C18	PT53A	1	T	
F18	PT52B	1	C		F18	PT52B	1	C	
A22	PT52A	1	T		A22	PT52A	1	T	
G18	PT51B	1	C		G18	PT51B	1	C	