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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	147
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec6e-5qn208c

Figure 2-8. Per Quadrant Primary Clock Selection

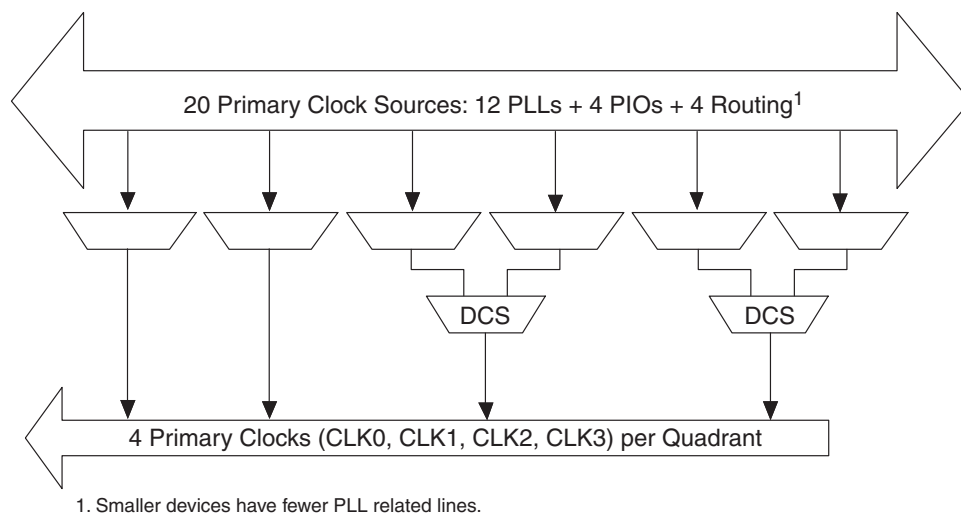


Figure 2-9. Per Quadrant Secondary Clock Selection

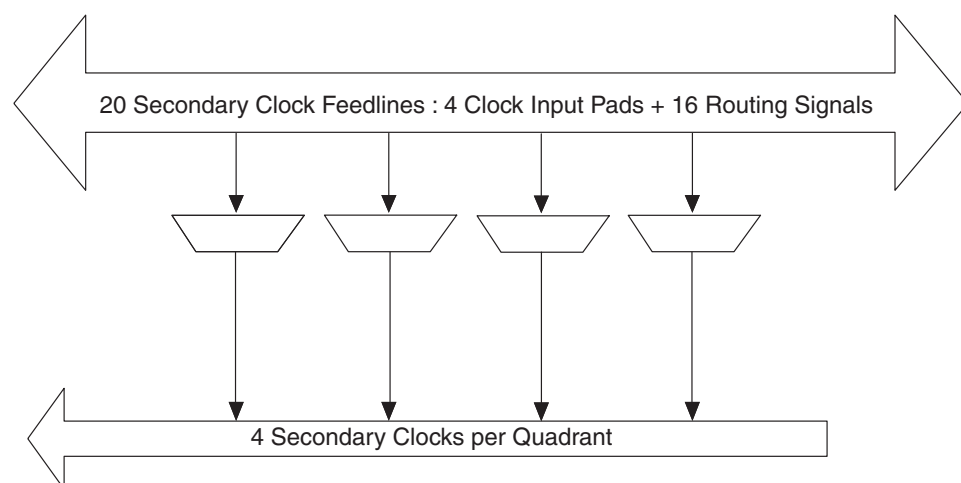
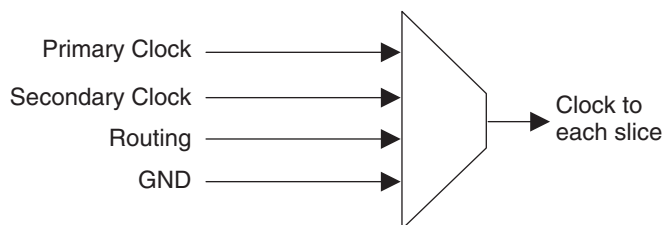


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

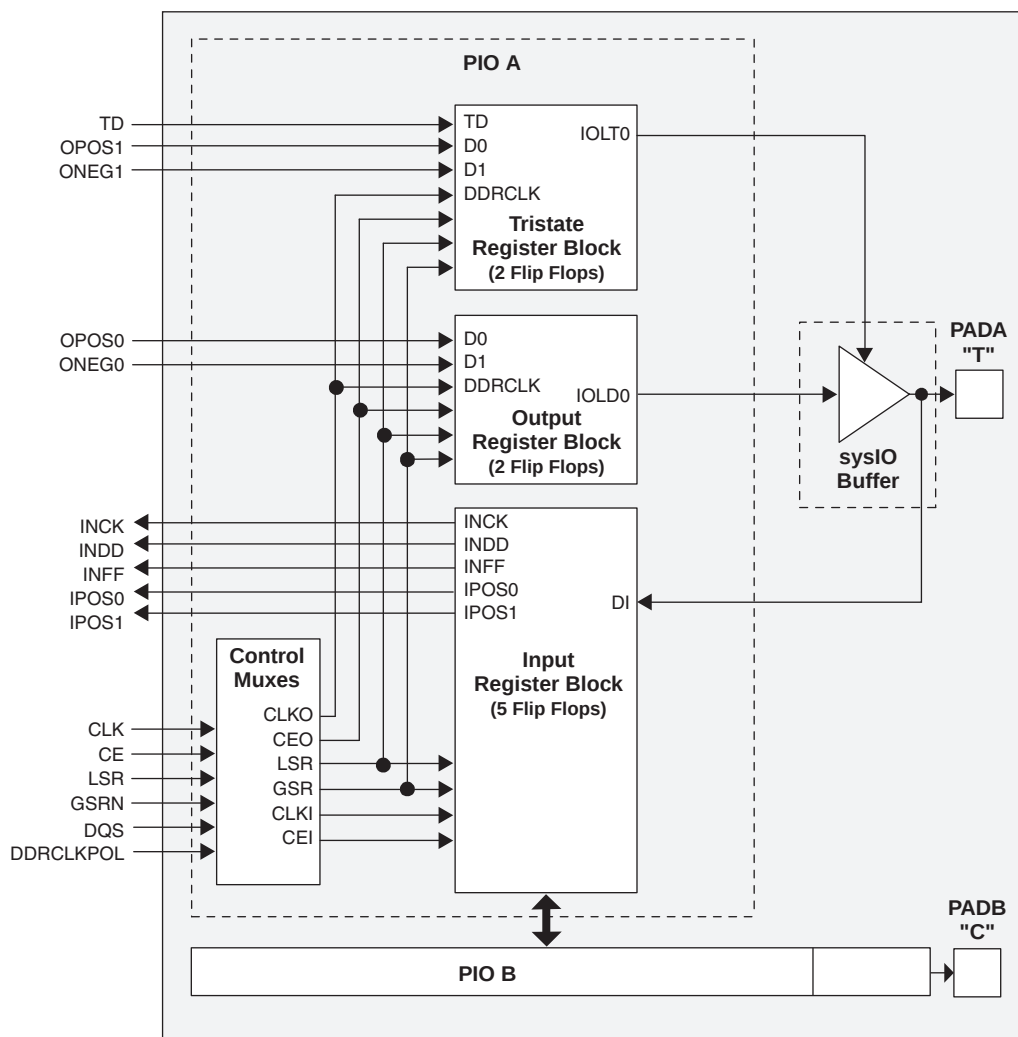
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Figure 2-27. Input Register DDR Waveforms

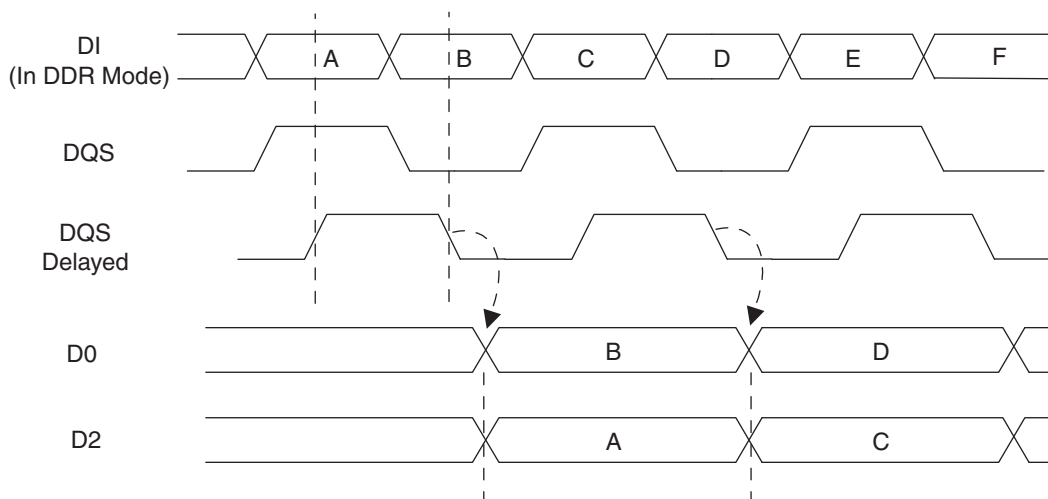
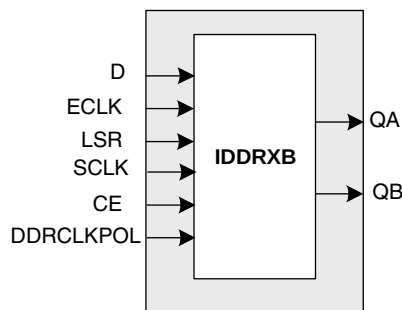


Figure 2-28. INDDRxB Primitive



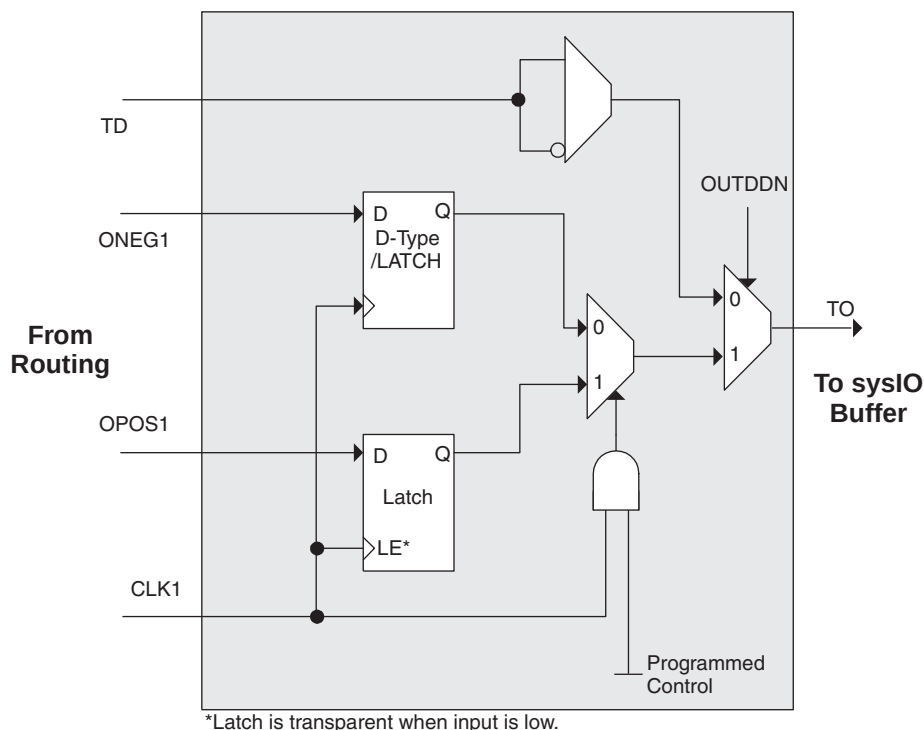
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sys/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-31. Tristate Register Block



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Initialization Supply Current^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Symbol	Parameter	Devices	Typ. ⁶	Units
I _{CC}	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFEC6/LFEC6	50	mA
		LFEC10/LFEC10	60	mA
		LFEC15/LFEC15	70	mA
		LFEC20/LFEC20	150	mA
		LFEC33/LFEC33	220	mA
I _{CCAUX}	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFEC6/LFEC6	30	mA
		LFEC10/LFEC10	35	mA
		LFEC15/LFEC15	35	mA
		LFEC20/LFEC20	40	mA
		LFEC33/LFEC33	40	mA
I _{CCPLL}	PLL Power Supply Current		12	mA
I _{CCIO}	Bank Power Supply Current ⁷	LFEC1	4	mA
		LFEC3	5	mA
		LFEC6/LFEC6	6	mA
		LFEC10/LFEC10	6	mA
		LFEC15/LFEC15	7	mA
		LFEC20/LFEC20	8	mA
		LFEC33/LFEC33	8	mA
I _{CCJ}	V _{CCJ} Power Supply Current		20	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.

6. T_J=25°C, power supplies at nominal voltage.

7. Per bank.

sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.465	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL ¹	3.135	3.3	3.465	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
RSDS ¹	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

LFEC6P/EC6, LFEC6P/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC6P/EC6				LFEC6P/EC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	VCCAUX	-			VCCAUX	-		
137	PR9B	2	C	PCLKC2_0	PR18B	2	C	PCLKC2_0
138	GND2	2			GND2	2		
139	PR9A	2	T	PCLKT2_0	PR18A	2	T	PCLKT2_0
140	PR8B	2	C		PR17B	2	C	
141	PR8A	2	T		PR17A	2	T	
142	PR7B	2	C		PR16B	2	C	
143	PR7A	2	T		PR16A	2	T	
144	PR6B	2	C		PR15B	2	C	
145	VCCIO2	2			VCCIO2	2		
146	PR6A	2	T	RDQS6	PR15A	2	T	RDQS15
147	PR5B	2	C		PR14B	2	C	
148	PR5A	2	T		PR14A	2	T	
149	PR4B	2	C		PR13B	2	C	
150	PR4A	2	T		PR13A	2	T	
151	NC	-			GND	-		
152	NC	-			VCC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	PT33A	1			PT41A	1		
159	PT25B	1	C		PT33B	1	C	
160	PT25A	1	T		PT33A	1	T	
161	PT24B	1	C		PT32B	1	C	
162	PT24A	1	T		PT32A	1	T	
163	PT23B	1	C		PT31B	1	C	
164	PT23A	1	T		PT31A	1	T	
165	PT22B	1	C		PT30B	1	C	
166	PT22A	1	T	TDQS22	PT30A	1	T	TDQS30
167	PT21B	1	C		PT29B	1	C	
168	GND1	1			GND1	1		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFEC/EC10 and LFEC/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFEC/EC10				LFEC/EC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFEC/EC10 and LFEC/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC/EC10				LFEC/EC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G12	PR18A	2	T	PCLKT2_0	PR22A	2	T	PCLKT2_0
G13	PR17B	2	C		PR21B	2	C	
F13	PR17A	2	T		PR21A	2	T	
F12	PR16B	2	C		PR20B	2	C	
E13	PR16A	2	T		PR20A	2	T	
D16	PR15B	2	C		PR19B	2	C	
D15	PR15A	2	T		PR19A	2	T	RDQS19
F14	PR14B	2	C		PR18B	2	C	
GND	GND2	2			GND2	2		
E14	PR14A	2	T		PR18A	2	T	
C16	PR13B	2	C		PR17B	2	C	
B16	PR13A	2	T		PR17A	2	T	
C15	PR12B	2	C		PR16B	2	C	
C14	PR12A	2	T		PR16A	2	T	
GND	GND2	2			GND2	2		
-	-	-			GND2	2		
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
-	-	-			GND1	1		
B13	PT34B	1	C		PT34B	1	C	
C13	PT34A	1	T		PT34A	1	T	
C12	PT33B	1	C		PT33B	1	C	
GND	GND1	1			GND1	1		
D12	PT33A	1	T		PT33A	1	T	
A15	PT32B	1	C		PT32B	1	C	
B14	PT32A	1	T		PT32A	1	T	
D11	PT31B	1	C		PT31B	1	C	
C11	PT31A	1	T		PT31A	1	T	
E10	PT30B	1	C		PT30B	1	C	
E11	PT30A	1	T	TDQS30	PT30A	1	T	TDQS30
A14	PT29B	1	C		PT29B	1	C	
GND	GND1	1			GND1	1		
A13	PT29A	1	T		PT29A	1	T	
D10	PT28B	1	C		PT28B	1	C	
C10	PT28A	1	T		PT28A	1	T	
A12	PT27B	1	C	VREF2_1	PT27B	1	C	VREF2_1
B12	PT27A	1	T	VREF1_1	PT27A	1	T	VREF1_1
A11	PT26B	1	C		PT26B	1	C	
B11	PT26A	1	T		PT26A	1	T	

LFEC/EC10 and LFEC/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC/EC10				LFEC/EC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
A10	PT25B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT25A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
C9	PT24B	0	C	VREF1_0	PT24B	0	C	VREF1_0
B9	PT24A	0	T	VREF2_0	PT24A	0	T	VREF2_0
E9	PT23B	0	C		PT23B	0	C	
D9	PT23A	0	T		PT23A	0	T	
D8	PT22B	0	C		PT22B	0	C	
C8	PT22A	0	T	TDQS22	PT22A	0	T	TDQS22
A9	PT21B	0	C		PT21B	0	C	
GND	GND0	0			GND0	0		
A8	PT21A	0	T		PT21A	0	T	
B8	PT20B	0	C		PT20B	0	C	
B7	PT20A	0	T		PT20A	0	T	
D7	PT19B	0	C		PT19B	0	C	
C7	PT19A	0	T		PT19A	0	T	
A7	PT18B	0	C		PT18B	0	C	
A6	PT18A	0	T		PT18A	0	T	
E7	PT17B	0	C		PT17B	0	C	
GND	GND0	0			GND0	0		
E6	PT17A	0	T		PT17A	0	T	
D6	PT16B	0	C		PT16B	0	C	
C6	PT16A	0	T		PT16A	0	T	
B6	PT15B	0	C		PT15B	0	C	
B5	PT15A	0	T		PT15A	0	T	
A5	PT14B	0	C		PT14B	0	C	
A4	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A3	PT13B	0	C		PT13B	0	C	
-	GND0	0			GND0	0		
A2	PT13A	0	T		PT13A	0	T	
B2	PT12B	0	C		PT12B	0	C	
B3	PT12A	0	T		PT12A	0	T	
D5	PT11B	0	C		PT11B	0	C	
C5	PT11A	0	T		PT11A	0	T	
C4	PT10B	0	C		PT10B	0	C	
B4	PT10A	0	T		PT10A	0	T	
GND	GND0	0			GND0	0		
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLT_FB_A	C22	PR9A	2	T	RUM0_PLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLT_IN_A	G18	PR8A	2	T	RUM0_PLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
F14	PT23B	1	C		F14	PT31B	1	C		F14	PT31B	1	C	
D14	PT23A	1	T		D14	PT31A	1	T		D14	PT31A	1	T	
E13	PT22B	1	C		E13	PT30B	1	C		E13	PT30B	1	C	
G13	PT22A	1	T	TDQS22	G13	PT30A	1	T	TDQS30	G13	PT30A	1	T	TDQS30
A12	PT21B	1	C		A12	PT29B	1	C		A12	PT29B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B12	PT21A	1	T		B12	PT29A	1	T		B12	PT29A	1	T	
F13	PT20B	1	C		F13	PT28B	1	C		F13	PT28B	1	C	
D13	PT20A	1	T		D13	PT28A	1	T		D13	PT28A	1	T	
F12	PT19B	1	C	VREF2_1	F12	PT27B	1	C	VREF2_1	F12	PT27B	1	C	VREF2_1
D12	PT19A	1	T	VREF1_1	D12	PT27A	1	T	VREF1_1	D12	PT27A	1	T	VREF1_1
F11	PT18B	1	C		F11	PT26B	1	C		F11	PT26B	1	C	
C12	PT18A	1	T		C12	PT26A	1	T		C12	PT26A	1	T	
A11	PT17B	0	C	PCLKC0_0	A11	PT25B	0	C	PCLKC0_0	A11	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0			GND	GND0	0		
A10	PT17A	0	T	PCLKT0_0	A10	PT25A	0	T	PCLKT0_0	A10	PT25A	0	T	PCLKT0_0
E12	PT16B	0	C	VREF1_0	E12	PT24B	0	C	VREF1_0	E12	PT24B	0	C	VREF1_0
E11	PT16A	0	T	VREF2_0	E11	PT24A	0	T	VREF2_0	E11	PT24A	0	T	VREF2_0
B11	PT15B	0	C		B11	PT23B	0	C		B11	PT23B	0	C	
C11	PT15A	0	T		C11	PT23A	0	T		C11	PT23A	0	T	
B9	PT14B	0	C		B9	PT22B	0	C		B9	PT22B	0	C	
B10	PT14A	0	T	TDQS14	B10	PT22A	0	T	TDQS22	B10	PT22A	0	T	TDQS22
A9	PT13B	0	C		A9	PT21B	0	C		A9	PT21B	0	C	
GND	GND0	0			GND	GND0	0			GND	GND0	0		
A8	PT13A	0	T		A8	PT21A	0	T		A8	PT21A	0	T	
D11	PT12B	0	C		D11	PT20B	0	C		D11	PT20B	0	C	
C10	PT12A	0	T		C10	PT20A	0	T		C10	PT20A	0	T	
A7	PT11B	0	C		A7	PT19B	0	C		A7	PT19B	0	C	
A6	PT11A	0	T		A6	PT19A	0	T		A6	PT19A	0	T	
B7	PT10B	0	C		B7	PT18B	0	C		B7	PT18B	0	C	
B8	PT10A	0	T		B8	PT18A	0	T		B8	PT18A	0	T	
A5	PT9B	0	C		A5	PT17B	0	C		A5	PT17B	0	C	
GND	GND0	0			GND	GND0	0			GND	GND0	0		
B6	PT9A	0	T		B6	PT17A	0	T		B6	PT17A	0	T	
G10	PT8B	0	C		G10	PT16B	0	C		G10	PT16B	0	C	
E10	PT8A	0	T		E10	PT16A	0	T		E10	PT16A	0	T	
F10	PT7B	0	C		F10	PT15B	0	C		F10	PT15B	0	C	
D10	PT7A	0	T		D10	PT15A	0	T		D10	PT15A	0	T	
G9	PT6B	0	C		G9	PT14B	0	C		G9	PT14B	0	C	
E9	PT6A	0	T	TDQS6	E9	PT14A	0	T	TDQS14	E9	PT14A	0	T	TDQS14
C9	PT5B	0	C		C9	PT13B	0	C		C9	PT13B	0	C	
GND	-	-			GND	GND0	0			GND	GND0	0		
C8	PT5A	0	T		C8	PT13A	0	T		C8	PT13A	0	T	
F9	PT4B	0	C		F9	PT12B	0	C		F9	PT12B	0	C	
D9	PT4A	0	T		D9	PT12A	0	T		D9	PT12A	0	T	
F8	PT3B	0	C		F8	PT11B	0	C		F8	PT11B	0	C	
D7	PT3A	0	T		D7	PT11A	0	T		D7	PT11A	0	T	
D8	PT2B	0	C		D8	PT10B	0	C		D8	PT10B	0	C	
C7	PT2A	0	T		C7	PT10A	0	T		C7	PT10A	0	T	
GND	GND0	0			GND	GND0	0			GND	GND0	0		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
GND	-	-			GND	GND7	7		
C3	PL3A	7	T		C3	PL10A	7	T	
B2	PL3B	7	C		B2	PL10B	7	C	
E5	PL4A	7	T		E5	PL11A	7	T	
F5	PL4B	7	C		F5	PL11B	7	C	
D3	PL5A	7	T		D3	PL12A	7	T	
C2	PL5B	7	C		C2	PL12B	7	C	
GND	-	-			GND	GND7	7		
F4	PL6A	7	T	LDQS6	F4	PL14A	7	T	LDQS14
G4	PL6B	7	C		G4	PL14B	7	C	
E3	PL7A	7	T		E3	PL15A	7	T	
D2	PL7B	7	C		D2	PL15B	7	C	
B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL16A	7	T	LUM0_PLLT_IN_A
C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL16B	7	C	LUM0_PLLC_IN_A
F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL17B	7	C	LUM0_PLLC_FB_A
GND	-	-			GND	GND7	7		
G5	PL11A	7	T		G5	PL23A	7	T	LDQS23
H6	PL11B	7	C		H6	PL23B	7	C	
G3	PL12A	7	T		G3	PL24A	7	T	
H4	PL12B	7	C		H4	PL24B	7	C	
J5	PL13A	7	T		J5	PL25A	7	T	
H5	PL13B	7	C		H5	PL25B	7	C	
F2	PL14A	7	T		F2	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
F1	PL14B	7	C		F1	PL26B	7	C	
E1	PL15A	7	T		E1	PL27A	7	T	
D1	PL15B	7	C		D1	PL27B	7	C	
H3	PL16A	7	T		H3	PL28A	7	T	
G2	PL16B	7	C		G2	PL28B	7	C	
H2	PL17A	7	T		H2	PL29A	7	T	
G1	PL17B	7	C		G1	PL29B	7	C	
J4	PL18A	7	T		J4	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
J3	PL18B	7	C		J3	PL30B	7	C	
J2	PL19A	7	T	LDQS19	J2	PL31A	7	T	LDQS31
H1	PL19B	7	C		H1	PL31B	7	C	
K4	PL20A	7	T		K4	PL32A	7	T	
K5	PL20B	7	C		K5	PL32B	7	C	

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A21	PT51A	1	T		A21	PT51A	1	T	
E17	PT50B	1	C		E17	PT50B	1	C	
B17	PT50A	1	T		B17	PT50A	1	T	
C17	PT49B	1	C		C17	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
D17	PT49A	1	T		D17	PT49A	1	T	
F17	PT48B	1	C		F17	PT48B	1	C	
E20	PT48A	1	T		E20	PT48A	1	T	
G17	PT47B	1	C		G17	PT47B	1	C	
B20	PT47A	1	T		B20	PT47A	1	T	
E16	PT46B	1	C		E16	PT46B	1	C	
A20	PT46A	1	T	TDQS46	A20	PT46A	1	T	TDQS46
A19	PT45B	1	C		A19	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
B19	PT45A	1	T		B19	PT45A	1	T	
D16	PT44B	1	C		D16	PT44B	1	C	
C16	PT44A	1	T		C16	PT44A	1	T	
F16	PT43B	1	C		F16	PT43B	1	C	
A18	PT43A	1	T		A18	PT43A	1	T	
G16	PT42B	1	C		G16	PT42B	1	C	
B18	PT42A	1	T		B18	PT42A	1	T	
A17	PT41B	1	C		A17	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
A16	PT41A	1	T		A16	PT41A	1	T	
D15	PT40B	1	C		D15	PT40B	1	C	
B16	PT40A	1	T		B16	PT40A	1	T	
E15	PT39B	1	C		E15	PT39B	1	C	
C15	PT39A	1	T		C15	PT39A	1	T	
F15	PT38B	1	C		F15	PT38B	1	C	
G15	PT38A	1	T	TDQS38	G15	PT38A	1	T	TDQS38
B15	PT37B	1	C		B15	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
A15	PT37A	1	T		A15	PT37A	1	T	
E14	PT36B	1	C		E14	PT36B	1	C	
G14	PT36A	1	T		G14	PT36A	1	T	
D14	PT35B	1	C	VREF2_1	D14	PT35B	1	C	VREF2_1
E13	PT35A	1	T	VREF1_1	E13	PT35A	1	T	VREF1_1
F14	PT34B	1	C		F14	PT34B	1	C	
C14	PT34A	1	T		C14	PT34A	1	T	
B14	PT33B	0	C	PCLKC0_0	B14	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A14	PT33A	0	T	PCLKT0_0	A14	PT33A	0	T	PCLKT0_0

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
J14	VCCIO1	1			J14	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
J16	VCCIO1	1			J16	VCCIO1	1		
J17	VCCIO1	1			J17	VCCIO1	1		
K17	VCCIO2	2			K17	VCCIO2	2		
K18	VCCIO2	2			K18	VCCIO2	2		
L18	VCCIO2	2			L18	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
N18	VCCIO2	2			N18	VCCIO2	2		
N19	VCCIO2	2			N19	VCCIO2	2		
P18	VCCIO3	3			P18	VCCIO3	3		
P19	VCCIO3	3			P19	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
R19	VCCIO3	3			R19	VCCIO3	3		
T18	VCCIO3	3			T18	VCCIO3	3		
U18	VCCIO3	3			U18	VCCIO3	3		
V14	VCCIO4	4			V14	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
V16	VCCIO4	4			V16	VCCIO4	4		
V17	VCCIO4	4			V17	VCCIO4	4		
W14	VCCIO4	4			W14	VCCIO4	4		
W15	VCCIO4	4			W15	VCCIO4	4		
V10	VCCIO5	5			V10	VCCIO5	5		
V11	VCCIO5	5			V11	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
V13	VCCIO5	5			V13	VCCIO5	5		
W12	VCCIO5	5			W12	VCCIO5	5		
W13	VCCIO5	5			W13	VCCIO5	5		
P8	VCCIO6	6			P8	VCCIO6	6		
P9	VCCIO6	6			P9	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T9	VCCIO6	6			T9	VCCIO6	6		
U9	VCCIO6	6			U9	VCCIO6	6		
K9	VCCIO7	7			K9	VCCIO7	7		
L9	VCCIO7	7			L9	VCCIO7	7		
M8	VCCIO7	7			M8	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
N8	VCCIO7	7			N8	VCCIO7	7		
N9	VCCIO7	7			N9	VCCIO7	7		
G13	VCCAUX	-			G13	VCCAUX	-		
H20	VCCAUX	-			H20	VCCAUX	-		