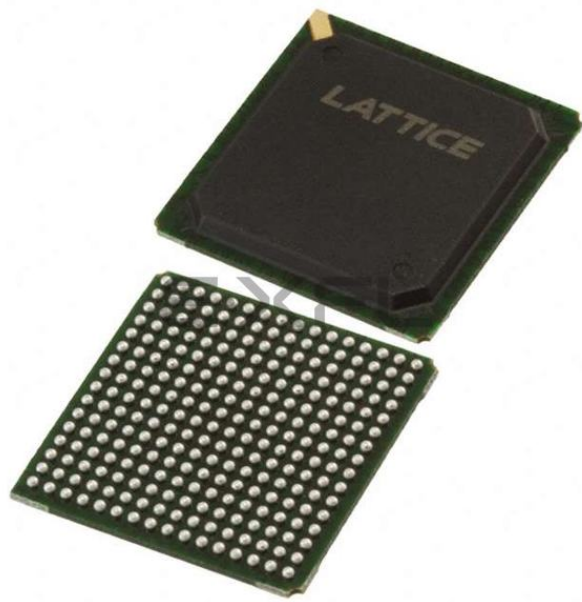




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

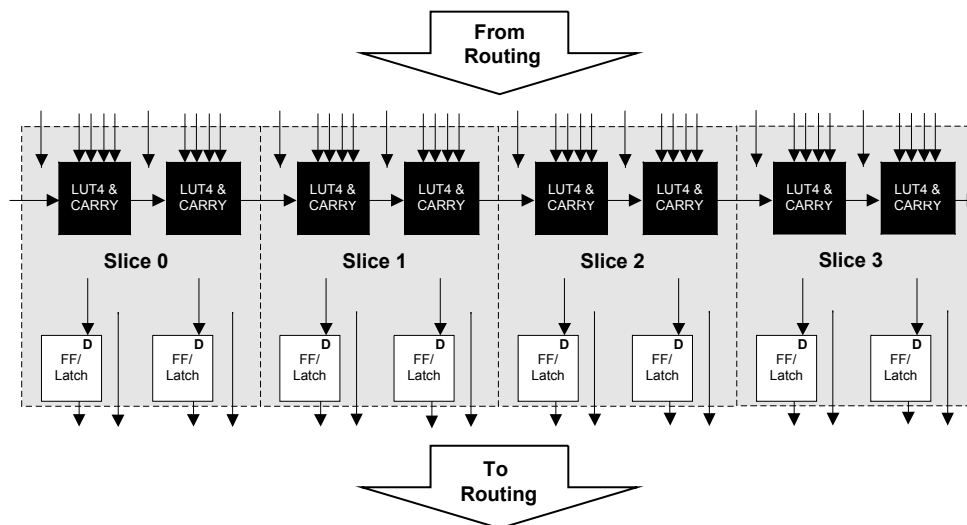
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp10e-3fn256c

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

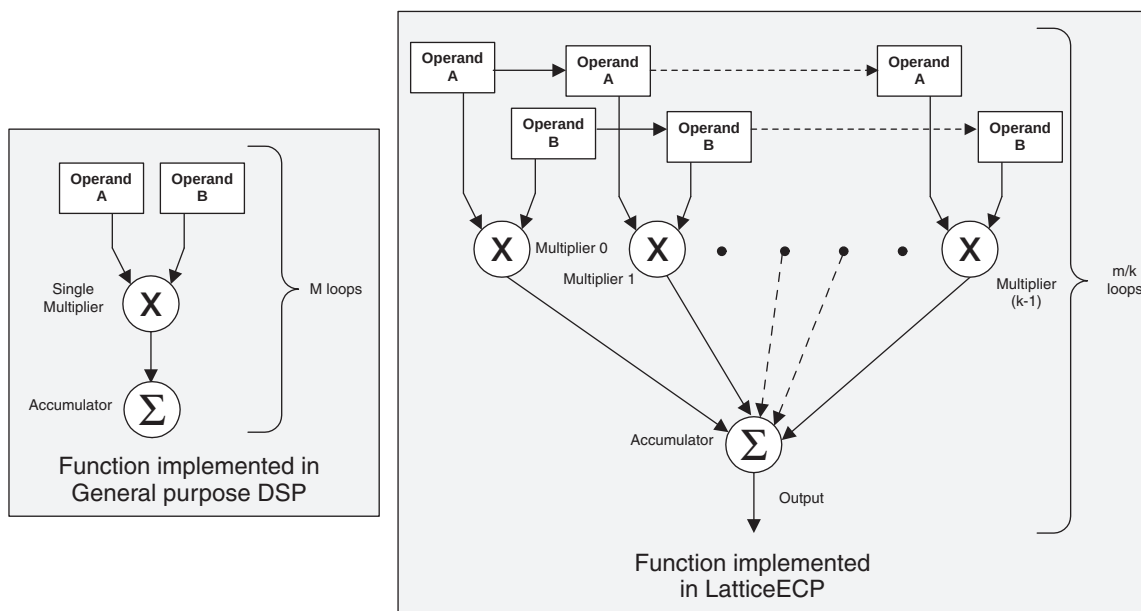
There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-18 compares the serial and the parallel implementations.

Figure 2-18. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

Figure 2-27. Input Register DDR Waveforms

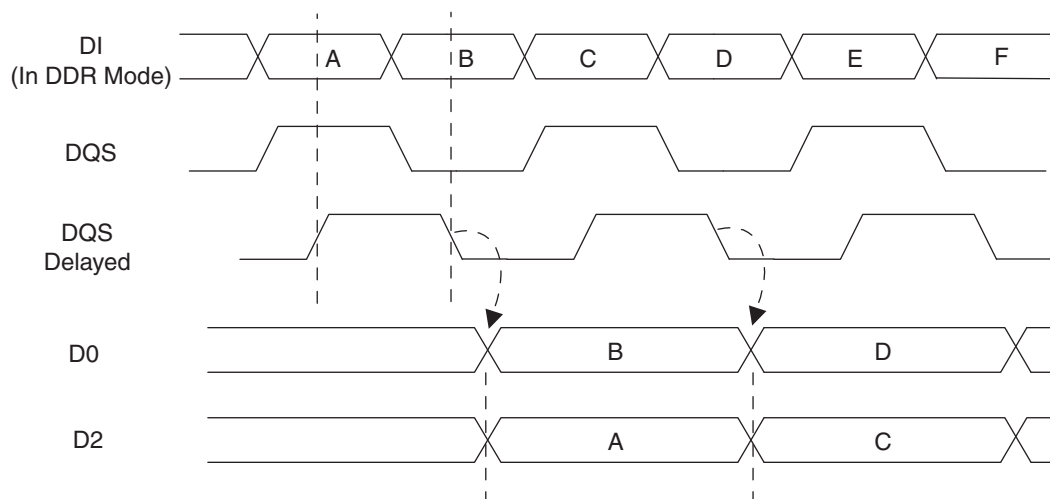
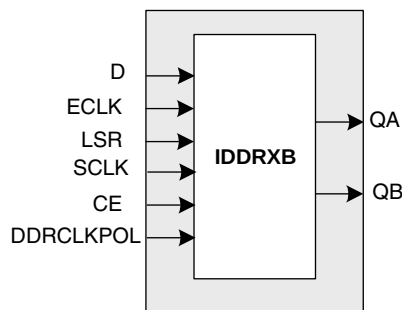


Figure 2-28. INDDRxB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sys/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.465	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL ¹	3.135	3.3	3.465	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
RSDS ¹	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold		+/-100	—	—	mV
V_{CM}	Input common mode voltage	100mV δV_{THD}	$V_{THD}/2$	1.2	1.8	V
		200mV δV_{THD}	$V_{THD}/2$	1.2	1.9	V
		350mV δV_{THD}	$V_{THD}/2$	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	μA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	0.9V	1.03	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100 \text{ Ohm}$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} + V_{OM})/2, R_T = 100 \text{ Ohm}$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0V$ Driver outputs shorted	—	—	6	mA

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

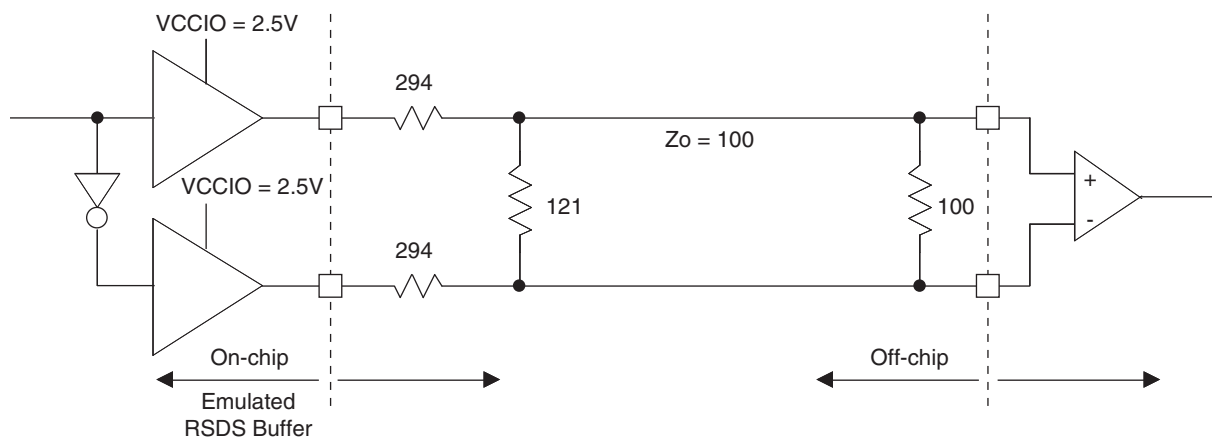


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	ohm
R _S	Driver series resistor	294	ohm
R _P	Driver parallel resistor	121	ohm
R _T	Receiver termination	100	ohm
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	101.5	ohm
I _{DC}	DC output current	3.66	mA

LatticeECP/EC External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	200	95	166	95	133	MHz
Primary and Secondary Clock⁶									
$f_{MAX_PRI}^2$	Frequency for Primary Clock Tree	All	—	420	—	378	—	340	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	All	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA. Loading of 0 pF.

2. Using LVDS I/O standard.

3. DDR timing numbers based on SSTL I/O.

4. DDR specifications are characterized but not tested.

5. UI is average bit period.

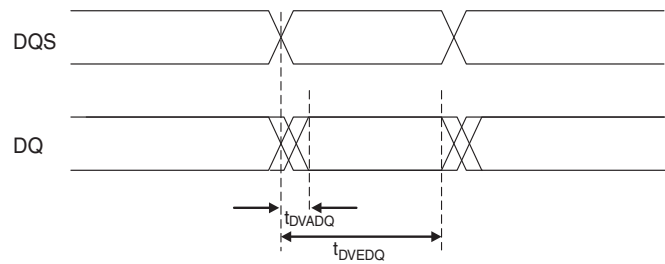
6. Based on a single primary clock.

7. These timing numbers were generated using ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

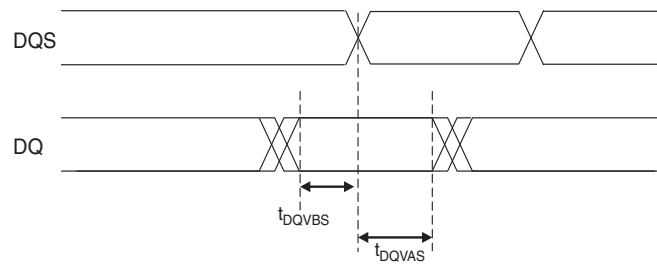
Timing v.G 0.30

Figure 3-5. DDR Timings

DQ and DQS Read Timings



DQ and DQS Write Timings



LatticeECP/EC Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUC_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.14	—	-0.17	—	-0.20	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t_{SUI_DSP}	Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HI_DSP}	Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.31	—	3.98	—	4.64	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{SUO_DSP}^4$	Output Register Setup Time	5.54	—	6.64	—	7.75	—	ns
$t_{HO_DSP}^4$	Output Register Hold Time	0.71	—	0.86	—	1.00	—	ns
$t_{COI_DSP}^4$	Input Register Clock to Output Time	—	7.50	—	9.00	—	10.50	ns
$t_{COP_DSP}^4$	Pipeline Register Clock to Output Time	—	4.66	—	5.60	—	6.53	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	1.47	—	1.77	—	2.06	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

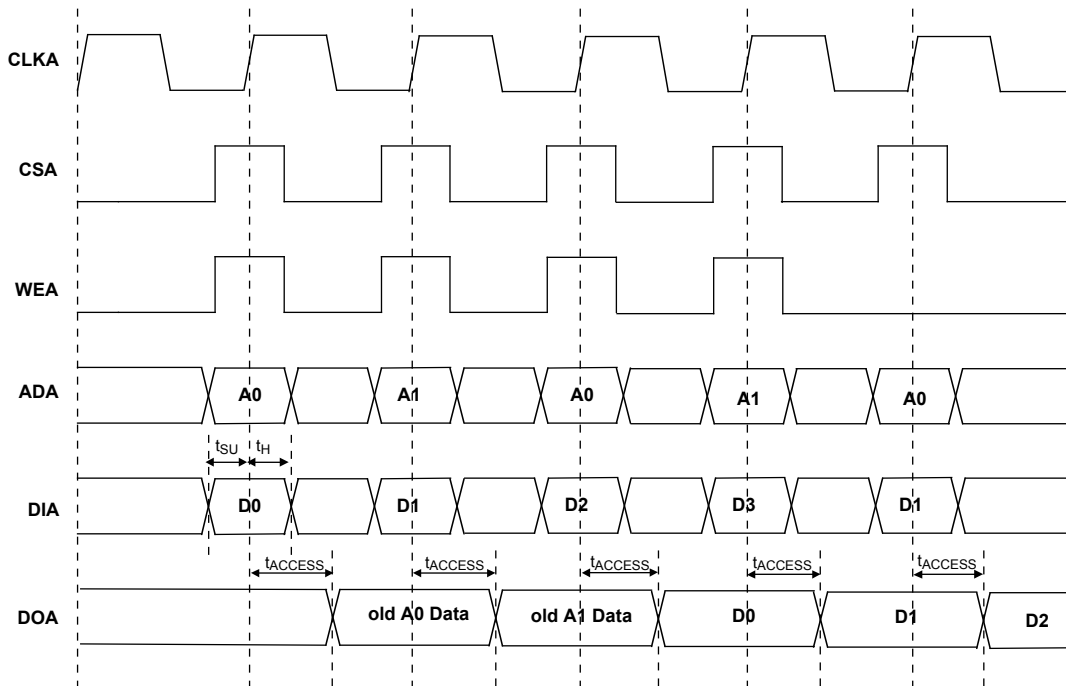
2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.

4. These parameters include the Adder Subtractor block in the path.

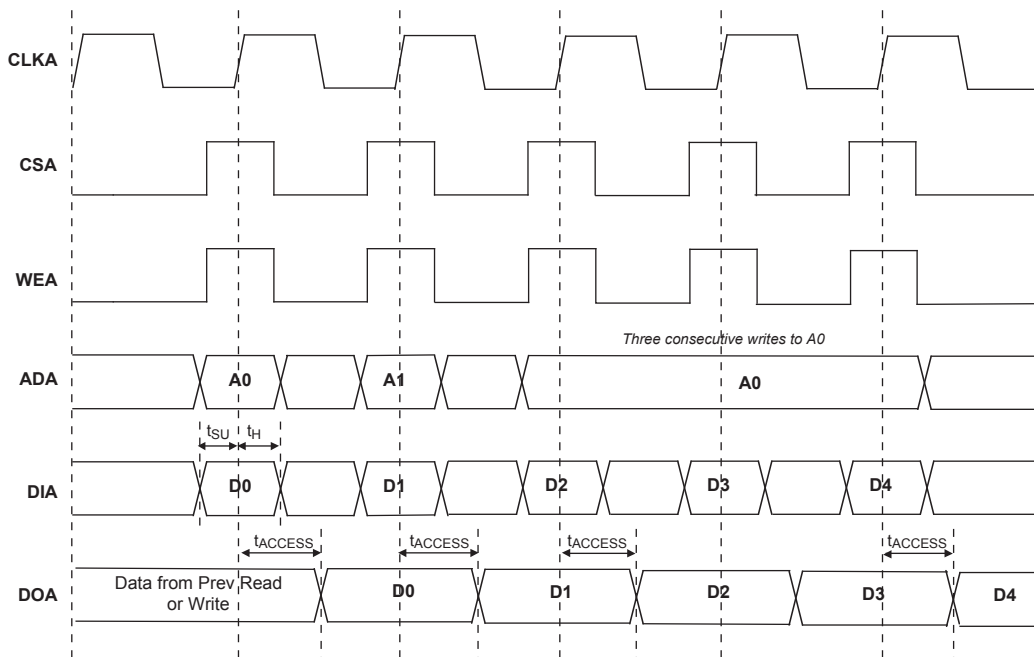
Timing v.G 0.30

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)

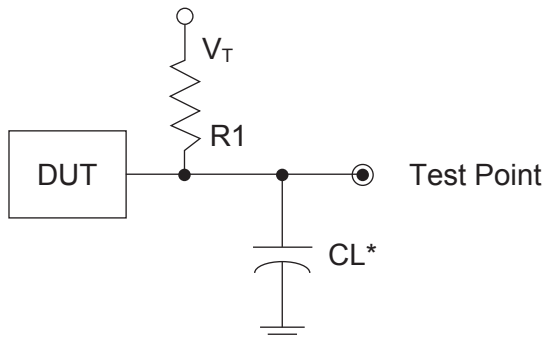


Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Switching Test Conditions

Figure 3-21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-21. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188 $\frac{3}{4}$	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			$V_{OH} - 0.15$	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			$V_{OL} + 0.15$	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ

Notes:

1. "n" is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

LFEC6P/EC6, LFEC6P/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC6P/EC6				LFEC6P/EC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
43	PL24A	6	T	LDQS24	PL33A	6	T	LDQS33
44	PL24B	6	C		PL33B	6	C	
45	PL25A	6	T		PL34A	6	T	
46	PL25B	6	C		PL34B	6	C	
47	PL26A	6	T		PL35A	6	T	
48	PL26B	6	C		PL35B	6	C	
49	PL27A	6	T	VREF1_6	PL36A	6	T	VREF1_6
50	PL27B	6	C	VREF2_6	PL36B	6	C	VREF2_6
51	VCCIO6	6			VCCIO6	6		
52*	GND5 GND6	-			GND5 GND6	-		
53	VCCIO5	5			VCCIO5	5		
54	PB2A	5	T		PB2A	5	T	
55	PB2B	5	C		PB2B	5	C	
56	PB3A	5	T		PB3A	5	T	
57	PB3B	5	C		PB3B	5	C	
58	PB4A	5	T		PB4A	5	T	
59	PB4B	5	C		PB4B	5	C	
60	PB5A	5	T		PB5A	5	T	
61	PB5B	5	C		PB5B	5	C	
62	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
63	PB6B	5	C		PB6B	5	C	
64	VCCIO5	5			VCCIO5	5		
65	PB10A	5	T		PB18A	5	T	
66	PB10B	5	C		PB18B	5	C	
67	PB11A	5	T		PB19A	5	T	
68	PB11B	5	C		PB19B	5	C	
69	PB12A	5	T		PB20A	5	T	
70	PB12B	5	C		PB20B	5	C	
71	PB13A	5	T		PB21A	5	T	
72	GND5	5			GND5	5		
73	PB13B	5	C		PB21B	5	C	
74	VCCIO5	5			VCCIO5	5		
75	PB14A	5	T	BDQS14	PB22A	5	T	BDQS22
76	PB14B	5	C		PB22B	5	C	
77	PB15A	5	T		PB23A	5	T	
78	PB15B	5	C		PB23B	5	C	
79	PB16A	5	T	VREF2_5	PB24A	5	T	VREF2_5
80	PB16B	5	C	VREF1_5	PB24B	5	C	VREF1_5
81	PB17A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
82	GND5	5			GND5	5		
83	PB17B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
84	VCCAUX	-			VCCAUX	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N7	PB18B	5	C		PB18B	5	C	
R7	PB19A	5	T		PB19A	5	T	
R8	PB19B	5	C		PB19B	5	C	
M7	PB20A	5	T		PB20A	5	T	
M8	PB20B	5	C		PB20B	5	C	
T8	PB21A	5	T		PB21A	5	T	
GND	GND5	5			GND5	5		
T9	PB21B	5	C		PB21B	5	C	
P8	PB22A	5	T	BDQS22	PB22A	5	T	BDQS22
N8	PB22B	5	C		PB22B	5	C	
R9	PB23A	5	T		PB23A	5	T	
R10	PB23B	5	C		PB23B	5	C	
P9	PB24A	5	T	VREF2_5	PB24A	5	T	VREF2_5
N9	PB24B	5	C	VREF1_5	PB24B	5	C	VREF1_5
T10	PB25A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB25B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
T12	PB26A	4	T	WRITEN	PB26A	4	T	WRITEN
T13	PB26B	4	C	CS1N	PB26B	4	C	CS1N
P10	PB27A	4	T	VREF1_4	PB27A	4	T	VREF1_4
N10	PB27B	4	C	CSN	PB27B	4	C	CSN
T14	PB28A	4	T	VREF2_4	PB28A	4	T	VREF2_4
T15	PB28B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
M10	PB29A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB29B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
R11	PB30A	4	T	BDQS30	PB30A	4	T	BDQS30
P11	PB30B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
R13	PB31A	4	T		PB31A	4	T	
R14	PB31B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
P12	PB32A	4	T		PB32A	4	T	
P13	PB32B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
N11	PB33A	4	T		PB33A	4	T	
GND	GND4	4			GND4	4		
N12	PB33B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
R12	PB34A	4			PB34A	4		
GND	GND4	4			GND4	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR36B	3	C	VREF2_3	PR44B	3	C	VREF2_3
N14	PR36A	3	T	VREF1_3	PR44A	3	T	VREF1_3

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
GND	-	-			GND	GND7	7		
C3	PL3A	7	T		C3	PL10A	7	T	
B2	PL3B	7	C		B2	PL10B	7	C	
E5	PL4A	7	T		E5	PL11A	7	T	
F5	PL4B	7	C		F5	PL11B	7	C	
D3	PL5A	7	T		D3	PL12A	7	T	
C2	PL5B	7	C		C2	PL12B	7	C	
GND	-	-			GND	GND7	7		
F4	PL6A	7	T	LDQS6	F4	PL14A	7	T	LDQS14
G4	PL6B	7	C		G4	PL14B	7	C	
E3	PL7A	7	T		E3	PL15A	7	T	
D2	PL7B	7	C		D2	PL15B	7	C	
B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL16A	7	T	LUM0_PLLT_IN_A
C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL16B	7	C	LUM0_PLLC_IN_A
F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL17B	7	C	LUM0_PLLC_FB_A
GND	-	-			GND	GND7	7		
G5	PL11A	7	T		G5	PL23A	7	T	LDQS23
H6	PL11B	7	C		H6	PL23B	7	C	
G3	PL12A	7	T		G3	PL24A	7	T	
H4	PL12B	7	C		H4	PL24B	7	C	
J5	PL13A	7	T		J5	PL25A	7	T	
H5	PL13B	7	C		H5	PL25B	7	C	
F2	PL14A	7	T		F2	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
F1	PL14B	7	C		F1	PL26B	7	C	
E1	PL15A	7	T		E1	PL27A	7	T	
D1	PL15B	7	C		D1	PL27B	7	C	
H3	PL16A	7	T		H3	PL28A	7	T	
G2	PL16B	7	C		G2	PL28B	7	C	
H2	PL17A	7	T		H2	PL29A	7	T	
G1	PL17B	7	C		G1	PL29B	7	C	
J4	PL18A	7	T		J4	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
J3	PL18B	7	C		J3	PL30B	7	C	
J2	PL19A	7	T	LDQS19	J2	PL31A	7	T	LDQS31
H1	PL19B	7	C		H1	PL31B	7	C	
K4	PL20A	7	T		K4	PL32A	7	T	
K5	PL20B	7	C		K5	PL32B	7	C	

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
E24	NC	-			E24	PR8B	2	C	
D24	NC	-			D24	PR8A	2	T	
E22	NC	-			E22	PR7B	2	C	
F22	NC	-			F22	PR7A	2	T	
E21	NC	-			E21	PR6B	2	C	
D22	NC	-			D22	PR6A	2	T	RDQS6
E23	PR2B	2	C	VREF1_2	E23	PR2B	2	C	VREF1_2
D23	PR2A	2	T	VREF2_2	D23	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
G20	NC	-			G20	PT65B	1	C	
F20	NC	-			F20	PT65A	1	T	
D21	NC	-			D21	PT64B	1	C	
C21	NC	-			C21	PT64A	1	T	
C23	NC	-			C23	PT63B	1	C	
C22	NC	-			C22	PT63A	1	T	
B23	NC	-			B23	PT62B	1	C	
C24	NC	-			C24	PT62A	1	T	TDQS62
D20	NC	-			D20	PT61B	1	C	
-	-	-			GND	GND1	1		
E19	NC	-			E19	PT61A	1	T	
B25	NC	-			B25	PT60B	1	C	
B24	NC	-			B24	PT60A	1	T	
B26	NC	-			B26	PT59B	1	C	
A25	NC	-			A25	PT59A	1	T	
C20	NC	-			C20	PT58B	1	C	
C19	NC	-			C19	PT58A	1	T	
A24	PT57B	1	C		A24	PT57B	1	C	
-	-	-			GND	GND1	1		
A23	PT57A	1	T		A23	PT57A	1	T	
E18	PT56B	1	C		E18	PT56B	1	C	
D19	PT56A	1	T		D19	PT56A	1	T	
F19	PT55B	1	C		F19	PT55B	1	C	
B22	PT55A	1	T		B22	PT55A	1	T	
G19	PT54B	1	C		G19	PT54B	1	C	
B21	PT54A	1	T	TDQS54	B21	PT54A	1	T	TDQS54
D18	PT53B	1	C		D18	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
C18	PT53A	1	T		C18	PT53A	1	T	
F18	PT52B	1	C		F18	PT52B	1	C	
A22	PT52A	1	T		A22	PT52A	1	T	
G18	PT51B	1	C		G18	PT51B	1	C	