Lattice Semiconductor Corporation - LFECP10E-4QN208C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	147
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp10e-4qn208c

LatticeECP/EC Family Data Sheet Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Figure 2-4. Slice Diagram

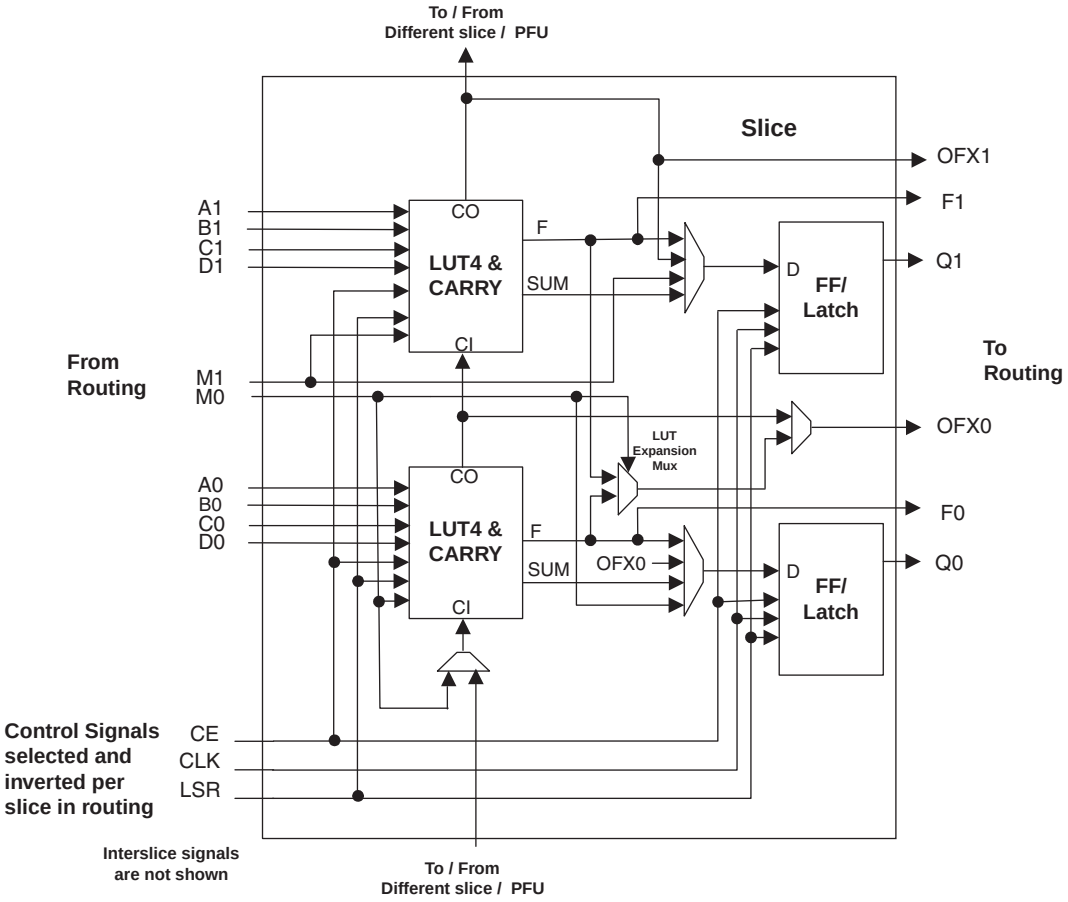


Table 2-1. Slice Signal Descriptions

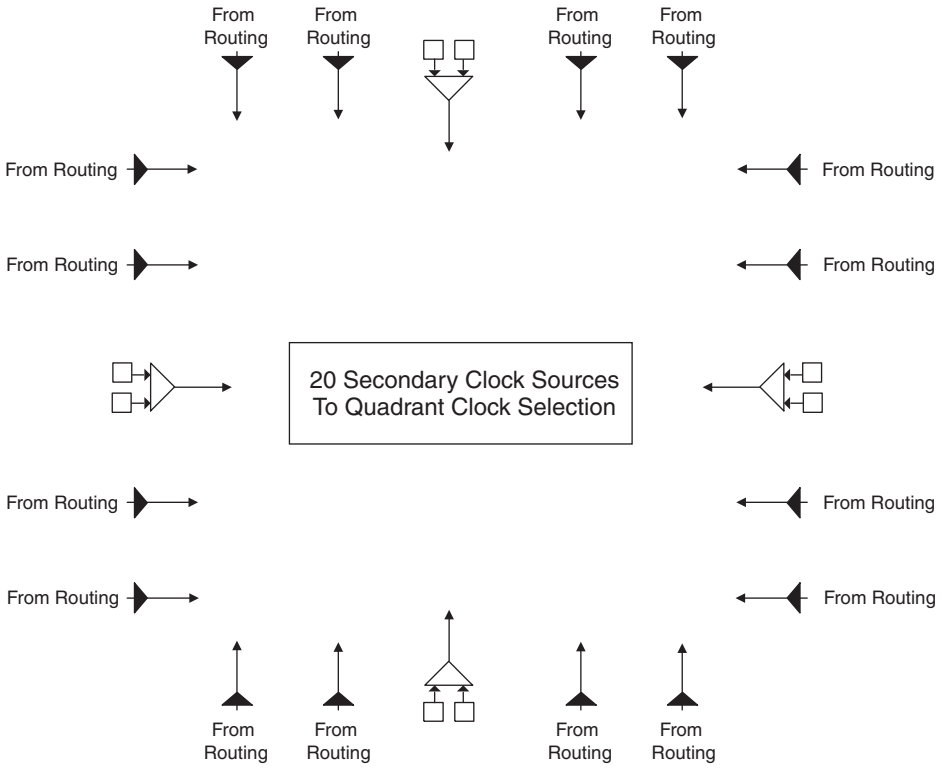
Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

Figure 2-7. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

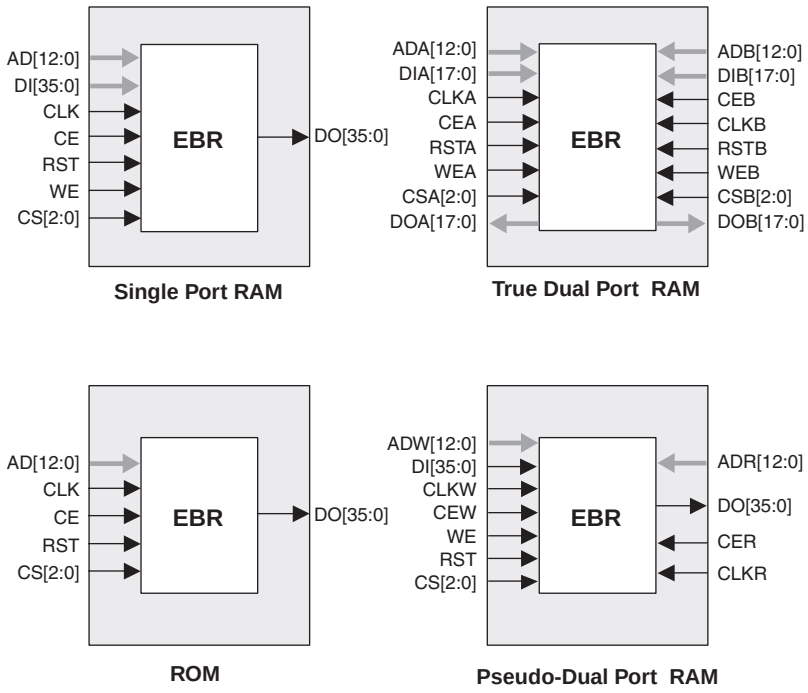
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



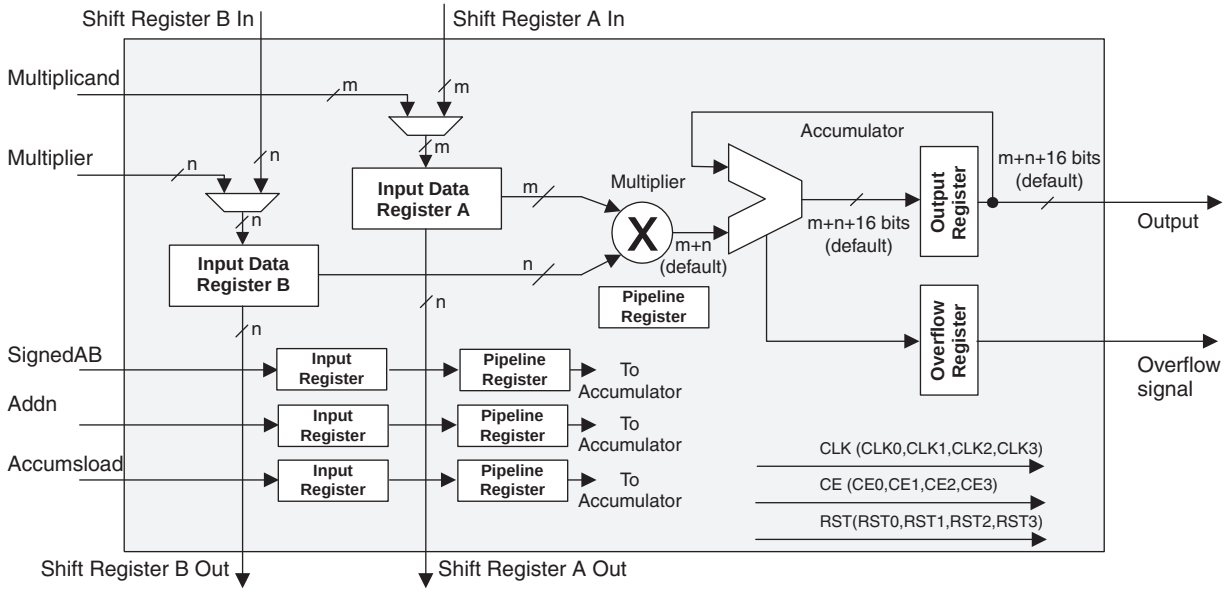
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

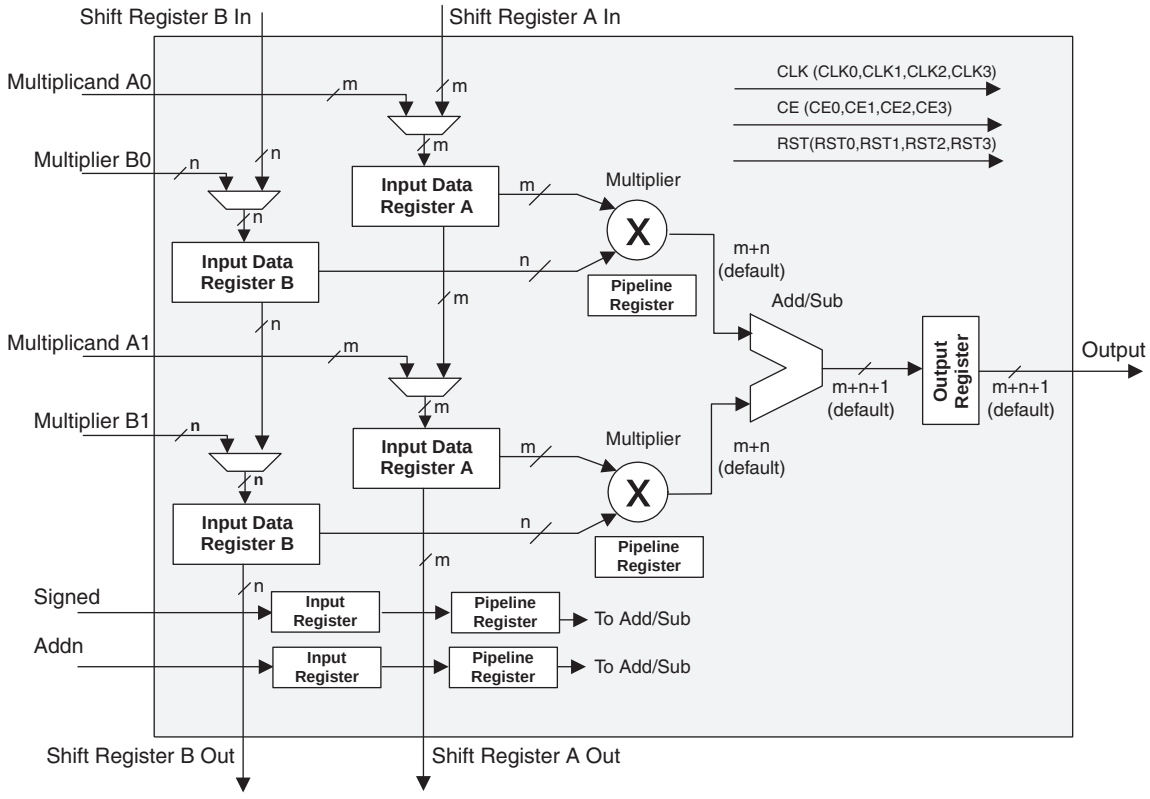
Figure 2-20. MAC sysDSP Element



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-21 shows the MULTADD sysDSP element.

Figure 2-21. MULTADD



LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from tICFG to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
C3	PL3A	7	T		PL3A	7	T	
C2	PL3B	7	C		PL3B	7	C	
B1	PL4A	7	T		PL4A	7	T	
C1	PL4B	7	C		PL4B	7	C	
E3	PL5A	7	T		PL5A	7	T	
E4	PL5B	7	C		PL5B	7	C	
F4	PL6A	7	T	LDQS6	PL6A	7	T	LDQS6
F5	PL6B	7	C		PL6B	7	C	
G4	PL7A	7	T		PL7A	7	T	
G3	PL7B	7	C		PL7B	7	C	
D2	PL8A	7	T		PL8A	7	T	
D1	PL8B	7	C		PL8B	7	C	
E1	PL9A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL9B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	NC	-			PL11A	6	T	
H5	NC	-			PL11B	6	C	
F2	NC	-			PL12A	6	T	
F1	NC	-			PL12B	6	C	
H4	NC	-			PL13A	6	T	
H3	NC	-			PL13B	6	C	
G2	NC	-			PL14A	6	T	
-	-	-			GND6	6		
G1	NC	-			PL14B	6	C	
J4	NC	-			PL15A	6	T	LDQS15
J3	NC	-			PL15B	6	C	
J5	NC	-			PL16A	6	T	
K5	NC	-			PL16B	6	C	
H2	NC	-			PL17A	6	T	
H1	NC	-			PL17B	6	C	
J2	NC	-			PL18A	6	T	
-	-	-			GND6	6		
J1	NC	-			PL18B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		
L3	TMS	6			TMS	6		
L5	TDO	6			TDO	6		
L4	VCCJ	6			VCCJ	6		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
K2	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
K1	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
L2	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
L1	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
M2	PL13A	6	T		PL22A	6	T	
M1	PL13B	6	C		PL22B	6	C	
N1	PL14A	6	T		PL23A	6	T	
GND	GND6	6			GND6	6		
N2	PL14B	6	C		PL23B	6	C	
M4	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
M3	PL15B	6	C		PL24B	6	C	
P1	PL16A	6	T		PL25A	6	T	
R1	PL16B	6	C		PL25B	6	C	
P2	PL17A	6	T		PL26A	6	T	
P3	PL17B	6	C		PL26B	6	C	
N3	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
N4	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
P4	PB2A	5	T		PB2A	5	T	
N5	PB2B	5	C		PB2B	5	C	
P5	PB3A	5	T		PB3A	5	T	
P6	PB3B	5	C		PB3B	5	C	
R4	PB4A	5	T		PB4A	5	T	
R3	PB4B	5	C		PB4B	5	C	
T2	PB5A	5	T		PB5A	5	T	
T3	PB5B	5	C		PB5B	5	C	
R5	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
R6	PB6B	5	C		PB6B	5	C	
T4	PB7A	5	T		PB7A	5	T	
T5	PB7B	5	C		PB7B	5	C	
N6	PB8A	5	T		PB8A	5	T	
M6	PB8B	5	C		PB8B	5	C	
T6	PB9A	5	T		PB9A	5	T	
GND	GND5	5			GND5	5		
T7	PB9B	5	C		PB9B	5	C	
P7	PB10A	5	T		PB10A	5	T	
N7	PB10B	5	C		PB10B	5	C	
R7	PB11A	5	T		PB11A	5	T	
R8	PB11B	5	C		PB11B	5	C	
M7	PB12A	5	T		PB12A	5	T	
M8	PB12B	5	C		PB12B	5	C	
T8	PB13A	5	T		PB13A	5	T	

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
L3	TMS	6			TMS	6		
L5	TDO	6			TDO	6		
L4	VCCJ	6			VCCJ	6		
K2	PL29A	6	T	LLM0_PLLT_IN_A	PL37A	6	T	LLM0_PLLT_IN_A
K1	PL29B	6	C	LLM0_PLLC_IN_A	PL37B	6	C	LLM0_PLLC_IN_A
L2	PL30A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A
L1	PL30B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A
M2	PL31A	6	T		PL39A	6	T	
M1	PL31B	6	C		PL39B	6	C	
N1	PL32A	6	T		PL40A	6	T	
GND	GND6	6			GND6	6		
-	-	-			GND6	6		
N2	PL32B	6	C		PL40B	6	C	
M4	PL33A	6	T	LDQS33	PL41A	6	T	LDQS41
M3	PL33B	6	C		PL41B	6	C	
P1	PL34A	6	T		PL42A	6	T	
R1	PL34B	6	C		PL42B	6	C	
P2	PL35A	6	T		PL43A	6	T	
P3	PL35B	6	C		PL43B	6	C	
N3	PL36A	6	T	VREF1_6	PL44A	6	T	VREF1_6
N4	PL36B	6	C	VREF2_6	PL44B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
GND	GND5	5			GND5	5		
P4	PB10A	5	T		PB10A	5	T	
N5	PB10B	5	C		PB10B	5	C	
P5	PB11A	5	T		PB11A	5	T	
P6	PB11B	5	C		PB11B	5	C	
R4	PB12A	5	T		PB12A	5	T	
R3	PB12B	5	C		PB12B	5	C	
T2	PB13A	5	T		PB13A	5	T	
GND	GND5	5			GND5	5		
T3	PB13B	5	C		PB13B	5	C	
R5	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
R6	PB14B	5	C		PB14B	5	C	
T4	PB15A	5	T		PB15A	5	T	
T5	PB15B	5	C		PB15B	5	C	
N6	PB16A	5	T		PB16A	5	T	
M6	PB16B	5	C		PB16B	5	C	
T6	PB17A	5	T		PB17A	5	T	
GND	GND5	5			GND5	5		
T7	PB17B	5	C		PB17B	5	C	
P7	PB18A	5	T		PB18A	5	T	

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N7	PB18B	5	C		PB18B	5	C	
R7	PB19A	5	T		PB19A	5	T	
R8	PB19B	5	C		PB19B	5	C	
M7	PB20A	5	T		PB20A	5	T	
M8	PB20B	5	C		PB20B	5	C	
T8	PB21A	5	T		PB21A	5	T	
GND	GND5	5			GND5	5		
T9	PB21B	5	C		PB21B	5	C	
P8	PB22A	5	T	BDQS22	PB22A	5	T	BDQS22
N8	PB22B	5	C		PB22B	5	C	
R9	PB23A	5	T		PB23A	5	T	
R10	PB23B	5	C		PB23B	5	C	
P9	PB24A	5	T	VREF2_5	PB24A	5	T	VREF2_5
N9	PB24B	5	C	VREF1_5	PB24B	5	C	VREF1_5
T10	PB25A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB25B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
T12	PB26A	4	T	WRITEN	PB26A	4	T	WRITEN
T13	PB26B	4	C	CS1N	PB26B	4	C	CS1N
P10	PB27A	4	T	VREF1_4	PB27A	4	T	VREF1_4
N10	PB27B	4	C	CSN	PB27B	4	C	CSN
T14	PB28A	4	T	VREF2_4	PB28A	4	T	VREF2_4
T15	PB28B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
M10	PB29A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB29B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
R11	PB30A	4	T	BDQS30	PB30A	4	T	BDQS30
P11	PB30B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
R13	PB31A	4	T		PB31A	4	T	
R14	PB31B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
P12	PB32A	4	T		PB32A	4	T	
P13	PB32B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
N11	PB33A	4	T		PB33A	4	T	
GND	GND4	4			GND4	4		
N12	PB33B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
R12	PB34A	4			PB34A	4		
GND	GND4	4			GND4	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR36B	3	C	VREF2_3	PR44B	3	C	VREF2_3
N14	PR36A	3	T	VREF1_3	PR44A	3	T	VREF1_3

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND	GND5	5			GND	GND5	5		
V7	NC	-			V7	PB2A	5	T		V7	PB2A	5	T	
T6	NC	-			T6	PB2B	5	C		T6	PB2B	5	C	
V8	NC	-			V8	PB3A	5	T		V8	PB3A	5	T	
U7	NC	-			U7	PB3B	5	C		U7	PB3B	5	C	
W5	NC	-			W5	PB4A	5	T		W5	PB4A	5	T	
U6	NC	-			U6	PB4B	5	C		U6	PB4B	5	C	
AA3	NC	-			AA3	PB5A	5	T		AA3	PB5A	5	T	
AB3	NC	-			AB3	PB5B	5	C		AB3	PB5B	5	C	
Y6	NC	-			Y6	PB6A	5	T	BDQS6	Y6	PB6A	5	T	BDQS6
V6	NC	-			V6	PB6B	5	C		V6	PB6B	5	C	
AA5	NC	-			AA5	PB7A	5	T		AA5	PB7A	5	T	
W6	NC	-			W6	PB7B	5	C		W6	PB7B	5	C	
Y5	NC	-			Y5	PB8A	5	T		Y5	PB8A	5	T	
Y4	NC	-			Y4	PB8B	5	C		Y4	PB8B	5	C	
AA4	NC	-			AA4	PB9A	5	T		AA4	PB9A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
AB4	NC	-			AB4	PB9B	5	C		AB4	PB9B	5	C	
Y7	PB2A	5	T		Y7	PB10A	5	T		Y7	PB10A	5	T	
W8	PB2B	5	C		W8	PB10B	5	C		W8	PB10B	5	C	
W7	PB3A	5	T		W7	PB11A	5	T		W7	PB11A	5	T	
U8	PB3B	5	C		U8	PB11B	5	C		U8	PB11B	5	C	
W9	PB4A	5	T		W9	PB12A	5	T		W9	PB12A	5	T	
U9	PB4B	5	C		U9	PB12B	5	C		U9	PB12B	5	C	
Y8	PB5A	5	T		Y8	PB13A	5	T		Y8	PB13A	5	T	
GND	-	-			GND	GND5	5			GND	GND5	5		
Y9	PB5B	5	C		Y9	PB13B	5	C		Y9	PB13B	5	C	
V9	PB6A	5	T	BDQS6	V9	PB14A	5	T	BDQS14	V9	PB14A	5	T	BDQS14
T9	PB6B	5	C		T9	PB14B	5	C		T9	PB14B	5	C	
W10	PB7A	5	T		W10	PB15A	5	T		W10	PB15A	5	T	
U10	PB7B	5	C		U10	PB15B	5	C		U10	PB15B	5	C	
V10	PB8A	5	T		V10	PB16A	5	T		V10	PB16A	5	T	
T10	PB8B	5	C		T10	PB16B	5	C		T10	PB16B	5	C	
AA6	PB9A	5	T		AA6	PB17A	5	T		AA6	PB17A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB5	PB9B	5	C		AB5	PB17B	5	C		AB5	PB17B	5	C	
AA8	PB10A	5	T		AA8	PB18A	5	T		AA8	PB18A	5	T	
AA7	PB10B	5	C		AA7	PB18B	5	C		AA7	PB18B	5	C	
AB6	PB11A	5	T		AB6	PB19A	5	T		AB6	PB19A	5	T	
AB7	PB11B	5	C		AB7	PB19B	5	C		AB7	PB19B	5	C	
Y10	PB12A	5	T		Y10	PB20A	5	T		Y10	PB20A	5	T	
W11	PB12B	5	C		W11	PB20B	5	C		W11	PB20B	5	C	
AB8	PB13A	5	T		AB8	PB21A	5	T		AB8	PB21A	5	T	
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB9	PB13B	5	C		AB9	PB21B	5	C		AB9	PB21B	5	C	
AA10	PB14A	5	T	BDQS14	AA10	PB22A	5	T	BDQS22	AA10	PB22A	5	T	BDQS22
AA9	PB14B	5	C		AA9	PB22B	5	C		AA9	PB22B	5	C	
Y11	PB15A	5	T		Y11	PB23A	5	T		Y11	PB23A	5	T	
AA11	PB15B	5	C		AA11	PB23B	5	C		AA11	PB23B	5	C	
V11	PB16A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5	V11	PB24A	5	T	VREF2_5

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K3	PL21A	7	T		K3	PL33A	7	T	
K2	PL21B	7	C		K2	PL33B	7	C	
J1	PL22A	7	T	PCLKT7_0	J1	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
K1	PL22B	7	C	PCLKC7_0	K1	PL34B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6		
L4	PL24A	6	T		L4	PL36A	6	T	
L5	PL24B	6	C		L5	PL36B	6	C	
L2	PL25A	6	T		L2	PL37A	6	T	
L1	PL25B	6	C		L1	PL37B	6	C	
M4	PL26A	6	T		M4	PL38A	6	T	
M5	PL26B	6	C		M5	PL38B	6	C	
M1	PL27A	6	T		M1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
M2	PL27B	6	C		M2	PL39B	6	C	
N3	PL28A	6	T	LDQS28	N3	PL40A	6	T	LDQS40
M3	PL28B	6	C		M3	PL40B	6	C	
N5	PL29A	6	T		N5	PL41A	6	T	
N4	PL29B	6	C		N4	PL41B	6	C	
N1	PL30A	6	T		N1	PL42A	6	T	
N2	PL30B	6	C		N2	PL42B	6	C	
P1	PL31A	6	T		P1	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
P2	PL31B	6	C		P2	PL43B	6	C	
R6	PL32A	6	T		R6	PL44A	6	T	
P5	PL32B	6	C		P5	PL44B	6	C	
P3	PL33A	6	T		P3	PL45A	6	T	
P4	PL33B	6	C		P4	PL45B	6	C	
R1	PL34A	6	T		R1	PL46A	6	T	
R2	PL34B	6	C		R2	PL46B	6	C	
R5	PL35A	6	T		R5	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
R4	PL35B	6	C		R4	PL47B	6	C	
T1	PL36A	6	T	LDQS36	T1	PL48A	6	T	LDQS48
T2	PL36B	6	C		T2	PL48B	6	C	
R3	PL37A	6	T		R3	PL49A	6	T	
T3	PL37B	6	C		T3	PL49B	6	C	
GND	GND6	6			GND	GND6	6		
T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6		
V1	PL41A	6	T	LLM0_PLLT_IN_A	V1	PL53A	6	T	LLM0_PLLT_IN_A

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AC13	PB32B	5	C	VREF1_5	AC13	PB32B	5	C	VREF1_5
AF14	PB33A	5	T	PCLKT5_0	AF14	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AE14	PB33B	5	C	PCLKC5_0	AE14	PB33B	5	C	PCLKC5_0
AA13	PB34A	4	T	WRITEN	AA13	PB34A	4	T	WRITEN
AB13	PB34B	4	C	CS1N	AB13	PB34B	4	C	CS1N
AD14	PB35A	4	T	VREF1_4	AD14	PB35A	4	T	VREF1_4
AA14	PB35B	4	C	CSN	AA14	PB35B	4	C	CSN
AC14	PB36A	4	T	VREF2_4	AC14	PB36A	4	T	VREF2_4
AB14	PB36B	4	C	D0/SPID7	AB14	PB36B	4	C	D0/SPID7
AF15	PB37A	4	T	D2/SPID5	AF15	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AE15	PB37B	4	C	D1/SPID6	AE15	PB37B	4	C	D1/SPID6
AD15	PB38A	4	T	BDQS38	AD15	PB38A	4	T	BDQS38
AC15	PB38B	4	C	D3/SPID4	AC15	PB38B	4	C	D3/SPID4
AF16	PB39A	4	T		AF16	PB39A	4	T	
Y14	PB39B	4	C	D4/SPID3	Y14	PB39B	4	C	D4/SPID3
AE16	PB40A	4	T		AE16	PB40A	4	T	
AB15	PB40B	4	C	D5/SPID2	AB15	PB40B	4	C	D5/SPID2
AF17	PB41A	4	T		AF17	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AE17	PB41B	4	C	D6/SPID1	AE17	PB41B	4	C	D6/SPID1
Y15	PB42A	4	T		Y15	PB42A	4	T	
AA15	PB42B	4	C		AA15	PB42B	4	C	
AD17	PB43A	4	T		AD17	PB43A	4	T	
Y16	PB43B	4	C		Y16	PB43B	4	C	
AD18	PB44A	4	T		AD18	PB44A	4	T	
AC16	PB44B	4	C		AC16	PB44B	4	C	
AE18	PB45A	4	T		AE18	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AF18	PB45B	4	C		AF18	PB45B	4	C	
AD16	PB46A	4	T	BDQS46	AD16	PB46A	4	T	BDQS46
AB16	PB46B	4	C		AB16	PB46B	4	C	
AF19	PB47A	4	T		AF19	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AA17	PB48A	4	T		AA17	PB48A	4	T	
Y17	PB48B	4	C		Y17	PB48B	4	C	
AF21	PB49A	4	T		AF21	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AF20	PB49B	4	C		AF20	PB49B	4	C	
AE21	PB50A	4	T		AE21	PB50A	4	T	
AC17	PB50B	4	C		AC17	PB50B	4	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFECP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFECP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFECP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFECP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFECP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFECP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFECP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFECP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFECP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFECP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFECP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFECP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFECP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFECP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFECP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFECP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFECP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFECP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFECP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFECP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFECP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFECP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFECP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFECP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFECP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFECP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFECP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFECP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFECP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFECP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFECP33E-5F672C	496	-5	fpBGA	672	COM	32.8K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFECP6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFECP6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFECP6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFECP6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFECP6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFECP6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFECP6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFECP10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFECP10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFECP10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFECP10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFECP10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFECP15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFECP15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFECP15E-4F256I	195	-4	fpBGA	256	IND	15.3K

LatticeECP Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFECP20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFECP20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFECP20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F672I	496	-3	fpBGA	672	IND	32.8K
LFECP33E-4F672I	496	-4	fpBGA	672	IND	32.8K
LFECP33E-3F484I	360	-3	fpBGA	484	IND	32.8K
LFECP33E-4F484I	360	-4	fpBGA	484	IND	32.8K

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFEC10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFEC10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC1E-3QN208I	112	-3	Lead-Free PQFP	208	IND	1.5K
LFEC1E-4QN208I	112	-4	Lead-Free PQFP	208	IND	1.5K
LFEC1E-3TN144I	97	-3	Lead-Free TQFP	144	IND	1.5K
LFEC1E-4TN144I	97	-4	Lead-Free TQFP	144	IND	1.5K
LFEC1E-3TN100I	67	-3	Lead-Free TQFP	100	IND	1.5K
LFEC1E-4TN100I	67	-4	Lead-Free TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC3E-3FN256I	160	-3	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-4FN256I	160	-4	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-3QN208I	145	-3	Lead-Free PQFP	208	IND	3.1K
LFEC3E-4QN208I	145	-4	Lead-Free PQFP	208	IND	3.1K
LFEC3E-3TN144I	97	-3	Lead-Free TQFP	144	IND	3.1K
LFEC3E-4TN144I	97	-4	Lead-Free TQFP	144	IND	3.1K
LFEC3E-3TN100I	67	-3	Lead-Free TQFP	100	IND	3.1K
LFEC3E-4TN100I	67	-4	Lead-Free TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K