Lattice Semiconductor Corporation - LFECP15E-4FN256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15400
Total RAM Bits	358400
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp15e-4fn256c

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (EConomy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (EConomy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (EConomy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)

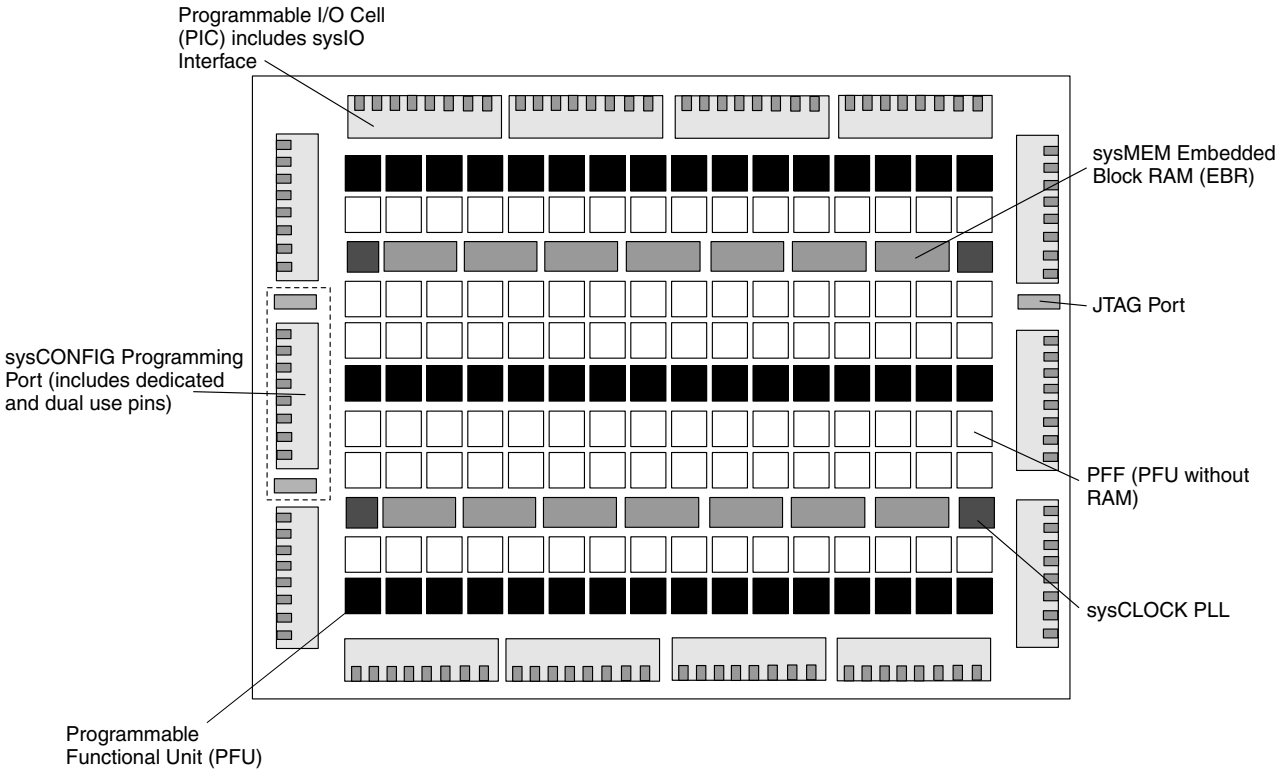
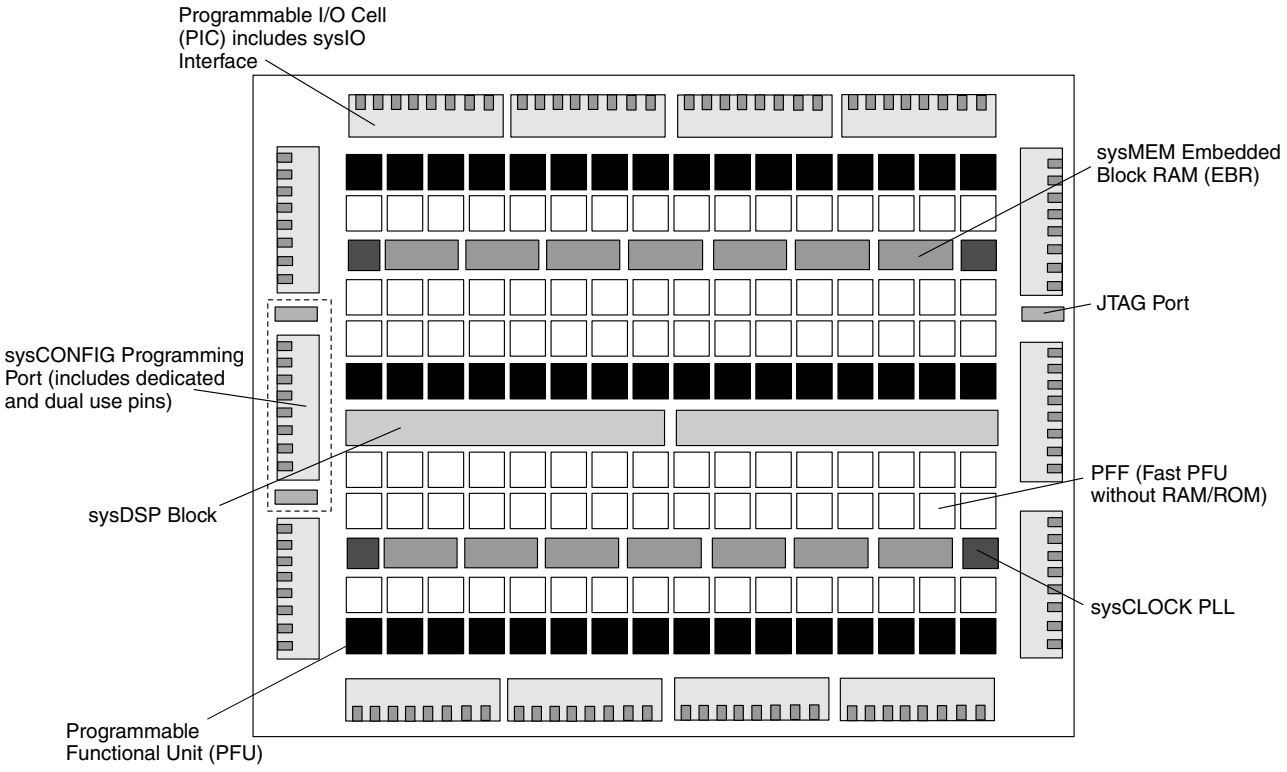


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)



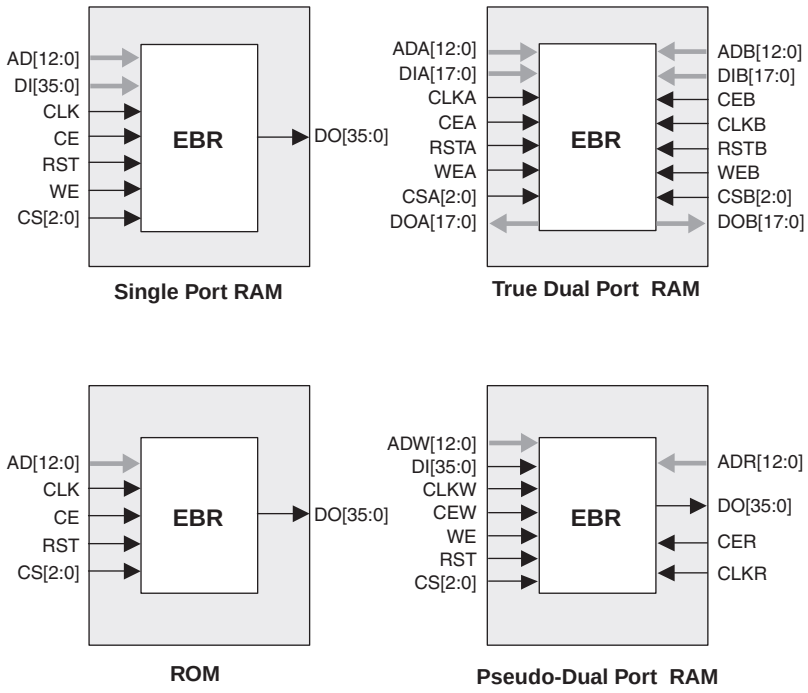
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



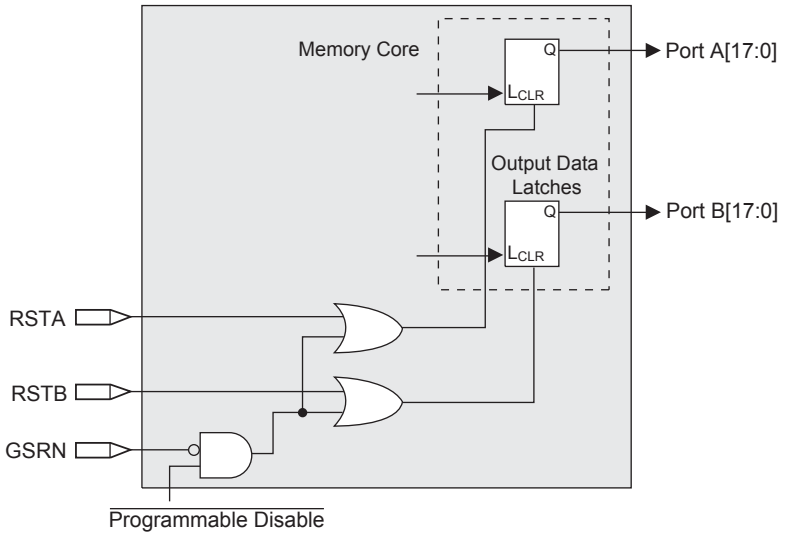
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-16. Memory Core Reset

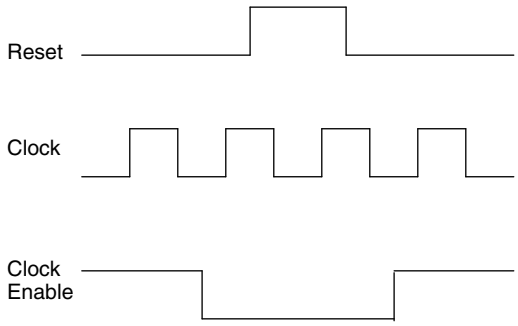


For further information about sysMEM EBR block, please see the the list of technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-17. The GSR input to the EBR is always asynchronous.

Figure 2-17. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

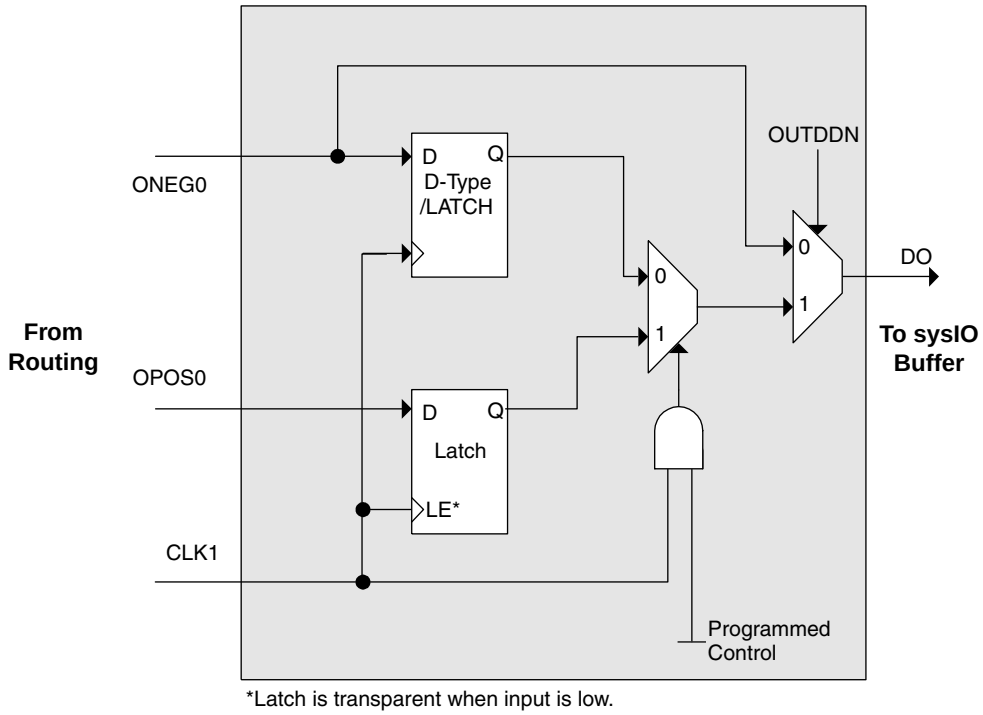
These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP Block

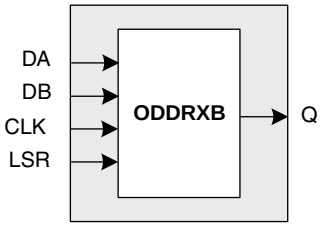
The LatticeECP-DSP family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and

Figure 2-29. Output Register Block



*Latch is transparent when input is low.

Figure 2-30. ODDRXB Primitive

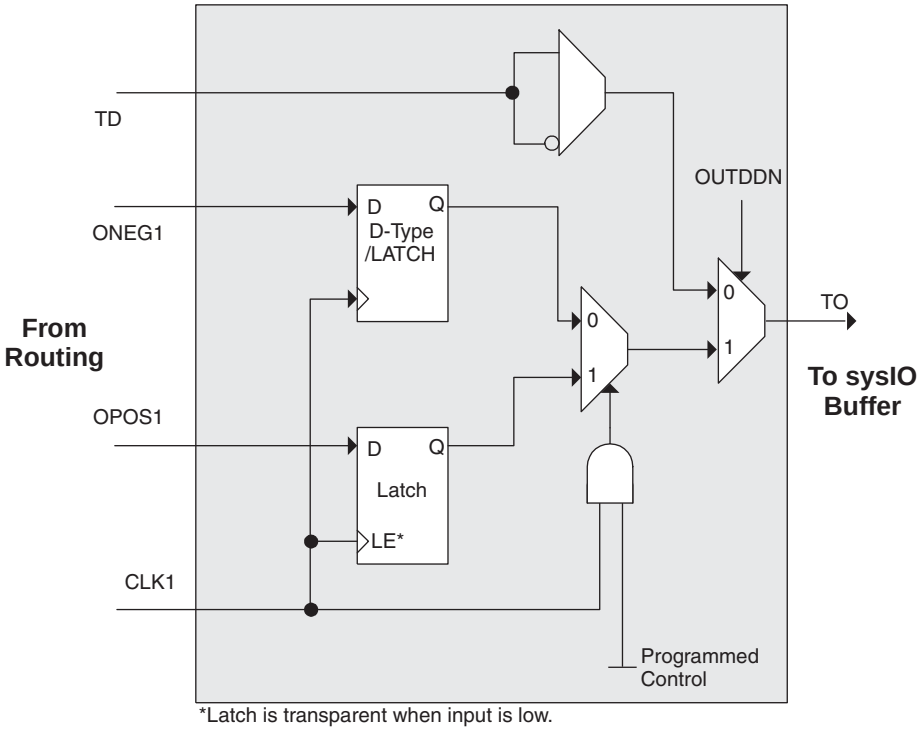


Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-31. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCIO} - 0.2V)	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	(V_{CCIO} - 0.2V) ð V_{IH} ð 3.6V	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCIO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO}.

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold		+/-100	—	—	mV
V_{CM}	Input common mode voltage	100mV ð V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ð V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ð V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	5.5	ns
32-bit decoder	6.9	ns
64-bit decoder	7.1	ns
4:1 MUX	4.3	ns
8:1 MUX	4.7	ns
16:1 MUX	5.0	ns
32:1 MUX	5.5	ns

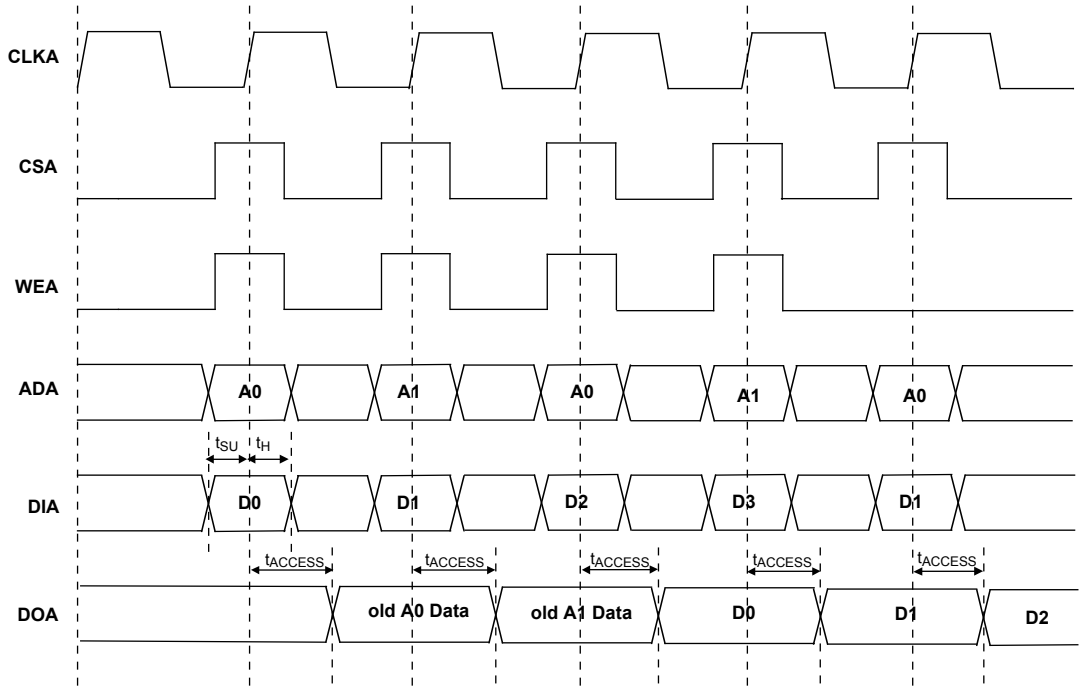
Register-to-Register Performance[1]

Function	-5 Timing	Units
Basic Functions		
16 bit decoder	410	MHz
32 bit decoder	283	MHz
64 bit decoder	272	MHz
4:1 MUX	613	MHz
8:1 MUX	565	MHz
16:1 MUX	526	MHz
32:1 MUX	442	MHz
8-bit adder	363	MHz
16-bit adder	353	MHz
64-bit adder	196	MHz
16-bit counter	414	MHz
32-bit counter	317	MHz
64-bit counter	216	MHz
64-bit accumulator	178	MHz
Embedded Memory Functions		
256x36 Single Port RAM	280	MHz
512x18 True-Dual Port RAM	280	MHz
Distributed Memory Functions		
16x2 Single Port RAM	460	MHz
64x2 Single Port RAM	375	MHz
128x4 Single Port RAM	294	MHz
32x2 Pseudo-Dual Port RAM	392	MHz
64x4 Pseudo-Dual Port RAM	332	MHz
DSP Function[2]		
9x9 Pipelined Multiply/Accumulate	242	MHz
18x18 Pipelined Multiply/Accumulate	238	MHz
36x36 Pipelined Multiply	235	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Applies to LatticeECP devices only.

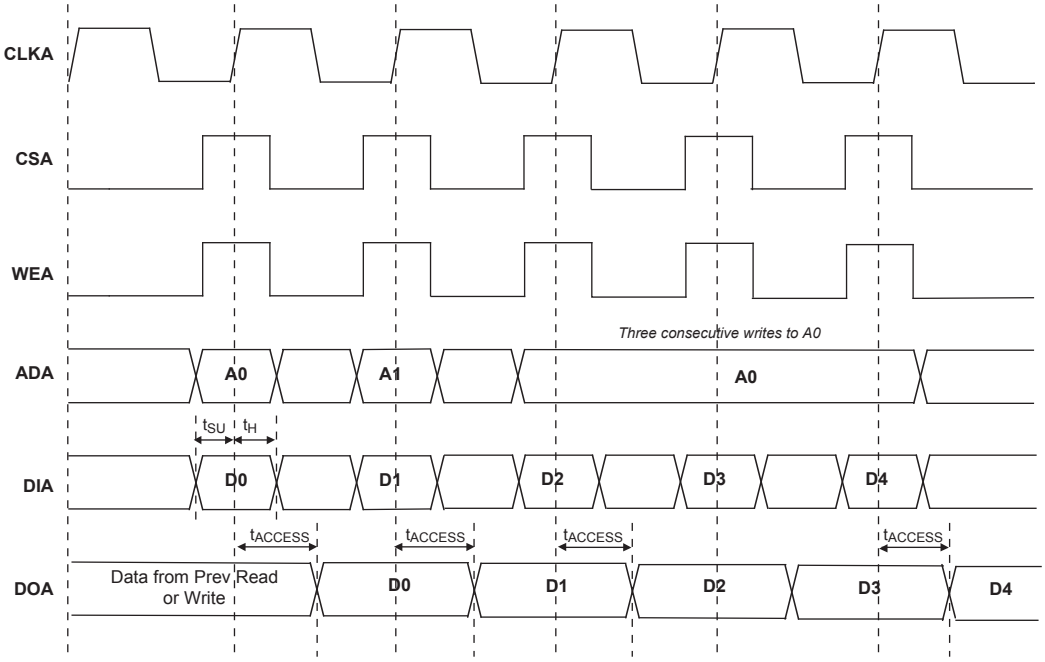
Timing v.G 0.30

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



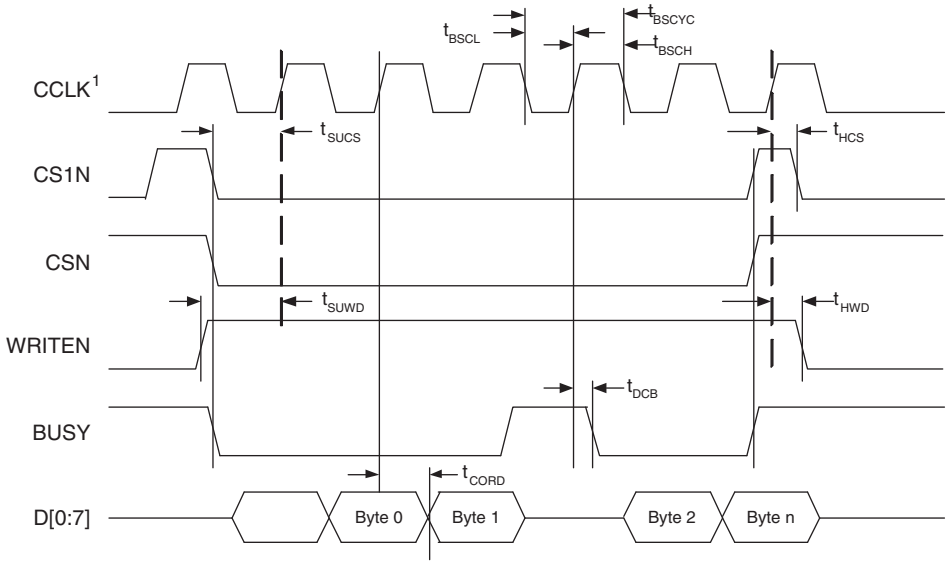
Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



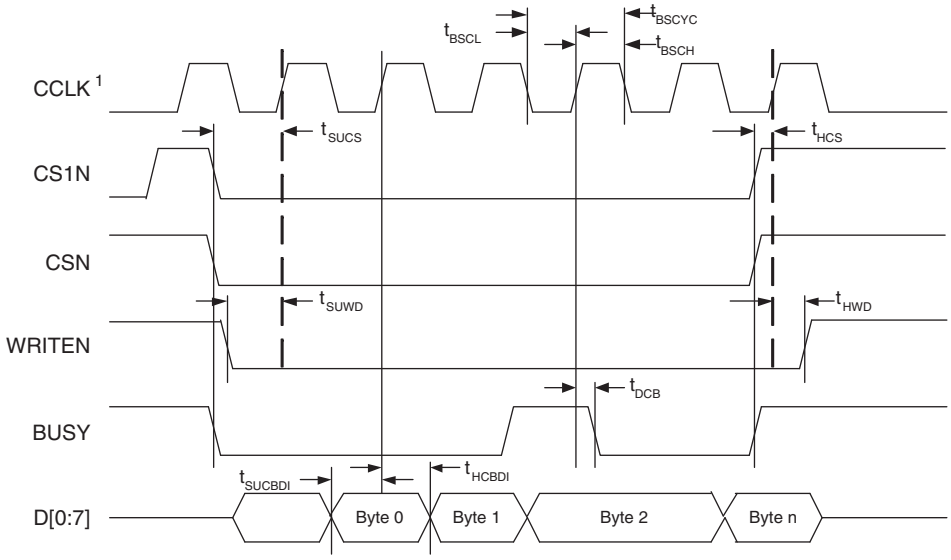
Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-12. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-13. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-14. sysCONFIG Master Serial Port Timing

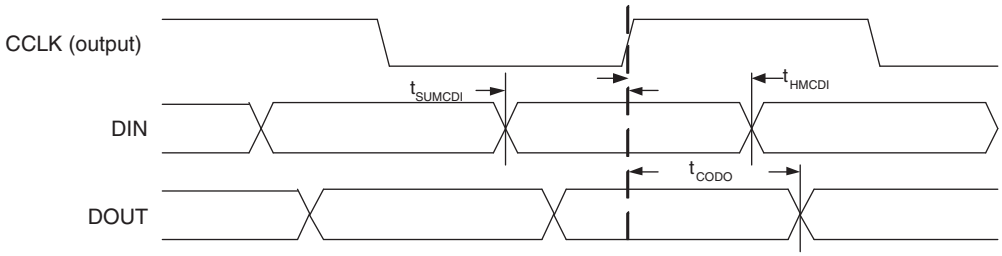


Figure 3-15. sysCONFIG Slave Serial Port Timing

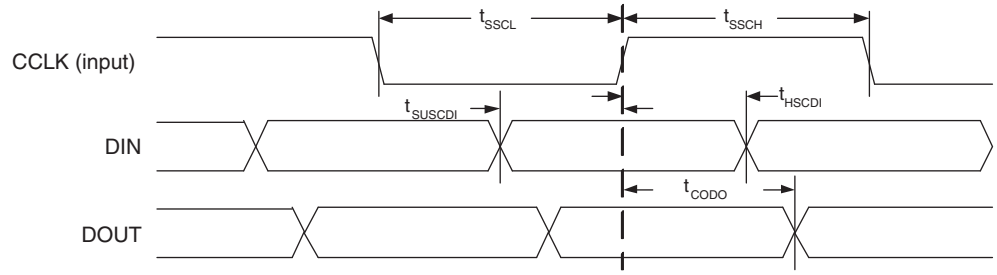
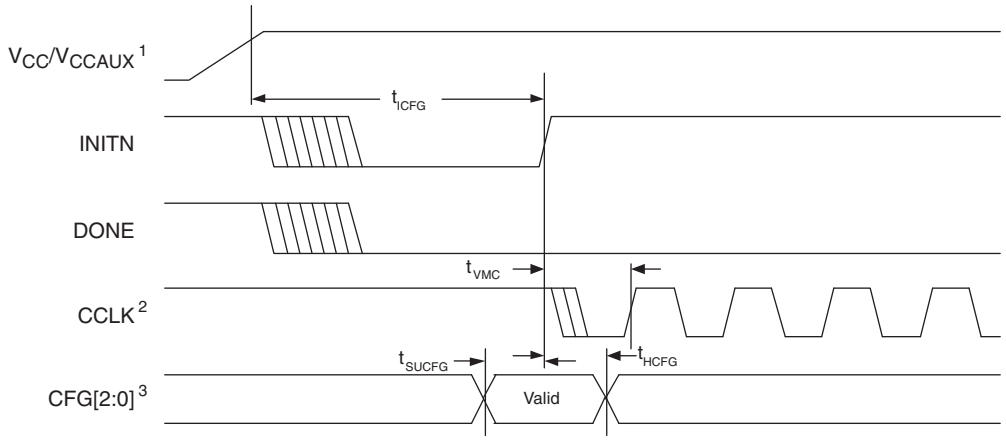


Figure 3-16. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX}, whichever is the last to reach its V_{MIN}.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

Pin Information Summary (Cont.)

Pin Type		LFECP/EC15		LFECP20/EC20		LFECP/EC33	
		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V_{CC}		10	20	20	32	16	28
V_{CCAUX}		2	12	12	20	12	20
V_{CCPLL}		0	0	0	0	4	4
V_{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V_{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	VCCAUX	-			VCCAUX	-		
137	PR9B	2	C	PCLKC2_0	PR18B	2	C	PCLKC2_0
138	GND2	2			GND2	2		
139	PR9A	2	T	PCLKT2_0	PR18A	2	T	PCLKT2_0
140	PR8B	2	C		PR17B	2	C	
141	PR8A	2	T		PR17A	2	T	
142	PR7B	2	C		PR16B	2	C	
143	PR7A	2	T		PR16A	2	T	
144	PR6B	2	C		PR15B	2	C	
145	VCCIO2	2			VCCIO2	2		
146	PR6A	2	T	RDQS6	PR15A	2	T	RDQS15
147	PR5B	2	C		PR14B	2	C	
148	PR5A	2	T		PR14A	2	T	
149	PR4B	2	C		PR13B	2	C	
150	PR4A	2	T		PR13A	2	T	
151	NC	-			GND	-		
152	NC	-			VCC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	PT33A	1			PT41A	1		
159	PT25B	1	C		PT33B	1	C	
160	PT25A	1	T		PT33A	1	T	
161	PT24B	1	C		PT32B	1	C	
162	PT24A	1	T		PT32A	1	T	
163	PT23B	1	C		PT31B	1	C	
164	PT23A	1	T		PT31A	1	T	
165	PT22B	1	C		PT30B	1	C	
166	PT22A	1	T	TDQS22	PT30A	1	T	TDQS30
167	PT21B	1	C		PT29B	1	C	
168	GND1	1			GND1	1		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N16	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
N15	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
M15	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
M16	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
L16	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
K16	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
J16	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
	-	-			GND3	3		
H16	NC	-			PR18B	3	C	
H15	NC	-			PR18A	3	T	
G16	NC	-			PR17B	3	C	
G15	NC	-			PR17A	3	T	
K12	NC	-			PR16B	3	C	
J12	NC	-			PR16A	3	T	
J14	NC	-			PR15B	3	C	
J15	NC	-			PR15A	3	T	RDQS15
F16	NC	-			PR14B	3	C	
-	-	-			GND3	3		
F15	NC	-			PR14A	3	T	
J13	NC	-			PR13B	3	C	
H13	NC	-			PR13A	3	T	
H14	NC	-			PR12B	3	C	
G14	NC	-			PR12A	3	T	
E16	NC	-			PR11B	3	C	
E15	NC	-			PR11A	3	T	
H12	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
GND	GND2	2			GND2			
G12	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
G13	PR8B	2	C		PR8B	2	C	
F13	PR8A	2	T		PR8A	2	T	
F12	PR7B	2	C		PR7B	2	C	
E13	PR7A	2	T		PR7A	2	T	
D16	PR6B	2	C		PR6B	2	C	
D15	PR6A	2	T	RDQS6	PR6A	2	T	RDQS6
F14	PR5B	2	C		PR5B	2	C	
E14	PR5A	2	T		PR5A	2	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
J14	VCCIO1	1			J14	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
J16	VCCIO1	1			J16	VCCIO1	1		
J17	VCCIO1	1			J17	VCCIO1	1		
K17	VCCIO2	2			K17	VCCIO2	2		
K18	VCCIO2	2			K18	VCCIO2	2		
L18	VCCIO2	2			L18	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
N18	VCCIO2	2			N18	VCCIO2	2		
N19	VCCIO2	2			N19	VCCIO2	2		
P18	VCCIO3	3			P18	VCCIO3	3		
P19	VCCIO3	3			P19	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
R19	VCCIO3	3			R19	VCCIO3	3		
T18	VCCIO3	3			T18	VCCIO3	3		
U18	VCCIO3	3			U18	VCCIO3	3		
V14	VCCIO4	4			V14	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
V16	VCCIO4	4			V16	VCCIO4	4		
V17	VCCIO4	4			V17	VCCIO4	4		
W14	VCCIO4	4			W14	VCCIO4	4		
W15	VCCIO4	4			W15	VCCIO4	4		
V10	VCCIO5	5			V10	VCCIO5	5		
V11	VCCIO5	5			V11	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
V13	VCCIO5	5			V13	VCCIO5	5		
W12	VCCIO5	5			W12	VCCIO5	5		
W13	VCCIO5	5			W13	VCCIO5	5		
P8	VCCIO6	6			P8	VCCIO6	6		
P9	VCCIO6	6			P9	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T9	VCCIO6	6			T9	VCCIO6	6		
U9	VCCIO6	6			U9	VCCIO6	6		
K9	VCCIO7	7			K9	VCCIO7	7		
L9	VCCIO7	7			L9	VCCIO7	7		
M8	VCCIO7	7			M8	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
N8	VCCIO7	7			N8	VCCIO7	7		
N9	VCCIO7	7			N9	VCCIO7	7		
G13	VCCAUX	-			G13	VCCAUX	-		
H20	VCCAUX	-			H20	VCCAUX	-		

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFECP33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFECP33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3T100I	67	-3	TQFP	100	IND	1.5K
LFEC1E-4T100I	67	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256I	160	-3	fpBGA	256	IND	3.1K
LFEC3E-4F256I	160	-4	fpBGA	256	IND	3.1K
LFEC3E-3Q208I	145	-3	PQFP	208	IND	3.1K
LFEC3E-4Q208I	145	-4	PQFP	208	IND	3.1K
LFEC3E-3T144I	97	-3	TQFP	144	IND	3.1K
LFEC3E-4T144I	97	-4	TQFP	144	IND	3.1K
LFEC3E-3T100I	67	-3	TQFP	100	IND	3.1K
LFEC3E-4T100I	67	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3 P208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4 P208I	147	-4	PQFP	208	IND	10.2K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFECP6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFECP6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFECP6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFECP6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFECP6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFECP6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFECP6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFECP10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFECP10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFECP10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFECP10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFECP10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFECP15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFECP15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFECP15E-4F256I	195	-4	fpBGA	256	IND	15.3K