Lattice Semiconductor Corporation - LFECP15E-5FN256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15400
Total RAM Bits	358400
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp15e-5fn256c

LatticeECP/EC Family Data Sheet Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

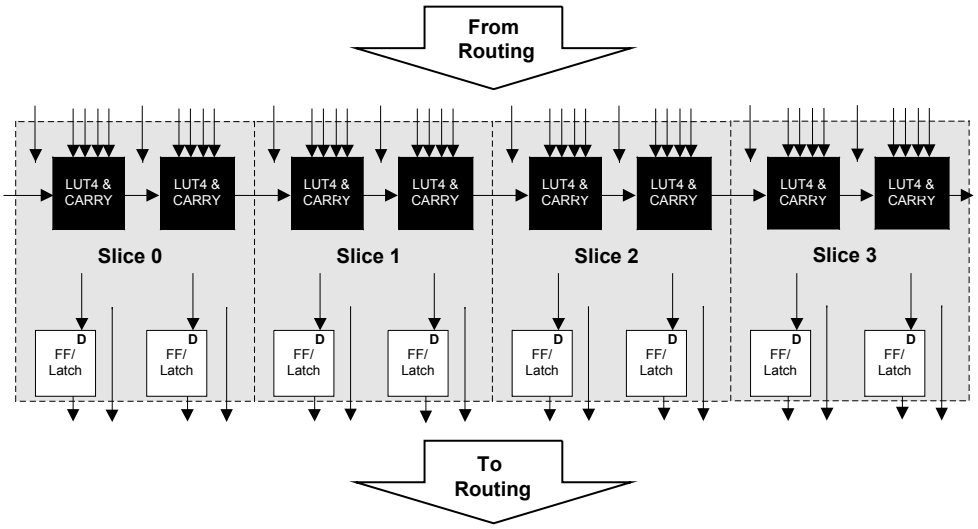
1. LatticeECP devices only.

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

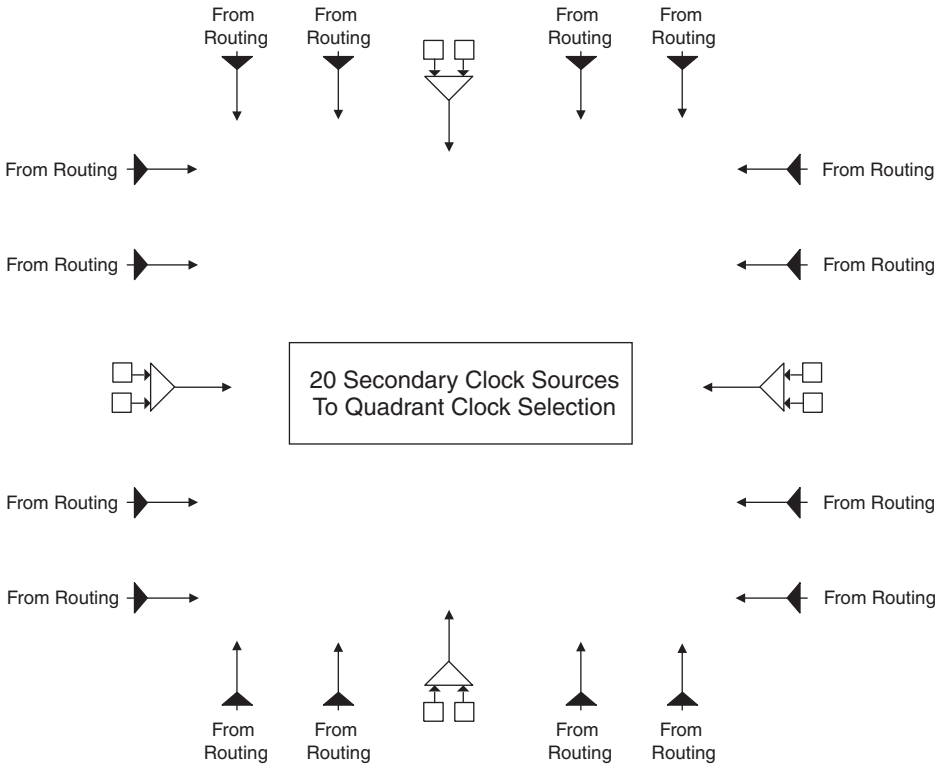
Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

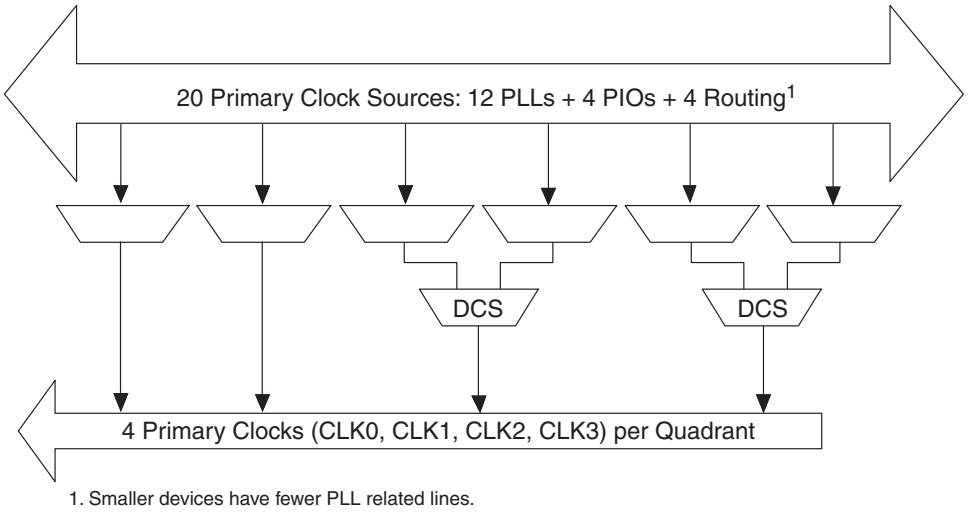
Figure 2-7. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

Figure 2-8. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-9. Per Quadrant Secondary Clock Selection

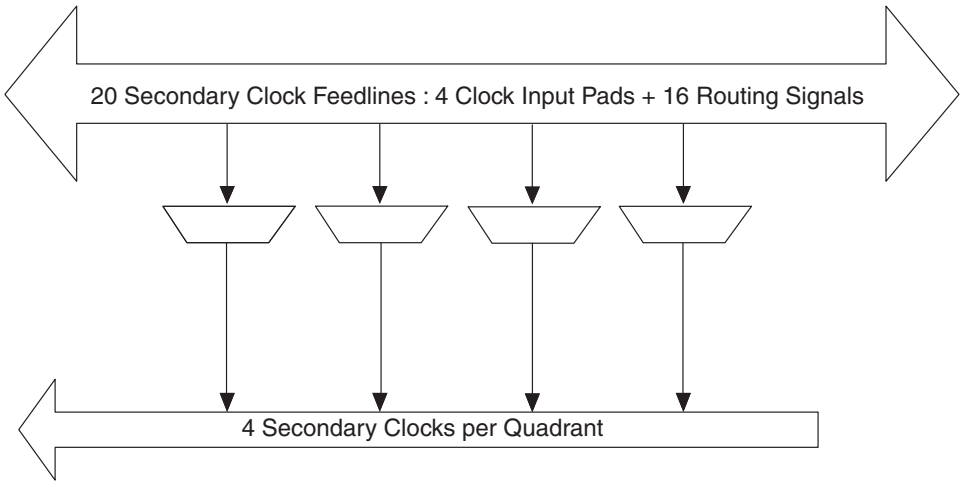
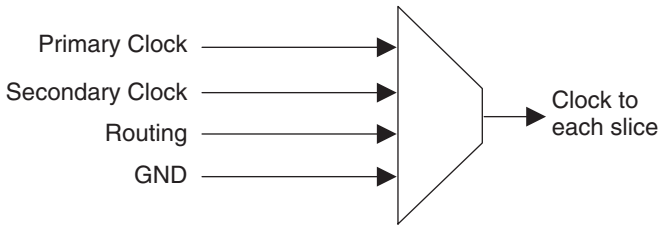


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-27 shows the input register waveforms for DDR operation and Figure 2-28 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Diagram

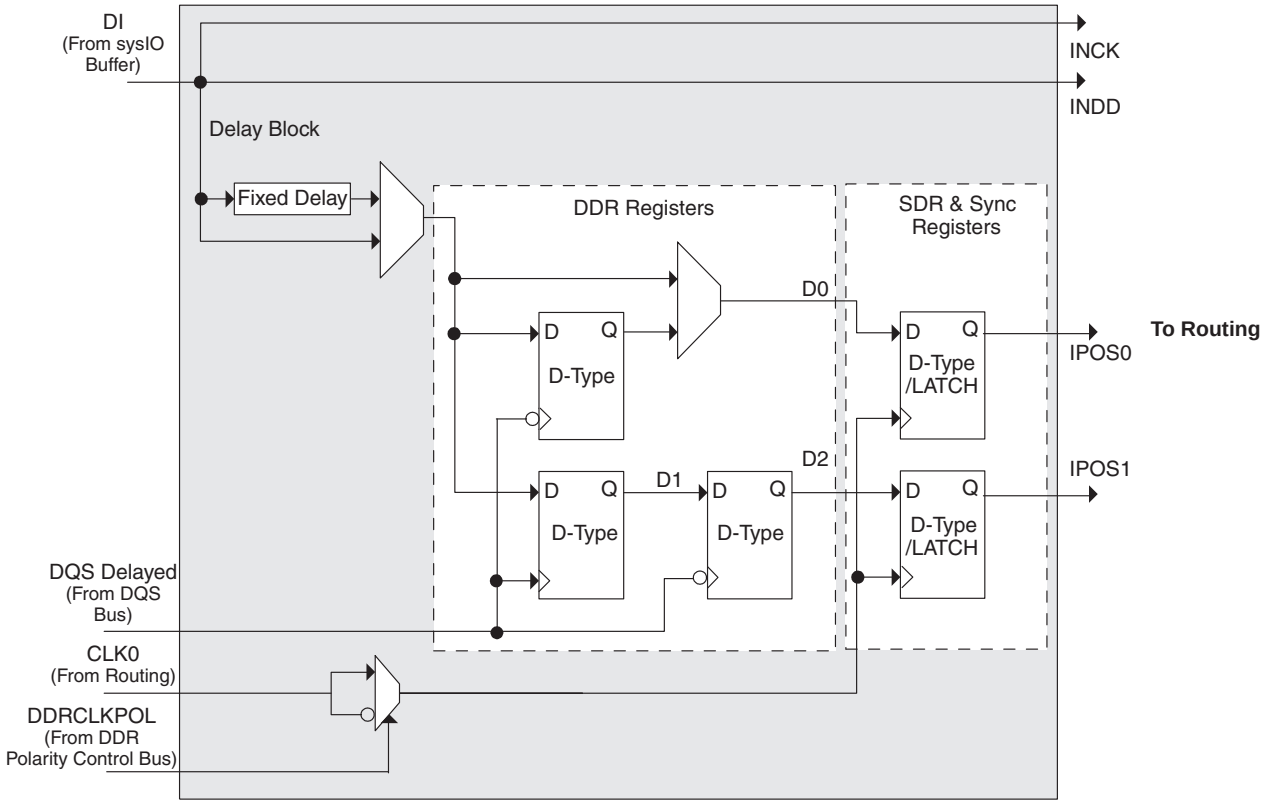


Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

BLVDS

The LatticeECP/EC devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

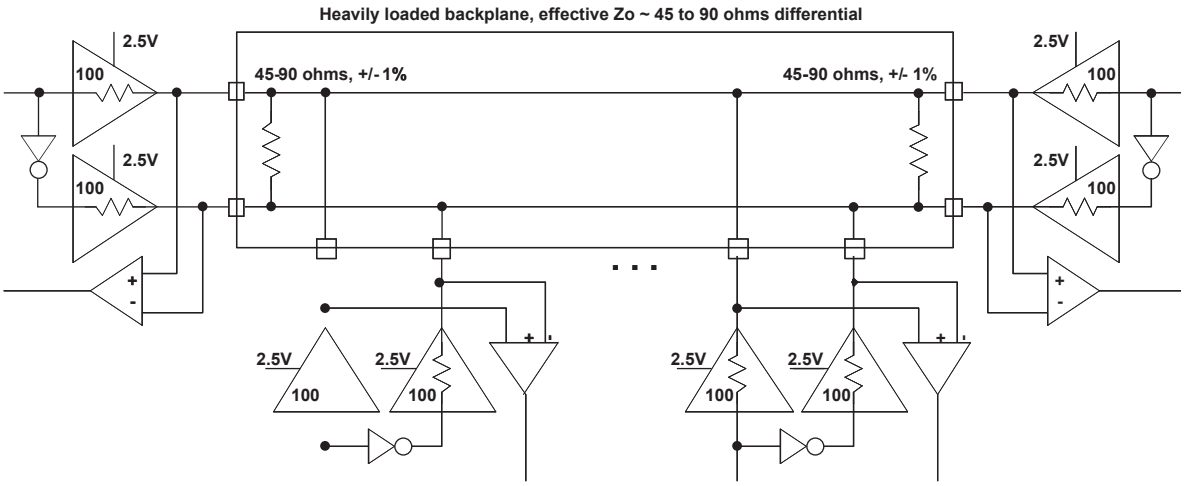


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	5.5	ns
32-bit decoder	6.9	ns
64-bit decoder	7.1	ns
4:1 MUX	4.3	ns
8:1 MUX	4.7	ns
16:1 MUX	5.0	ns
32:1 MUX	5.5	ns

Register-to-Register Performance[1]

Function	-5 Timing	Units
Basic Functions		
16 bit decoder	410	MHz
32 bit decoder	283	MHz
64 bit decoder	272	MHz
4:1 MUX	613	MHz
8:1 MUX	565	MHz
16:1 MUX	526	MHz
32:1 MUX	442	MHz
8-bit adder	363	MHz
16-bit adder	353	MHz
64-bit adder	196	MHz
16-bit counter	414	MHz
32-bit counter	317	MHz
64-bit counter	216	MHz
64-bit accumulator	178	MHz
Embedded Memory Functions		
256x36 Single Port RAM	280	MHz
512x18 True-Dual Port RAM	280	MHz
Distributed Memory Functions		
16x2 Single Port RAM	460	MHz
64x2 Single Port RAM	375	MHz
128x4 Single Port RAM	294	MHz
32x2 Pseudo-Dual Port RAM	392	MHz
64x4 Pseudo-Dual Port RAM	332	MHz
DSP Function[2]		
9x9 Pipelined Multiply/Accumulate	242	MHz
18x18 Pipelined Multiply/Accumulate	238	MHz
36x36 Pipelined Multiply	235	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Applies to LatticeECP devices only.

Timing v.G 0.30

LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

Figure 3-14. sysCONFIG Master Serial Port Timing

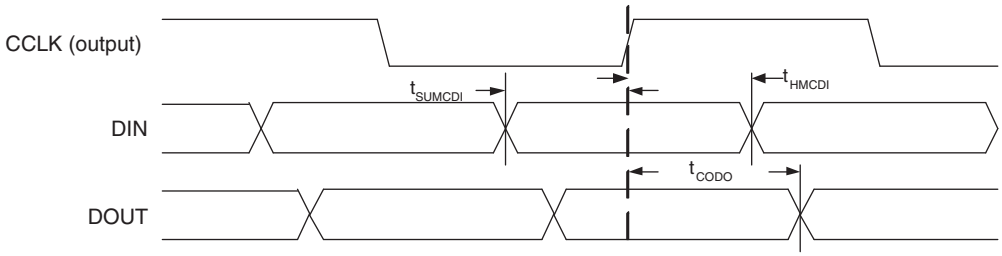


Figure 3-15. sysCONFIG Slave Serial Port Timing

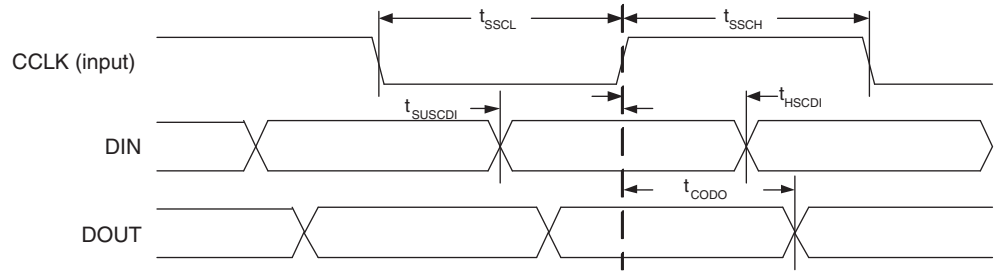
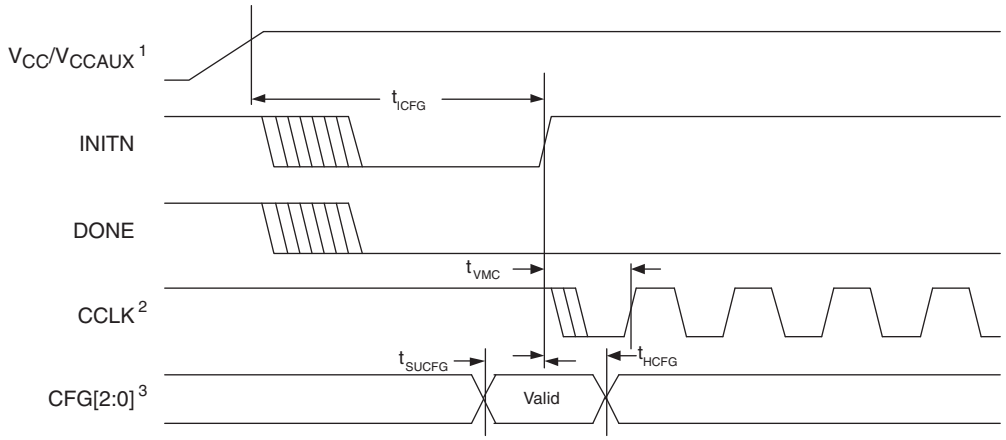


Figure 3-16. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX}, whichever is the last to reach its V_{MIN}.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
C3	PL3A	7	T		PL3A	7	T	
C2	PL3B	7	C		PL3B	7	C	
B1	PL4A	7	T		PL4A	7	T	
C1	PL4B	7	C		PL4B	7	C	
E3	PL5A	7	T		PL5A	7	T	
E4	PL5B	7	C		PL5B	7	C	
F4	PL6A	7	T	LDQS6	PL6A	7	T	LDQS6
F5	PL6B	7	C		PL6B	7	C	
G4	PL7A	7	T		PL7A	7	T	
G3	PL7B	7	C		PL7B	7	C	
D2	PL8A	7	T		PL8A	7	T	
D1	PL8B	7	C		PL8B	7	C	
E1	PL9A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL9B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	NC	-			PL11A	6	T	
H5	NC	-			PL11B	6	C	
F2	NC	-			PL12A	6	T	
F1	NC	-			PL12B	6	C	
H4	NC	-			PL13A	6	T	
H3	NC	-			PL13B	6	C	
G2	NC	-			PL14A	6	T	
-	-	-			GND6	6		
G1	NC	-			PL14B	6	C	
J4	NC	-			PL15A	6	T	LDQS15
J3	NC	-			PL15B	6	C	
J5	NC	-			PL16A	6	T	
K5	NC	-			PL16B	6	C	
H2	NC	-			PL17A	6	T	
H1	NC	-			PL17B	6	C	
J2	NC	-			PL18A	6	T	
-	-	-			GND6	6		
J1	NC	-			PL18B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		
L3	TMS	6			TMS	6		
L5	TDO	6			TDO	6		
L4	VCCJ	6			VCCJ	6		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N16	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
N15	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
M15	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
M16	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
L16	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
K16	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
J16	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
	-	-			GND3	3		
H16	NC	-			PR18B	3	C	
H15	NC	-			PR18A	3	T	
G16	NC	-			PR17B	3	C	
G15	NC	-			PR17A	3	T	
K12	NC	-			PR16B	3	C	
J12	NC	-			PR16A	3	T	
J14	NC	-			PR15B	3	C	
J15	NC	-			PR15A	3	T	RDQS15
F16	NC	-			PR14B	3	C	
-	-	-			GND3	3		
F15	NC	-			PR14A	3	T	
J13	NC	-			PR13B	3	C	
H13	NC	-			PR13A	3	T	
H14	NC	-			PR12B	3	C	
G14	NC	-			PR12A	3	T	
E16	NC	-			PR11B	3	C	
E15	NC	-			PR11A	3	T	
H12	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
GND	GND2	2			GND2			
G12	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
G13	PR8B	2	C		PR8B	2	C	
F13	PR8A	2	T		PR8A	2	T	
F12	PR7B	2	C		PR7B	2	C	
E13	PR7A	2	T		PR7A	2	T	
D16	PR6B	2	C		PR6B	2	C	
D15	PR6A	2	T	RDQS6	PR6A	2	T	RDQS6
F14	PR5B	2	C		PR5B	2	C	
E14	PR5A	2	T		PR5A	2	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
P14	PR35B	3	C		PR43B	3	C	
P15	PR35A	3	T		PR43A	3	T	
R15	PR34B	3	C		PR42B	3	C	
R16	PR34A	3	T		PR42A	3	T	
M13	PR33B	3	C		PR41B	3	C	
M14	PR33A	3	T	RDQS33	PR41A	3	T	RDQS41
P16	PR32B	3	C	RLM0_PLLC_FB_A	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		
N16	PR32A	3	T	RLM0_PLLT_FB_A	PR40A	3	T	RLM0_PLLT_FB_A
N15	PR31B	3	C	RLM0_PLLC_IN_A	PR39B	3	C	RLM0_PLLC_IN_A
M15	PR31A	3	T	RLM0_PLLT_IN_A	PR39A	3	T	RLM0_PLLT_IN_A
M16	PR30B	3	C	DI/CSSPIN	PR38B	3	C	DI/CSSPIN
L16	PR30A	3	T	DOUT/CSON	PR38A	3	T	DOUT/CSON
K16	PR29B	3	C	BUSY/SISPI	PR37B	3	C	BUSY/SISPI
J16	PR29A	3	T	D7/SPID0	PR37A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
GND	GND3	3			GND3	3		
H16	PR27B	3	C		PR31B	3	C	
-	-	-			GND3	3		
H15	PR27A	3	T		PR31A	3	T	
G16	PR26B	3	C		PR30B	3	C	
G15	PR26A	3	T		PR30A	3	T	
K12	PR25B	3	C		PR29B	3	C	
J12	PR25A	3	T		PR29A	3	T	
J14	PR24B	3	C		PR28B	3	C	
J15	PR24A	3	T	RDQS24	PR28A	3	T	RDQS28
F16	PR23B	3	C		PR27B	3	C	
GND	GND3	3			GND3	3		
F15	PR23A	3	T		PR27A	3	T	
J13	PR22B	3	C		PR26B	3	C	
H13	PR22A	3	T		PR26A	3	T	
H14	PR21B	3	C		PR25B	3	C	
G14	PR21A	3	T		PR25A	3	T	
E16	PR20B	3	C		PR24B	3	C	
E15	PR20A	3	T		PR24A	3	T	
H12	PR18B	2	C	PCLKC2_0	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND2	2		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G12	PR18A	2	T	PCLKT2_0	PR22A	2	T	PCLKT2_0
G13	PR17B	2	C		PR21B	2	C	
F13	PR17A	2	T		PR21A	2	T	
F12	PR16B	2	C		PR20B	2	C	
E13	PR16A	2	T		PR20A	2	T	
D16	PR15B	2	C		PR19B	2	C	
D15	PR15A	2	T		PR19A	2	T	RDQS19
F14	PR14B	2	C		PR18B	2	C	
GND	GND2	2			GND2	2		
E14	PR14A	2	T		PR18A	2	T	
C16	PR13B	2	C		PR17B	2	C	
B16	PR13A	2	T		PR17A	2	T	
C15	PR12B	2	C		PR16B	2	C	
C14	PR12A	2	T		PR16A	2	T	
GND	GND2	2			GND2	2		
-	-	-			GND2	2		
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
-	-	-			GND1	1		
B13	PT34B	1	C		PT34B	1	C	
C13	PT34A	1	T		PT34A	1	T	
C12	PT33B	1	C		PT33B	1	C	
GND	GND1	1			GND1	1		
D12	PT33A	1	T		PT33A	1	T	
A15	PT32B	1	C		PT32B	1	C	
B14	PT32A	1	T		PT32A	1	T	
D11	PT31B	1	C		PT31B	1	C	
C11	PT31A	1	T		PT31A	1	T	
E10	PT30B	1	C		PT30B	1	C	
E11	PT30A	1	T	TDQS30	PT30A	1	T	TDQS30
A14	PT29B	1	C		PT29B	1	C	
GND	GND1	1			GND1	1		
A13	PT29A	1	T		PT29A	1	T	
D10	PT28B	1	C		PT28B	1	C	
C10	PT28A	1	T		PT28A	1	T	
A12	PT27B	1	C	VREF2_1	PT27B	1	C	VREF2_1
B12	PT27A	1	T	VREF1_1	PT27A	1	T	VREF1_1
A11	PT26B	1	C		PT26B	1	C	
B11	PT26A	1	T		PT26A	1	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A5	PT13B	0	C		A5	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
A4	PT13A	0	T		A4	PT13A	0	T	
F9	PT12B	0	C		F9	PT12B	0	C	
B6	PT12A	0	T		B6	PT12A	0	T	
E9	PT11B	0	C		E9	PT11B	0	C	
C8	PT11A	0	T		C8	PT11A	0	T	
G8	PT10B	0	C		G8	PT10B	0	C	
B5	PT10A	0	T		B5	PT10A	0	T	
A3	PT9B	0	C		A3	PT9B	0	C	
GND	GND0	0			GND	GND0	0		
A2	PT9A	0	T		A2	PT9A	0	T	
F8	PT8B	0	C		F8	PT8B	0	C	
B4	PT8A	0	T		B4	PT8A	0	T	
E8	PT7B	0	C		E8	PT7B	0	C	
B3	PT7A	0	T		B3	PT7A	0	T	
D8	PT6B	0	C		D8	PT6B	0	C	
G7	PT6A	0	T	TDQS6	G7	PT6A	0	T	TDQS6
C4	PT5B	0	C		C4	PT5B	0	C	
C5	PT5A	0	T		C5	PT5A	0	T	
E7	PT4B	0	C		E7	PT4B	0	C	
D4	PT4A	0	T		D4	PT4A	0	T	
F7	PT3B	0	C		F7	PT3B	0	C	
D6	PT3A	0	T		D6	PT3A	0	T	
D7	PT2B	0	C		D7	PT2B	0	C	
E6	PT2A	0	T		E6	PT2A	0	T	
GND	GND0	0			GND	GND0	0		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K15	GND	-			K15	GND	-		
K16	GND	-			K16	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L15	GND	-			L15	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		

Conventional Packaging

LatticeEC Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208C	112	-3	PQFP	208	COM	1.5K
LFEC1E-4Q208C	112	-4	PQFP	208	COM	1.5K
LFEC1E-5Q208C	112	-5	PQFP	208	COM	1.5K
LFEC1E-3T144C	97	-3	TQFP	144	COM	1.5K
LFEC1E-4T144C	97	-4	TQFP	144	COM	1.5K
LFEC1E-5T144C	97	-5	TQFP	144	COM	1.5K
LFEC1E-3T100C	67	-3	TQFP	100	COM	1.5K
LFEC1E-4T100C	67	-4	TQFP	100	COM	1.5K
LFEC1E-5T100C	67	-5	TQFP	100	COM	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256C	160	-3	fpBGA	256	COM	3.1K
LFEC3E-4F256C	160	-4	fpBGA	256	COM	3.1K
LFEC3E-5F256C	160	-5	fpBGA	256	COM	3.1K
LFEC3E-3Q208C	145	-3	PQFP	208	COM	3.1K
LFEC3E-4Q208C	145	-4	PQFP	208	COM	3.1K
LFEC3E-5Q208C	145	-5	PQFP	208	COM	3.1K
LFEC3E-3T144C	97	-3	TQFP	144	COM	3.1K
LFEC3E-4T144C	97	-4	TQFP	144	COM	3.1K
LFEC3E-5T144C	97	-5	TQFP	144	COM	3.1K
LFEC3E-3T100C	67	-3	TQFP	100	COM	3.1K
LFEC3E-4T100C	67	-4	TQFP	100	COM	3.1K
LFEC3E-5T100C	67	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFEC6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFEC6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFEC6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFEC6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFEC6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFEC6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFEC6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFEC6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFEC6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFEC6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFEC6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFEC10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFEC10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFEC10E-3F256C	195	-3	fpBGA	256	COM	10.2K

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFEC10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFEC10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFEC10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFEC10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFEC15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFEC15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFEC15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFEC15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFEC15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFEC20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFEC20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFEC20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFEC20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFEC20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFEC33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFEC33E-5F672C	496	-5	fpBGA	672	COM	32.8K
LFEC33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFEC33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFEC33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFECP6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFECP6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFECP6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFECP6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFECP6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFECP6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFECP6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFECP10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFECP10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFECP10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFECP10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFECP10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFECP15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFECP15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFECP15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Date	Version	Section	Change Summary
September 2005	02.0	Architecture	sysIO section has been updated.
		DC & Switching Characteristics	Recommended Operating Conditions has been updated with V_{CCPLL}.
			DC Electrical Characteristics table has been updated
			Removed 5V Tolerant Input Buffer section.
			Register-to-Register performance table has been updated (rev. G 0.28).
			LatticeECP/EC External Switching Characteristics table has been updated (rev. G 0.28).
			LatticeECP/EC Internal Switching Characteristics table has been updated (rev. G 0.28).
			LatticeECP/EC Family Timing Adders have been updated (rev. G 0.28).
			sysCLOCK PLL timing table has been updated (rev. G 0.28)
			LatticeECP/EC sysCONFIG Port Timing specification table has been updated (rev. G 0.28).
			Master Clock table has been updated (rev. G 0.28).
			JTAG Port Timing specification table has been updated (rev. G 0.28).
		Pinout Information	Signal Description table has been updated with V_{CCPLL}.
November 2005	02.1	DC & Switching Characteristics	Pin-to-Pin Performance table has been updated (G 0.30) - 4:1MUX, 8:1MUX, 16:1MUX, 32:1MUX Register-to-Register Performance (G 0.30) - No timing number changes.
			External Switching Characteristics (G 0.30) - No timing number changes.
			Internal Switching Characteristics (G 0.30) -t_{SUP_DSP}, t_{HP_DSP}, t_{SUO_DSP}, t_{HO_DSP}, t_{COI_DSP}, t_{COD_DSP} numbers have been updated.
			Family Timing Adders (G 0.30) - No timing number changes.
			sysCLOCK PLL Timing (G 0.30) - No timing number changes.
			sysCONFIG Port Timing Specifications (G 0.30) - No timing number changes.
			Master Clock (G 0.30) - No timing number changes.
			JTAG Port Timing Specification (G 0.30) - No timing number changes.
		Ordering Information	Added 208-PQFP lead-free part numbers.
March 2006	02.2	DC & Switching Characteristics	Added footnote 3. to V_{CCAUX} in the Recommended Operating Conditions table.
January 2007	02.3	Architecture	EBR Asynchronous Reset section added.
February 2007	02.4	Architecture	Updated EBR Asynchronous Reset section.
			Updated Maximum Number of Elements in a Block table - MAC value for x9 changed to 2.
May 2007	02.5	Architecture	Updated text in Ripple Mode section.
November 2007	02.6	DC & Switching Characteristics	Added JTAG Port Waveforms diagram.
			Updated t_{RST} timing information in the sysCLOCK PLL Timing table.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
February 2008	02.7	DC & Switching Characteristics	Read/Write Mode (Normal) and Read/Write Mode with Input and Output Registers waveforms in the EBR Memory Timing Diagrams section have been updated.
September 2012	02.8	All	Updated document with new corporate logo.