Lattice Semiconductor Corporation - LFECP20E-3FN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

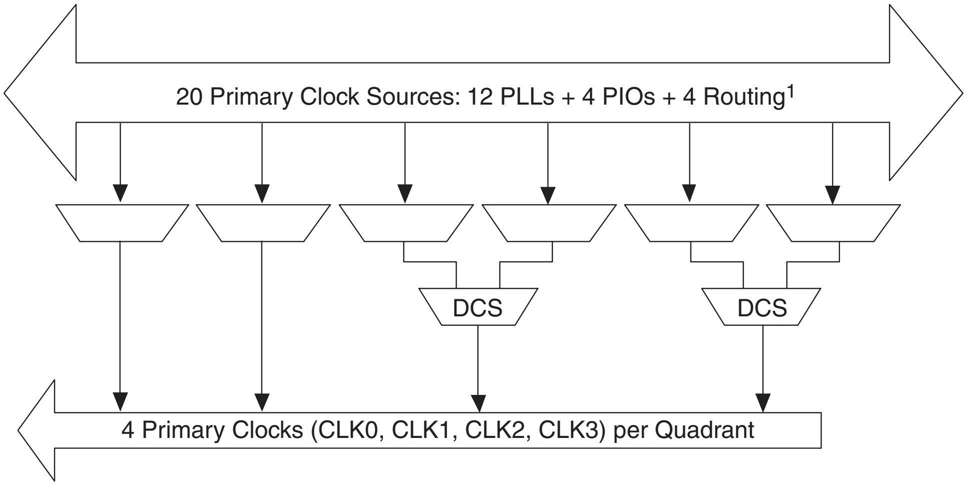
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	19700
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp20e-3fn484c

Figure 2-8. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-9. Per Quadrant Secondary Clock Selection

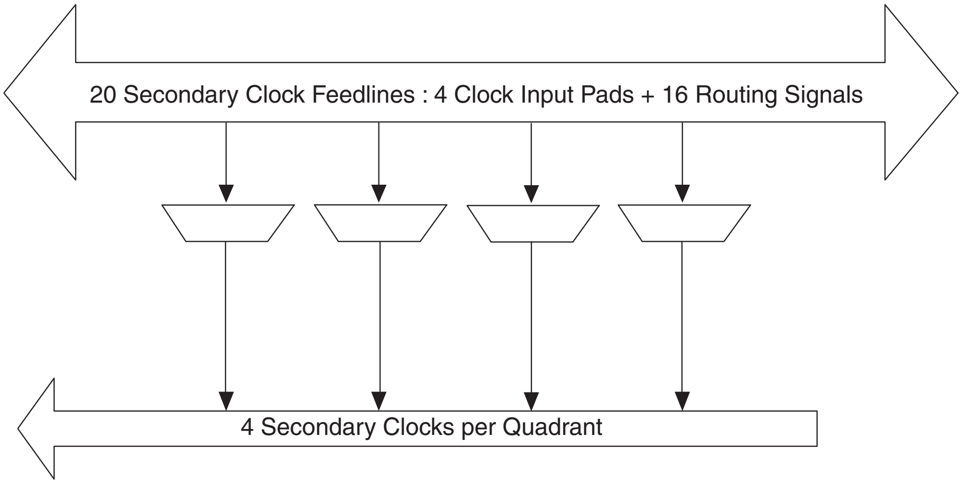
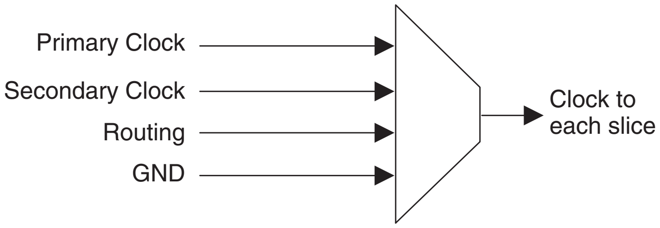


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

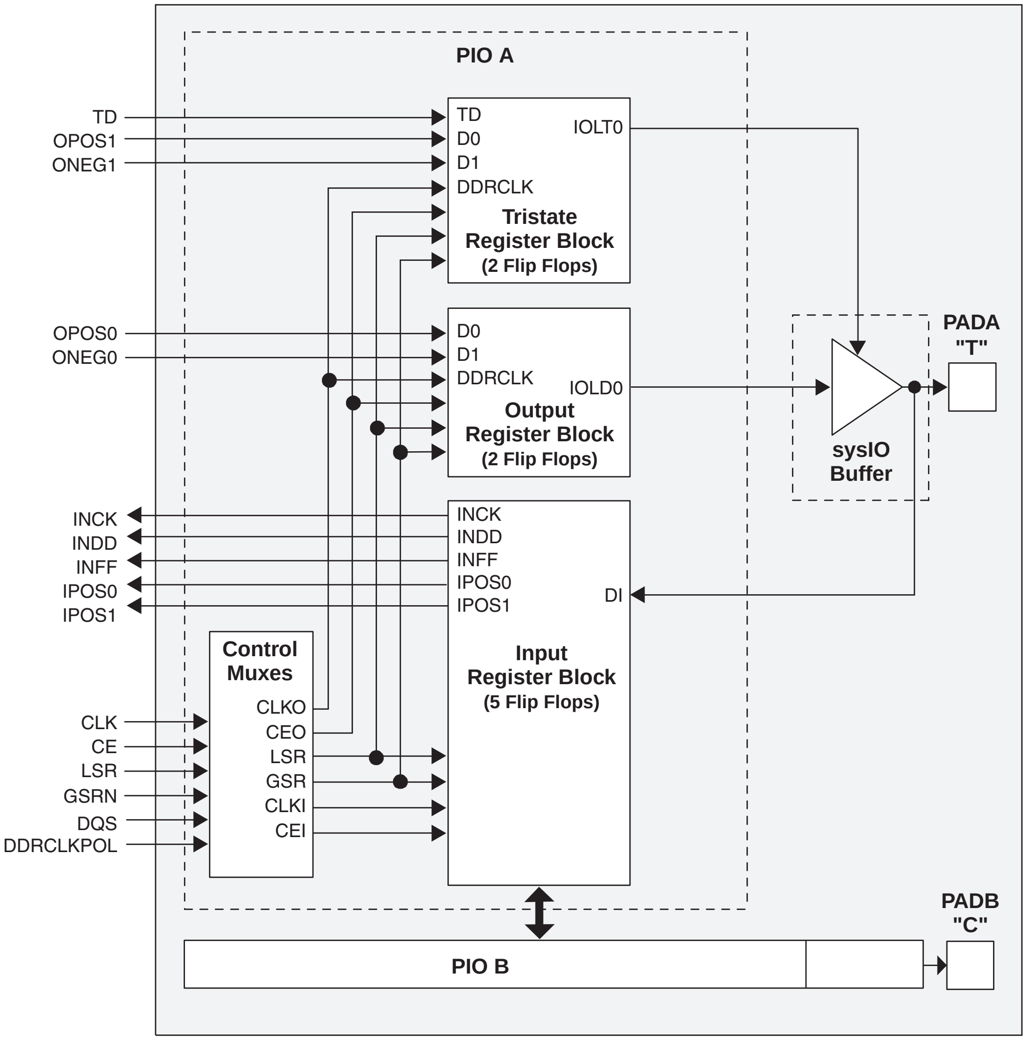
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

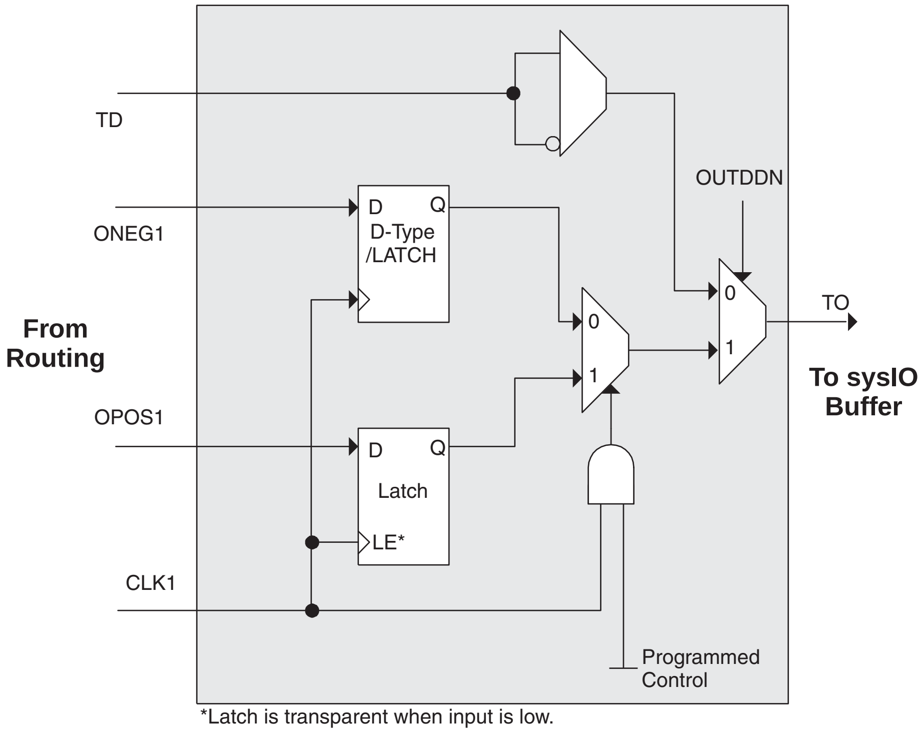
Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Figure 2-31. Tristate Register Block



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-32. DQS Local Bus.

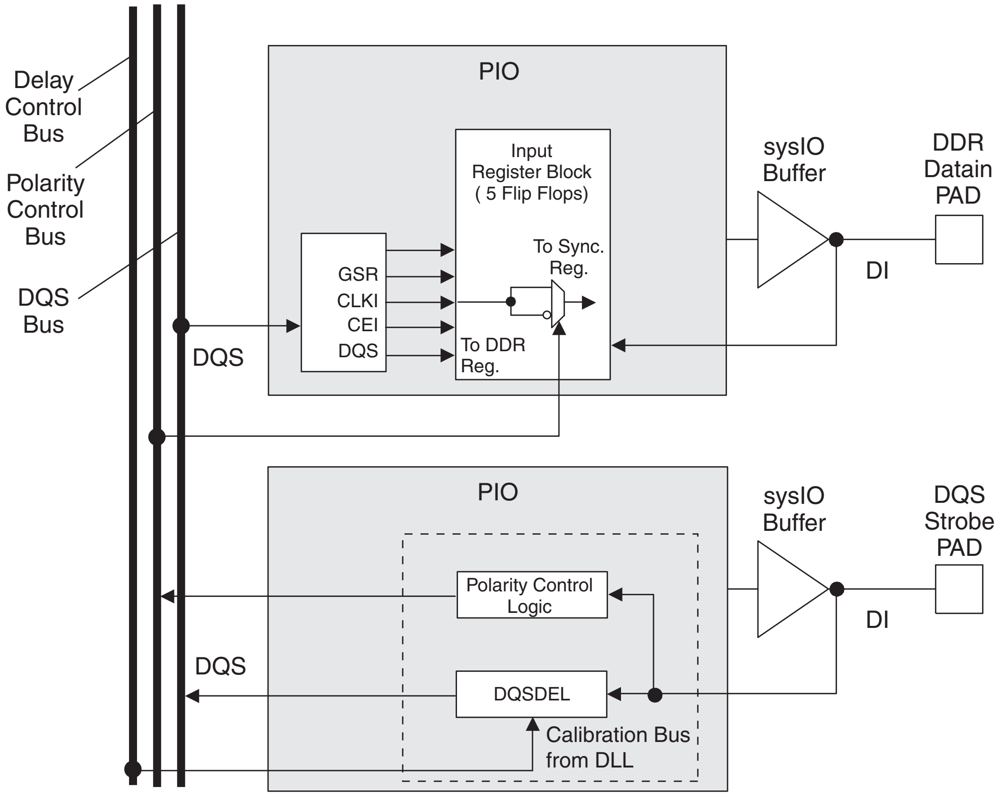
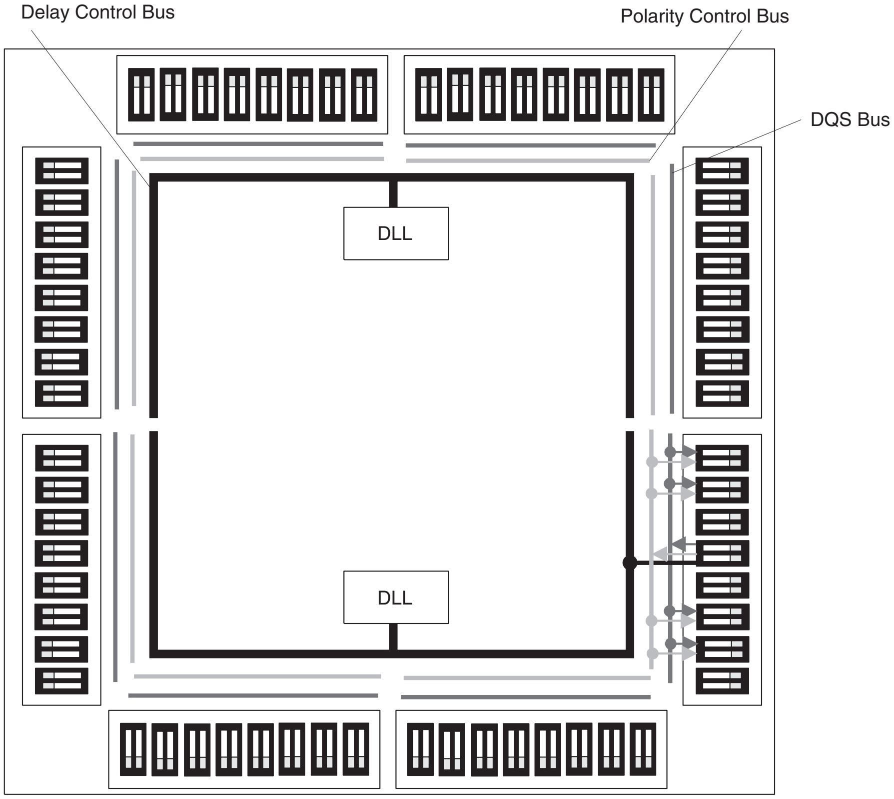


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution



DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCIO} - 0.2V)	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	(V_{CCIO} - 0.2V) ð V_{IH} ð 3.6V	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCIO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO}.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables: T_J °C.

Table 3-5. Delay Derating Table for Internal Blocks

T_J °C Commercial	**T_J °C Industrial**	**Power Supply Voltage**		
		1.14V	**1.2V**	**1.26V**
—	-40	0.82	0.77	0.71
—	-25	0.82	0.76	0.71
0	20	0.89	0.83	0.78
25	45	0.93	0.87	0.81
85	105	1.00	0.94	0.89

LatticeECP/EC External Switching Characteristics (Continued)

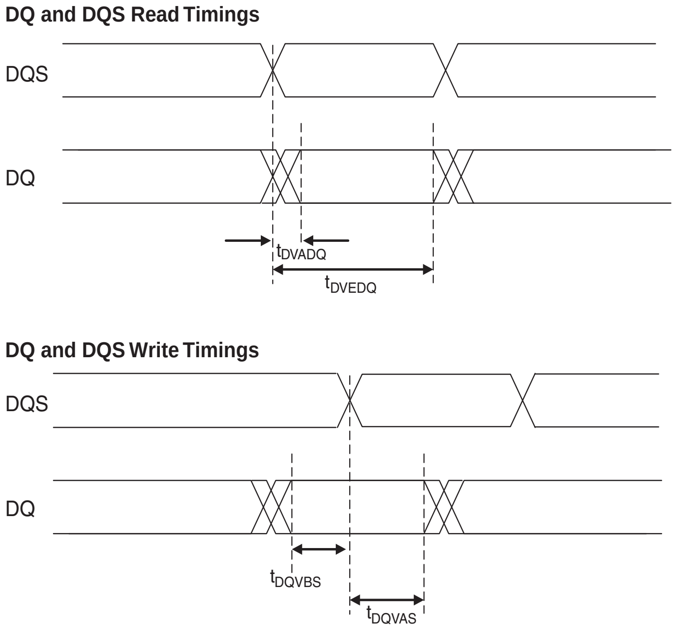
Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	200	95	166	95	133	MHz
Primary and Secondary Clock[6]									
f_{MAX_PRI}[2]	Frequency for Primary Clock Tree	All	—	420	—	378	—	340	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	All	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA. Loading of 0 pF.
2. Using LVDS I/O standard.
3. DDR timing numbers based on SSTL I/O.
4. DDR specifications are characterized but not tested.
5. UI is average bit period.
6. Based on a single primary clock.
7. These timing numbers were generated using ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.G 0.30

Figure 3-5. DDR Timings



LatticeECP/EC Internal Switching Characteristics (Continued)

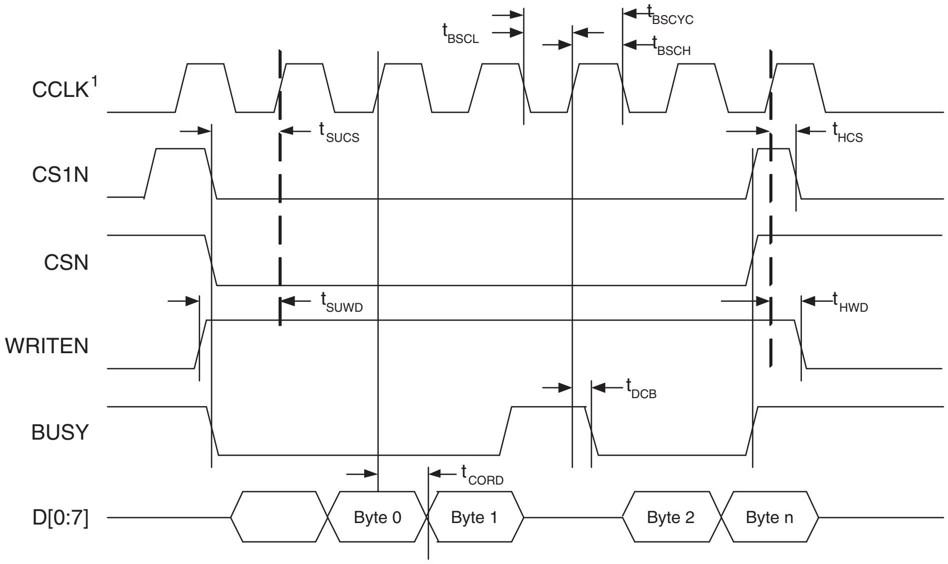
Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.18	—	0.21	—	0.25	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.14	—	-0.17	—	-0.20	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.47	—	1.76	—	2.05	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing[2, 3]								
t_{SUI_DSP}	Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HI_DSP}	Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.31	—	3.98	—	4.64	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{SUO_DSP}[4]	Output Register Setup Time	5.54	—	6.64	—	7.75	—	ns
t_{HO_DSP}[4]	Output Register Hold Time	0.71	—	0.86	—	1.00	—	ns
t_{COI_DSP}[4]	Input Register Clock to Output Time	—	7.50	—	9.00	—	10.50	ns
t_{COP_DSP}[4]	Pipeline Register Clock to Output Time	—	4.66	—	5.60	—	6.53	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	1.47	—	1.77	—	2.06	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.38	—	-0.30	—	-0.23	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.71	—	0.86	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.
4. These parameters include the Adder Subtractor block in the path.

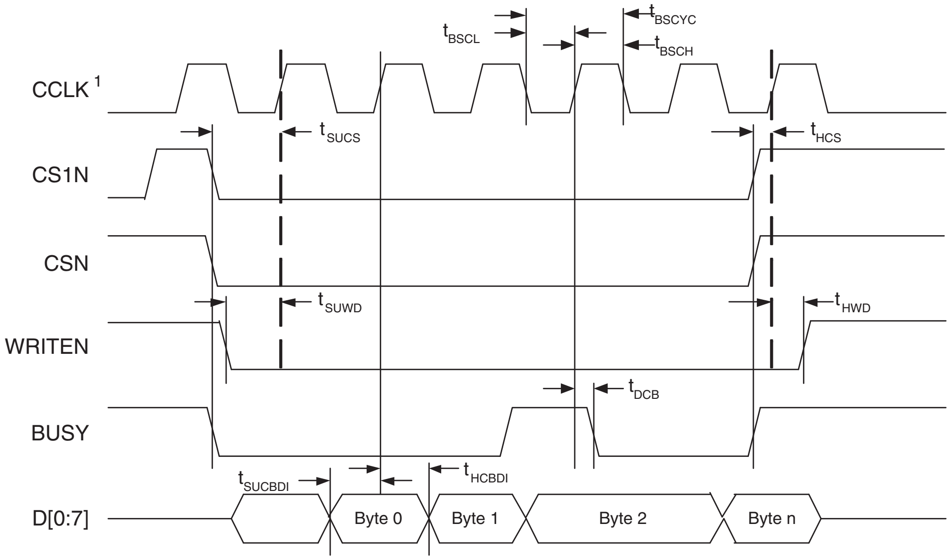
Timing v.G 0.30

Figure 3-12. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-13. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Pin Information Summary (Cont.)

		LFECP/EC15		LFECP20/EC20		LFECP/EC33	
Pin Type		**256-fpBGA**	**484-fpBGA**	**484-fpBGA**	**672-fpBGA**	**484-fpBGA**	**672-fpBGA**
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V_{CC}		10	20	20	32	16	28
V_{CCAUX}		2	12	12	20	12	20
V_{CCPLL}		0	0	0	0	4	4
V_{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V_{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U9	PB20B	5	C		U9	PB20B	5	C	
Y8	PB21A	5	T		Y8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
Y9	PB21B	5	C		Y9	PB21B	5	C	
V9	PB22A	5	T	BDQS22	V9	PB22A	5	T	BDQS22
T9	PB22B	5	C		T9	PB22B	5	C	
W10	PB23A	5	T		W10	PB23A	5	T	
U10	PB23B	5	C		U10	PB23B	5	C	
V10	PB24A	5	T		V10	PB24A	5	T	
T10	PB24B	5	C		T10	PB24B	5	C	
AA6	PB25A	5	T		AA6	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AB5	PB25B	5	C		AB5	PB25B	5	C	
AA8	PB26A	5	T		AA8	PB26A	5	T	
AA7	PB26B	5	C		AA7	PB26B	5	C	
AB6	PB27A	5	T		AB6	PB27A	5	T	
AB7	PB27B	5	C		AB7	PB27B	5	C	
Y10	PB28A	5	T		Y10	PB28A	5	T	
W11	PB28B	5	C		W11	PB28B	5	C	
AB8	PB29A	5	T		AB8	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AB9	PB29B	5	C		AB9	PB29B	5	C	
AA10	PB30A	5	T	BDQS30	AA10	PB30A	5	T	BDQS30
AA9	PB30B	5	C		AA9	PB30B	5	C	
Y11	PB31A	5	T		Y11	PB31A	5	T	
AA11	PB31B	5	C		AA11	PB31B	5	C	
V11	PB32A	5	T	VREF2_5	V11	PB32A	5	T	VREF2_5
V12	PB32B	5	C	VREF1_5	V12	PB32B	5	C	VREF1_5
AB10	PB33A	5	T	PCLKT5_0	AB10	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AB11	PB33B	5	C	PCLKC5_0	AB11	PB33B	5	C	PCLKC5_0
Y12	PB34A	4	T	WRITEN	Y12	PB34A	4	T	WRITEN
U11	PB34B	4	C	CS1N	U11	PB34B	4	C	CS1N
W12	PB35A	4	T	VREF1_4	W12	PB35A	4	T	VREF1_4
U12	PB35B	4	C	CSN	U12	PB35B	4	C	CSN
W13	PB36A	4	T	VREF2_4	W13	PB36A	4	T	VREF2_4
U13	PB36B	4	C	D0/SPID7	U13	PB36B	4	C	D0/SPID7
AA12	PB37A	4	T	D2/SPID5	AA12	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AB12	PB37B	4	C	D1/SPID6	AB12	PB37B	4	C	D1/SPID6
T13	PB38A	4	T	BDQS38	T13	PB38A	4	T	BDQS38
V13	PB38B	4	C	D3/SPID4	V13	PB38B	4	C	D3/SPID4
W14	PB39A	4	T		W14	PB39A	4	T	
U14	PB39B	4	C	D4/SPID3	U14	PB39B	4	C	D4/SPID3

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA

LFEC20/LFECP20					LFECP/EC33				
Ball Number	**Ball Function**	**Bank**	**LVDS**	**Dual Function**	**Ball Number**	**Ball Function**	**Bank**	**LVDS**	**Dual Function**
GND	GND7	7			GND	GND7	7		
E3	PL2A	7	T	VREF2_7	E3	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
E5	NC	-			E5	PL6A	7	T	LDQS6
D5	NC	-			D5	PL6B	7	C	
F4	NC	-			F4	PL7A	7	T	
F5	NC	-			F5	PL7B	7	C	
C3	NC	-			C3	PL8A	7	T	
D3	NC	-			D3	PL8B	7	C	
C2	NC	-			C2	PL9A	7	T	
-	-	-			GND	GND7	7		
B2	NC	-			B2	PL9B	7	C	
B1	PL3A	7	T		B1	PL10A	7	T	
C1	PL3B	7	C		C1	PL10B	7	C	
F3	PL4A	7	T		F3	PL11A	7	T	
G3	PL4B	7	C		G3	PL11B	7	C	
D2	PL5A	7	T		D2	PL12A	7	T	
E2	PL5B	7	C		E2	PL12B	7	C	
-	-	-			GND	GND7	7		
D1	PL6A	7	T	LDQS6	D1	PL14A	7	T	LDQS14
E1	PL6B	7	C		E1	PL14B	7	C	
F2	PL7A	7	T		F2	PL15A	7	T	
G2	PL7B	7	C		G2	PL15B	7	C	
F6	PL8A	7	T	LUM0_PLLT_IN_A	F6	PL16A	7	T	LUM0_PLLT_IN_A
G6	PL8B	7	C	LUM0_PLLC_IN_A	G6	PL16B	7	C	LUM0_PLLC_IN_A
H4	PL9A	7	T	LUM0_PLLT_FB_A	H4	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
G4	PL9B	7	C	LUM0_PLLC_FB_A	G4	PL17B	7	C	LUM0_PLLC_FB_A
H6	NC	-			H6	PL19A	7	T	
J7	NC	-			J7	PL19B	7	C	
G5	NC	-			G5	PL20A	7	T	
H5	NC	-			H5	PL20B	7	C	
H3	NC	-			H3	PL21A	7	T	
J3	NC	-			J3	PL21B	7	C	
H2	NC	-			H2	PL22A	7	T	
-	-	-			GND	GND7	7		
J2	NC	-			J2	PL22B	7	C	
J4	PL11A	7	T		J4	PL23A	7	T	LDQS23
J5	PL11B	7	C		J5	PL23B	7	C	
K4	PL12A	7	T		K4	PL24A	7	T	
K5	PL12B	7	C		K5	PL24B	7	C	
J6	PL13A	7	T		J6	PL25A	7	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A21	PT51A	1	T		A21	PT51A	1	T	
E17	PT50B	1	C		E17	PT50B	1	C	
B17	PT50A	1	T		B17	PT50A	1	T	
C17	PT49B	1	C		C17	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
D17	PT49A	1	T		D17	PT49A	1	T	
F17	PT48B	1	C		F17	PT48B	1	C	
E20	PT48A	1	T		E20	PT48A	1	T	
G17	PT47B	1	C		G17	PT47B	1	C	
B20	PT47A	1	T		B20	PT47A	1	T	
E16	PT46B	1	C		E16	PT46B	1	C	
A20	PT46A	1	T	TDQS46	A20	PT46A	1	T	TDQS46
A19	PT45B	1	C		A19	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
B19	PT45A	1	T		B19	PT45A	1	T	
D16	PT44B	1	C		D16	PT44B	1	C	
C16	PT44A	1	T		C16	PT44A	1	T	
F16	PT43B	1	C		F16	PT43B	1	C	
A18	PT43A	1	T		A18	PT43A	1	T	
G16	PT42B	1	C		G16	PT42B	1	C	
B18	PT42A	1	T		B18	PT42A	1	T	
A17	PT41B	1	C		A17	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
A16	PT41A	1	T		A16	PT41A	1	T	
D15	PT40B	1	C		D15	PT40B	1	C	
B16	PT40A	1	T		B16	PT40A	1	T	
E15	PT39B	1	C		E15	PT39B	1	C	
C15	PT39A	1	T		C15	PT39A	1	T	
F15	PT38B	1	C		F15	PT38B	1	C	
G15	PT38A	1	T	TDQS38	G15	PT38A	1	T	TDQS38
B15	PT37B	1	C		B15	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
A15	PT37A	1	T		A15	PT37A	1	T	
E14	PT36B	1	C		E14	PT36B	1	C	
G14	PT36A	1	T		G14	PT36A	1	T	
D14	PT35B	1	C	VREF2_1	D14	PT35B	1	C	VREF2_1
E13	PT35A	1	T	VREF1_1	E13	PT35A	1	T	VREF1_1
F14	PT34B	1	C		F14	PT34B	1	C	
C14	PT34A	1	T		C14	PT34A	1	T	
B14	PT33B	0	C	PCLKC0_0	B14	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A14	PT33A	0	T	PCLKT0_0	A14	PT33A	0	T	PCLKT0_0

LatticeECP/EC Family Data Sheet
Ordering Information

September 2012 **Data Sheet**

Part Number Description

LFXXX XX X – X XXXX X

Device Family
Lattice EC (FPGA)
Lattice ECP (EC FPGA + DSP Blocks)

Logic Capacity
1* = 1.5K LUTs
3* = 3K LUTs
6 = 6K LUTs
10 = 10K LUTs
15 = 15K LUTs
20 = 20K LUTs
33 = 33K LUTs

Supply Voltage
E = 1.2V

Grade
C = Commercial
I = Industrial

Package
T100 = 100-pin TQFP*
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA

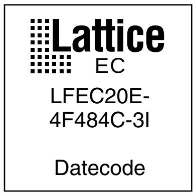
TN100 = 100-pin Lead-free TQFP*
TN144 = 144-pin Lead-free TQFP
QN208 = 208-pin Lead-free PQFP
FN256 = 256-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA
FN672 = 672-ball Lead-free fpBGA

Speed
3 = Slowest
4
5 = Fastest

*Not available in the LatticeECP Family.

Ordering Information

Note:þLatticeECP/EC devices are dual marked. For example, the commercial speed grade LFEC20E-4F484C is also marked with industrial grade -3I (LFEC20E-3F484I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFEC15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFEC15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFEC15E-4F256I	195	-4	fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFEC20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFEC20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFEC20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC33E-3F672I	496	-3	fpBGA	672	IND	32.8
LFEC33E-4F672I	496	-4	fpBGA	672	IND	32.8
LFEC33E-3F484I	360	-3	fpBGA	484	IND	32.8
LFEC33E-4F484I	360	-4	fpBGA	484	IND	32.8

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFECP6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFECP6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFECP6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFECP6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFECP6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFECP6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFECP6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFECP10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFECP10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFECP10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFECP10E-3Q208I	147	-3	PQFP	208	IND	10.2K
LFECP10E-4Q208I	147	-4	PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP15E-3F484I	352	-3	fpBGA	484	IND	15.3K
LFECP15E-4F484I	352	-4	fpBGA	484	IND	15.3K
LFECP15E-3F256I	195	-3	fpBGA	256	IND	15.3K
LFECP15E-4F256I	195	-4	fpBGA	256	IND	15.3K

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFEC10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFEC10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K