Lattice Semiconductor Corporation - LFECP20E-3FN484I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	19700
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp20e-3fn484i

Figure 2-4. Slice Diagram

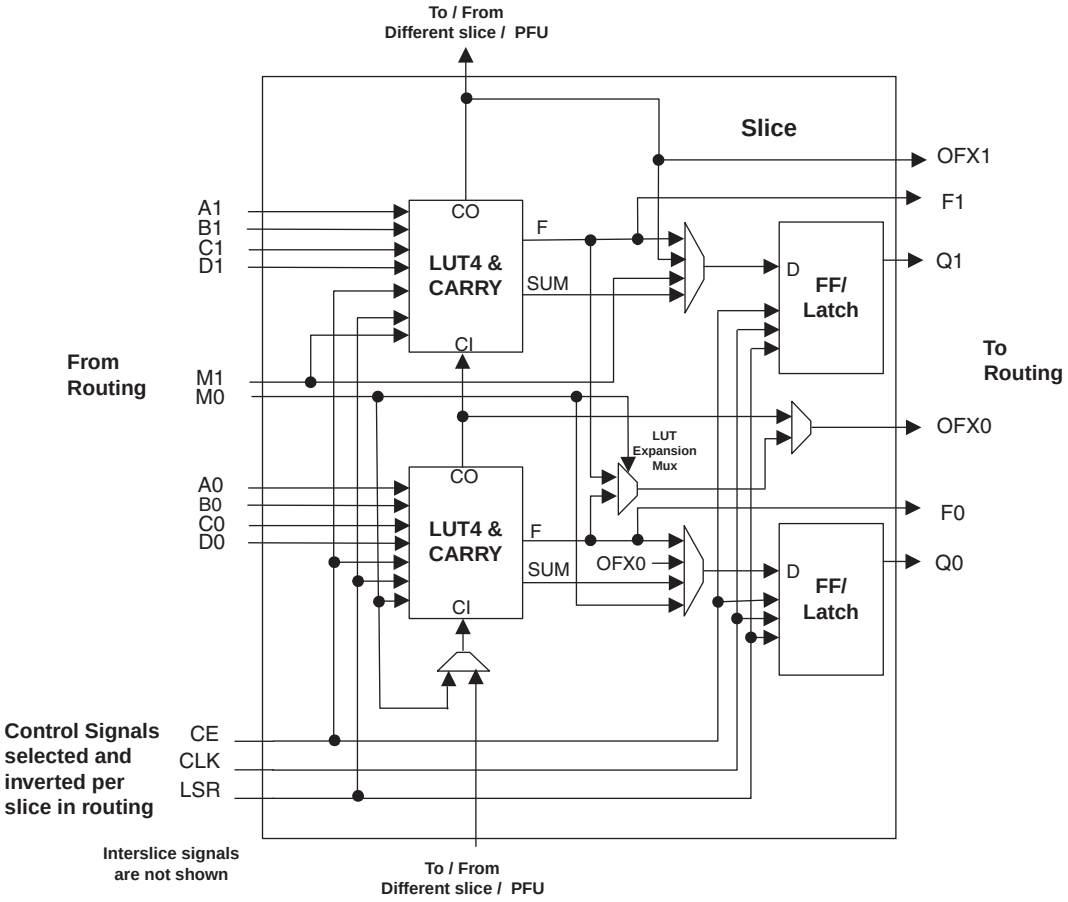
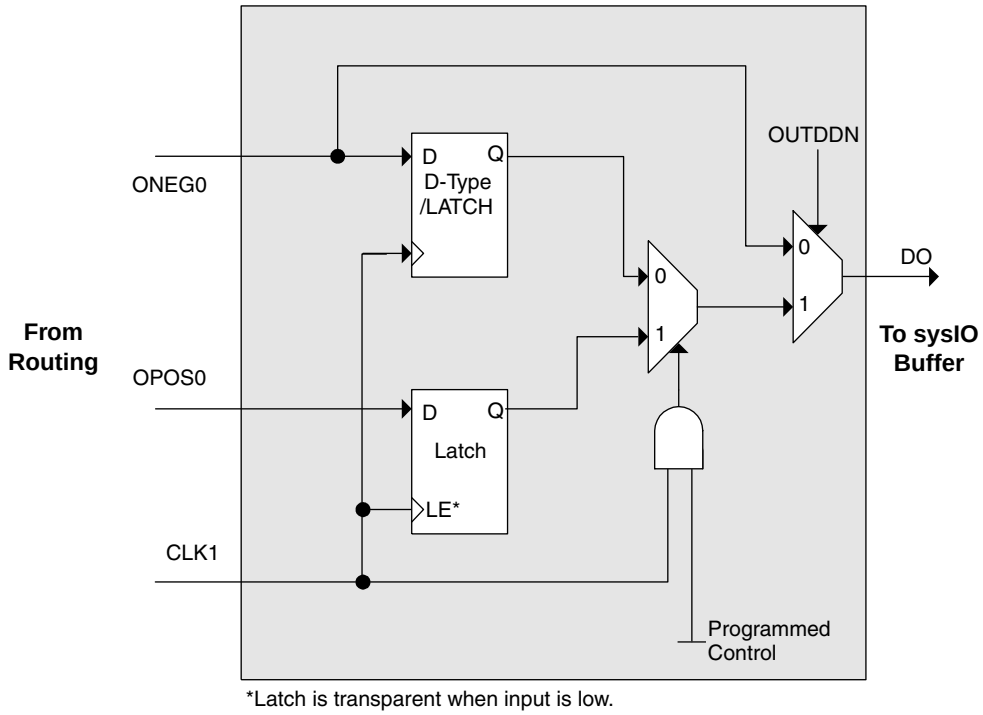


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

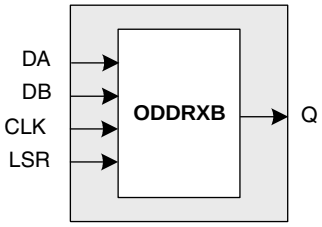
1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Figure 2-29. Output Register Block



*Latch is transparent when input is low.

Figure 2-30. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

LatticeECP/EC Family Data Sheet DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

Dedicated Input Voltage Applied[4] . . . . . -0.5 to 4.25V

I/O Tristate Voltage Applied [4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temp. (Tj) . . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[3]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage for ECP/EC33	1.14	1.26	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.140	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.140	3.465	V
t_{JCOM}	Junction Commercial Operation	0	85	°C
t_{JIND}	Junction Industrial Operation	-40	100	°C

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCAUX} ramp rate must not exceed 3mV/µs for commercial and 0.6 mV/µs for industrial device operations during power up when transitioning between 0.8V and 1.8V.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Top and Bottom General Purpose sysI/Os (Banks 0, 1, 4 and 5), JTAG and Dedicated sysCONFIG Pins						
I_{DK_TB}	Input or I/O Leakage Current	0 ð V_{IN} ð V_{IH} (MAX.)	—	—	+/-1000	µA
Left and Right General Purpose sysI/Os (Banks 2, 3, 6 and 7)						
I_{DK_LR}	Input or I/O Leakage Current	V_{IN} ð V_{CCIO}	—	—	+/-1000	µA
		V_{IN} > V_{CCIO}	—	35	—	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. 0 ð V_{CC} ð V_{CC} (MAX), 0 ð V_{CCIO} ð V_{CCIO} (MAX) or 0 ð V_{CCAUX} ð V_{CCAUX} (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

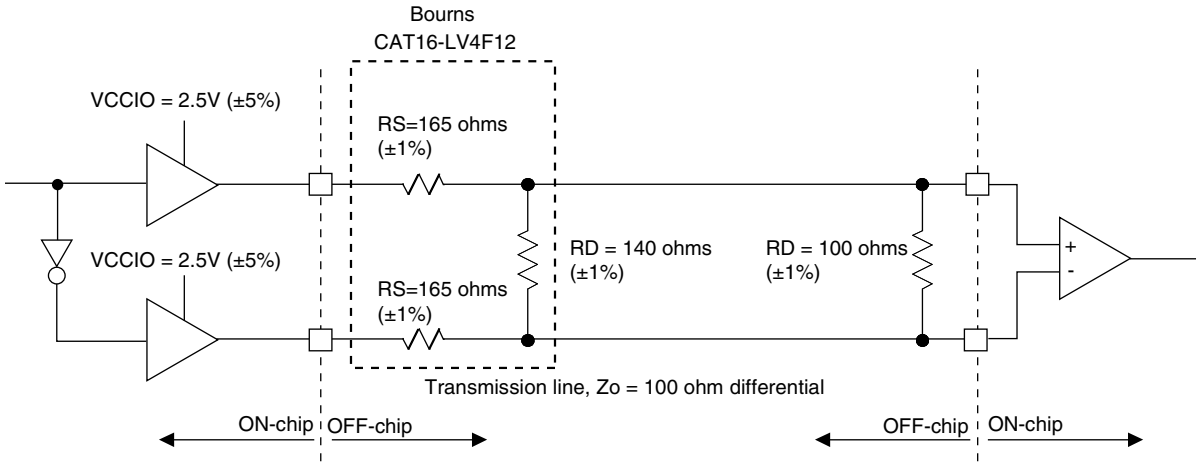


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.42	V
V_{OL}	Output low voltage	1.08	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	¾

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}[7]	Clock to Output - PIO Output Register	LFEC1	—	5.09	—	6.11	—	7.13	ns
		LFEC3	—	5.71	—	6.85	—	7.99	ns
		LFEC6	—	5.60	—	6.72	—	7.84	ns
		LFEC10	—	5.47	—	6.57	—	7.66	ns
		LFEC15	—	5.67	—	6.81	—	7.94	ns
		LFEC20	—	5.89	—	7.07	—	8.25	ns
		LFEC33	—	6.19	—	7.42	—	8.66	ns
t_{SU}[7]	Clock to Data Setup - PIO Input Register	LFEC1	-0.08	—	-0.10	—	-0.12	—	ns
		LFEC3	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC6	-0.63	—	-0.76	—	-0.89	—	ns
		LFEC10	-0.43	—	-0.52	—	-0.61	—	ns
		LFEC15	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC20	-0.88	—	-1.06	—	-1.24	—	ns
		LFEC33	-1.12	—	-1.34	—	-1.56	—	ns
t_{H}[7]	Clock to Data Hold - PIO Input Register	LFEC1	2.19	—	2.62	—	3.06	—	ns
		LFEC3	2.80	—	3.36	—	3.92	—	ns
		LFEC6	2.69	—	3.23	—	3.77	—	ns
		LFEC10	2.56	—	3.08	—	3.59	—	ns
		LFEC15	2.76	—	3.32	—	3.87	—	ns
		LFEC20	2.99	—	3.58	—	4.18	—	ns
		LFEC33	3.28	—	3.93	—	4.59	—	ns
t_{SU_DEL}[7]	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC1	3.36	—	4.03	—	4.70	—	ns
		LFEC3	2.74	—	3.29	—	3.84	—	ns
		LFEC6	2.81	—	3.37	—	3.93	—	ns
		LFEC10	3.01	—	3.61	—	4.21	—	ns
		LFEC15	2.74	—	3.29	—	3.83	—	ns
		LFEC20	2.56	—	3.07	—	3.58	—	ns
		LFEC33	2.32	—	2.79	—	3.25	—	ns
t_{H_DEL}[7]	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC1	-1.31	—	-1.57	—	-1.83	—	ns
		LFEC3	-0.70	—	-0.83	—	-0.97	—	ns
		LFEC6	-0.80	—	-0.96	—	-1.12	—	ns
		LFEC10	-0.93	—	-1.12	—	-1.30	—	ns
		LFEC15	-0.73	—	-0.88	—	-1.02	—	ns
		LFEC20	-0.51	—	-0.61	—	-0.71	—	ns
		LFEC33	-0.22	—	-0.26	—	-0.30	—	ns
f_{MAX_IO}[2]	Clock Frequency of I/O and PFU Register	All	—	420	—	378	—	340	Mhz
DDR I/O Pin Parameters[3, 4, 5]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

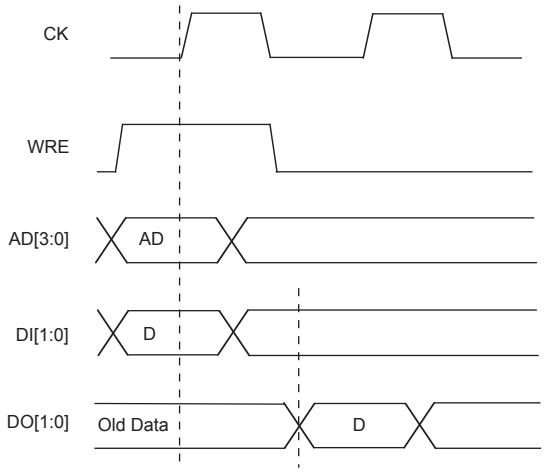
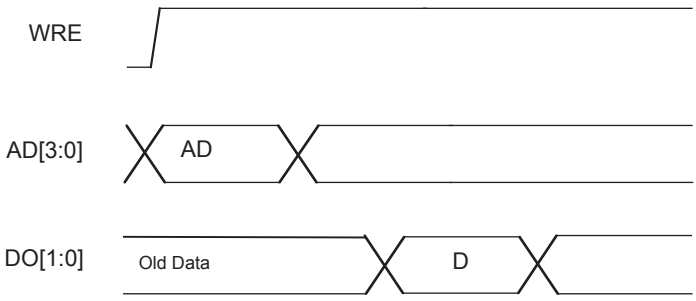


Figure 3-7. Slice Single /Dual Port Read Cycle Timing

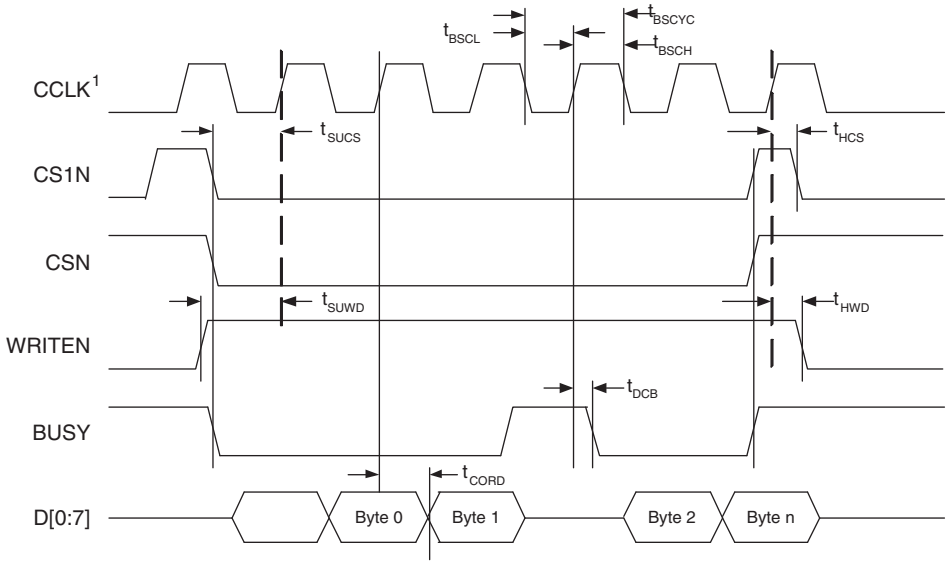


LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

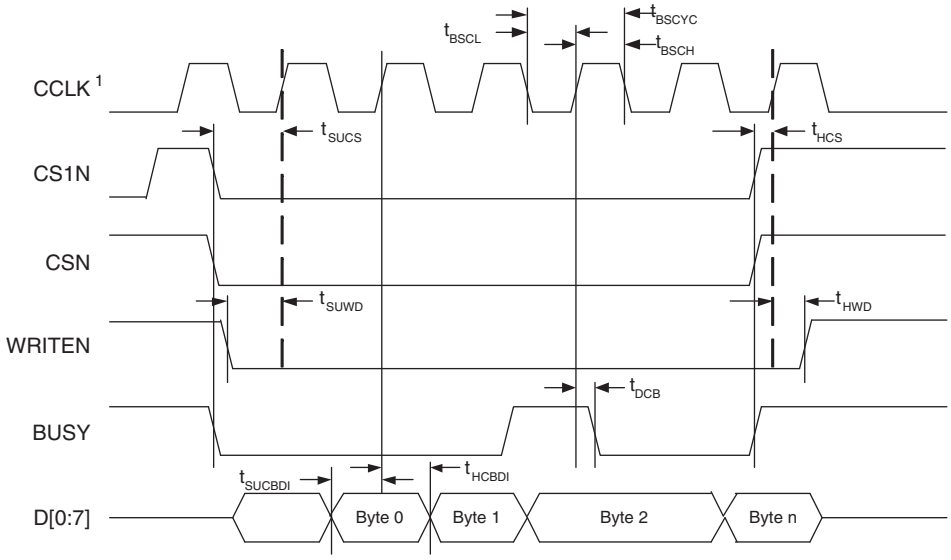
Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from tICFG to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

Figure 3-12. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-13. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN
87	PB10B	4	C	CS1N	PB18B	4	C	CS1N
88	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
89	PB11B	4	C	CSN	PB19B	4	C	CSN
90	PB12A	4	T	VREF2_4	PB20A	4	T	VREF2_4
91	PB12B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
92	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
95	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
96	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
97	PB15A	4	T		PB23A	4	T	
98	PB15B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
99	PB16A	4	T		PB24A	4	T	
100	PB16B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
101	PB17A	4	T		PB25A	4	T	
102	PB17B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
103	NC	-			NC	-		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR14B	3	C	VREF2_3	PR18B	3	C	VREF2_3
108	PR14A	3	T	VREF1_3	PR18A	3	T	VREF1_3
109	PR13B	3	C		PR17B	3	C	
110	PR13A	3	T		PR17A	3	T	
111	PR12B	3	C		PR16B	3	C	
112	PR12A	3	T		PR16A	3	T	
113	PR11B	3	C		PR15B	3	C	
114	PR11A	3	T	RDQS11	PR15A	3	T	RDQS15
115	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
118	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
119	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
122	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
123	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
124	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
K2	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
K1	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
L2	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
L1	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
M2	PL13A	6	T		PL22A	6	T	
M1	PL13B	6	C		PL22B	6	C	
N1	PL14A	6	T		PL23A	6	T	
GND	GND6	6			GND6	6		
N2	PL14B	6	C		PL23B	6	C	
M4	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
M3	PL15B	6	C		PL24B	6	C	
P1	PL16A	6	T		PL25A	6	T	
R1	PL16B	6	C		PL25B	6	C	
P2	PL17A	6	T		PL26A	6	T	
P3	PL17B	6	C		PL26B	6	C	
N3	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
N4	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
P4	PB2A	5	T		PB2A	5	T	
N5	PB2B	5	C		PB2B	5	C	
P5	PB3A	5	T		PB3A	5	T	
P6	PB3B	5	C		PB3B	5	C	
R4	PB4A	5	T		PB4A	5	T	
R3	PB4B	5	C		PB4B	5	C	
T2	PB5A	5	T		PB5A	5	T	
T3	PB5B	5	C		PB5B	5	C	
R5	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
R6	PB6B	5	C		PB6B	5	C	
T4	PB7A	5	T		PB7A	5	T	
T5	PB7B	5	C		PB7B	5	C	
N6	PB8A	5	T		PB8A	5	T	
M6	PB8B	5	C		PB8B	5	C	
T6	PB9A	5	T		PB9A	5	T	
GND	GND5	5			GND5	5		
T7	PB9B	5	C		PB9B	5	C	
P7	PB10A	5	T		PB10A	5	T	
N7	PB10B	5	C		PB10B	5	C	
R7	PB11A	5	T		PB11A	5	T	
R8	PB11B	5	C		PB11B	5	C	
M7	PB12A	5	T		PB12A	5	T	
M8	PB12B	5	C		PB12B	5	C	
T8	PB13A	5	T		PB13A	5	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND5	5			GND5	5		
T9	PB13B	5	C		PB13B	5	C	
P8	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
N8	PB14B	5	C		PB14B	5	C	
R9	PB15A	5	T		PB15A	5	T	
R10	PB15B	5	C		PB15B	5	C	
P9	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5
N9	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
T10	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
T12	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
T13	PB18B	4	C	CS1N	PB18B	4	C	CS1N
P10	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
N10	PB19B	4	C	CSN	PB19B	4	C	CSN
T14	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
T15	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
M10	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
R11	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
P11	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
R13	PB23A	4	T		PB23A	4	T	
R14	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
P12	PB24A	4	T		PB24A	4	T	
P13	PB24B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
N11	PB25A	4	T		PB25A	4	T	
-	-	-			GND4	4		
N12	PB25B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
R12	NC	-			PB26A	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR18B	3	C	VREF2_3	PR27B	3	C	VREF2_3
N14	PR18A	3	T	VREF1_3	PR27A	3	T	VREF1_3
P14	PR17B	3	C		PR26B	3	C	
P15	PR17A	3	T		PR26A	3	T	
R15	PR16B	3	C		PR25B	3	C	
R16	PR16A	3	T		PR25A	3	T	
M13	PR15B	3	C		PR24B	3	C	
M14	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
P16	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND3	3		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N13	GND	-			N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-			J7	VCC	-		
K16	VCC	-			K16	VCC	-			K16	VCC	-		
K17	VCC	-			K17	VCC	-			K17	VCC	-		
K6	VCC	-			K6	VCC	-			K6	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
L17	VCC	-			L17	VCC	-			L17	VCC	-		
L6	VCC	-			L6	VCC	-			L6	VCC	-		
M17	VCC	-			M17	VCC	-			M17	VCC	-		
M6	VCC	-			M6	VCC	-			M6	VCC	-		
N16	VCC	-			N16	VCC	-			N16	VCC	-		
N17	VCC	-			N17	VCC	-			N17	VCC	-		
N6	VCC	-			N6	VCC	-			N6	VCC	-		
N7	VCC	-			N7	VCC	-			N7	VCC	-		
P16	VCC	-			P16	VCC	-			P16	VCC	-		
P7	VCC	-			P7	VCC	-			P7	VCC	-		
G11	VCCIO0	0			G11	VCCIO0	0			G11	VCCIO0	0		
H10	VCCIO0	0			H10	VCCIO0	0			H10	VCCIO0	0		
H11	VCCIO0	0			H11	VCCIO0	0			H11	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0			H9	VCCIO0	0		
G12	VCCIO1	1			G12	VCCIO1	1			G12	VCCIO1	1		
H12	VCCIO1	1			H12	VCCIO1	1			H12	VCCIO1	1		
H13	VCCIO1	1			H13	VCCIO1	1			H13	VCCIO1	1		
H14	VCCIO1	1			H14	VCCIO1	1			H14	VCCIO1	1		
J15	VCCIO2	2			J15	VCCIO2	2			J15	VCCIO2	2		
K15	VCCIO2	2			K15	VCCIO2	2			K15	VCCIO2	2		
L15	VCCIO2	2			L15	VCCIO2	2			L15	VCCIO2	2		
L16	VCCIO2	2			L16	VCCIO2	2			L16	VCCIO2	2		
M15	VCCIO3	3			M15	VCCIO3	3			M15	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3			M16	VCCIO3	3		
N15	VCCIO3	3			N15	VCCIO3	3			N15	VCCIO3	3		
P15	VCCIO3	3			P15	VCCIO3	3			P15	VCCIO3	3		
R12	VCCIO4	4			R12	VCCIO4	4			R12	VCCIO4	4		
R13	VCCIO4	4			R13	VCCIO4	4			R13	VCCIO4	4		
R14	VCCIO4	4			R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4			T12	VCCIO4	4		
R10	VCCIO5	5			R10	VCCIO5	5			R10	VCCIO5	5		
R11	VCCIO5	5			R11	VCCIO5	5			R11	VCCIO5	5		
R9	VCCIO5	5			R9	VCCIO5	5			R9	VCCIO5	5		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U9	PB20B	5	C		U9	PB20B	5	C	
Y8	PB21A	5	T		Y8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
Y9	PB21B	5	C		Y9	PB21B	5	C	
V9	PB22A	5	T	BDQS22	V9	PB22A	5	T	BDQS22
T9	PB22B	5	C		T9	PB22B	5	C	
W10	PB23A	5	T		W10	PB23A	5	T	
U10	PB23B	5	C		U10	PB23B	5	C	
V10	PB24A	5	T		V10	PB24A	5	T	
T10	PB24B	5	C		T10	PB24B	5	C	
AA6	PB25A	5	T		AA6	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AB5	PB25B	5	C		AB5	PB25B	5	C	
AA8	PB26A	5	T		AA8	PB26A	5	T	
AA7	PB26B	5	C		AA7	PB26B	5	C	
AB6	PB27A	5	T		AB6	PB27A	5	T	
AB7	PB27B	5	C		AB7	PB27B	5	C	
Y10	PB28A	5	T		Y10	PB28A	5	T	
W11	PB28B	5	C		W11	PB28B	5	C	
AB8	PB29A	5	T		AB8	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AB9	PB29B	5	C		AB9	PB29B	5	C	
AA10	PB30A	5	T	BDQS30	AA10	PB30A	5	T	BDQS30
AA9	PB30B	5	C		AA9	PB30B	5	C	
Y11	PB31A	5	T		Y11	PB31A	5	T	
AA11	PB31B	5	C		AA11	PB31B	5	C	
V11	PB32A	5	T	VREF2_5	V11	PB32A	5	T	VREF2_5
V12	PB32B	5	C	VREF1_5	V12	PB32B	5	C	VREF1_5
AB10	PB33A	5	T	PCLKT5_0	AB10	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AB11	PB33B	5	C	PCLKC5_0	AB11	PB33B	5	C	PCLKC5_0
Y12	PB34A	4	T	WRITEN	Y12	PB34A	4	T	WRITEN
U11	PB34B	4	C	CS1N	U11	PB34B	4	C	CS1N
W12	PB35A	4	T	VREF1_4	W12	PB35A	4	T	VREF1_4
U12	PB35B	4	C	CSN	U12	PB35B	4	C	CSN
W13	PB36A	4	T	VREF2_4	W13	PB36A	4	T	VREF2_4
U13	PB36B	4	C	D0/SPID7	U13	PB36B	4	C	D0/SPID7
AA12	PB37A	4	T	D2/SPID5	AA12	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AB12	PB37B	4	C	D1/SPID6	AB12	PB37B	4	C	D1/SPID6
T13	PB38A	4	T	BDQS38	T13	PB38A	4	T	BDQS38
V13	PB38B	4	C	D3/SPID4	V13	PB38B	4	C	D3/SPID4
W14	PB39A	4	T		W14	PB39A	4	T	
U14	PB39B	4	C	D4/SPID3	U14	PB39B	4	C	D4/SPID3

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
D13	PT32B	0	C	VREF1_0	D13	PT32B	0	C	VREF1_0
C13	PT32A	0	T	VREF2_0	C13	PT32A	0	T	VREF2_0
A13	PT31B	0	C		A13	PT31B	0	C	
B13	PT31A	0	T		B13	PT31A	0	T	
F13	PT30B	0	C		F13	PT30B	0	C	
F12	PT30A	0	T	TDQS30	F12	PT30A	0	T	TDQS30
A12	PT29B	0	C		A12	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
B12	PT29A	0	T		B12	PT29A	0	T	
A11	PT28B	0	C		A11	PT28B	0	C	
B11	PT28A	0	T		B11	PT28A	0	T	
D12	PT27B	0	C		D12	PT27B	0	C	
C12	PT27A	0	T		C12	PT27A	0	T	
B10	PT26B	0	C		B10	PT26B	0	C	
A10	PT26A	0	T		A10	PT26A	0	T	
G12	PT25B	0	C		G12	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
A9	PT25A	0	T		A9	PT25A	0	T	
E12	PT24B	0	C		E12	PT24B	0	C	
B9	PT24A	0	T		B9	PT24A	0	T	
F11	PT23B	0	C		F11	PT23B	0	C	
A8	PT23A	0	T		A8	PT23A	0	T	
D11	PT22B	0	C		D11	PT22B	0	C	
C11	PT22A	0	T	TDQS22	C11	PT22A	0	T	TDQS22
B8	PT21B	0	C		B8	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
B7	PT21A	0	T		B7	PT21A	0	T	
E11	PT20B	0	C		E11	PT20B	0	C	
A7	PT20A	0	T		A7	PT20A	0	T	
G11	PT19B	0	C		G11	PT19B	0	C	
C7	PT19A	0	T		C7	PT19A	0	T	
G10	PT18B	0	C		G10	PT18B	0	C	
C6	PT18A	0	T		C6	PT18A	0	T	
C10	PT17B	0	C		C10	PT17B	0	C	
GND	GND0	0			GND	GND0	0		
D10	PT17A	0	T		D10	PT17A	0	T	
F10	PT16B	0	C		F10	PT16B	0	C	
A6	PT16A	0	T		A6	PT16A	0	T	
E10	PT15B	0	C		E10	PT15B	0	C	
C9	PT15A	0	T		C9	PT15A	0	T	
G9	PT14B	0	C		G9	PT14B	0	C	
D9	PT14A	0	T	TDQS14	D9	PT14A	0	T	TDQS14

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
M15	GND	-			M15	GND	-		
M16	GND	-			M16	GND	-		
M17	GND	-			M17	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N16	GND	-			N16	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P16	GND	-			P16	GND	-		
P17	GND	-			P17	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
R15	GND	-			R15	GND	-		
R16	GND	-			R16	GND	-		
R17	GND	-			R17	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T12	GND	-			T12	GND	-		
T13	GND	-			T13	GND	-		
T14	GND	-			T14	GND	-		
T15	GND	-			T15	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
H7	VCCAUX	-			H7	VCCAUX	-		
J19	VCCAUX	-			J19	VCCAUX	-		
J8	VCCAUX	-			J8	VCCAUX	-		
K7	VCCAUX	-			K7	VCCAUX	-		
L20	VCCAUX	-			L20	VCCAUX	-		
M20	VCCAUX	-			M20	VCCAUX	-		
M7	VCCAUX	-			M7	VCCAUX	-		
N20	VCCAUX	-			N20	VCCAUX	-		
P20	VCCAUX	-			P20	VCCAUX	-		
P7	VCCAUX	-			P7	VCCAUX	-		
T20	VCCAUX	-			T20	VCCAUX	-		
T7	VCCAUX	-			T7	VCCAUX	-		
T8	VCCAUX	-			T8	VCCAUX	-		
V19	VCCAUX	-			V19	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
W20	VCCAUX	-			W20	VCCAUX	-		
Y13	VCCAUX	-			Y13	VCCAUX	-		
Y7	VCCAUX	-			Y7	VCCAUX	-		
K19	VCC[1]	-			K19	VCCPLL	-		
L8	VCC[1]	-			L8	VCCPLL	-		
U19	VCC[1]	-			U19	VCCPLL	-		
U8	VCC[1]	-			U8	VCCPLL	-		

1. Tied to V_{CCPLL}.

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC1E-3QN208I	112	-3	Lead-Free PQFP	208	IND	1.5K
LFEC1E-4QN208I	112	-4	Lead-Free PQFP	208	IND	1.5K
LFEC1E-3TN144I	97	-3	Lead-Free TQFP	144	IND	1.5K
LFEC1E-4TN144I	97	-4	Lead-Free TQFP	144	IND	1.5K
LFEC1E-3TN100I	67	-3	Lead-Free TQFP	100	IND	1.5K
LFEC1E-4TN100I	67	-4	Lead-Free TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC3E-3FN256I	160	-3	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-4FN256I	160	-4	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-3QN208I	145	-3	Lead-Free PQFP	208	IND	3.1K
LFEC3E-4QN208I	145	-4	Lead-Free PQFP	208	IND	3.1K
LFEC3E-3TN144I	97	-3	Lead-Free TQFP	144	IND	3.1K
LFEC3E-4TN144I	97	-4	Lead-Free TQFP	144	IND	3.1K
LFEC3E-3TN100I	67	-3	Lead-Free TQFP	100	IND	3.1K
LFEC3E-4TN100I	67	-4	Lead-Free TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

LatticeECP/EC Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com