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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	19700
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp20e-5f484c

Figure 2-4. Slice Diagram

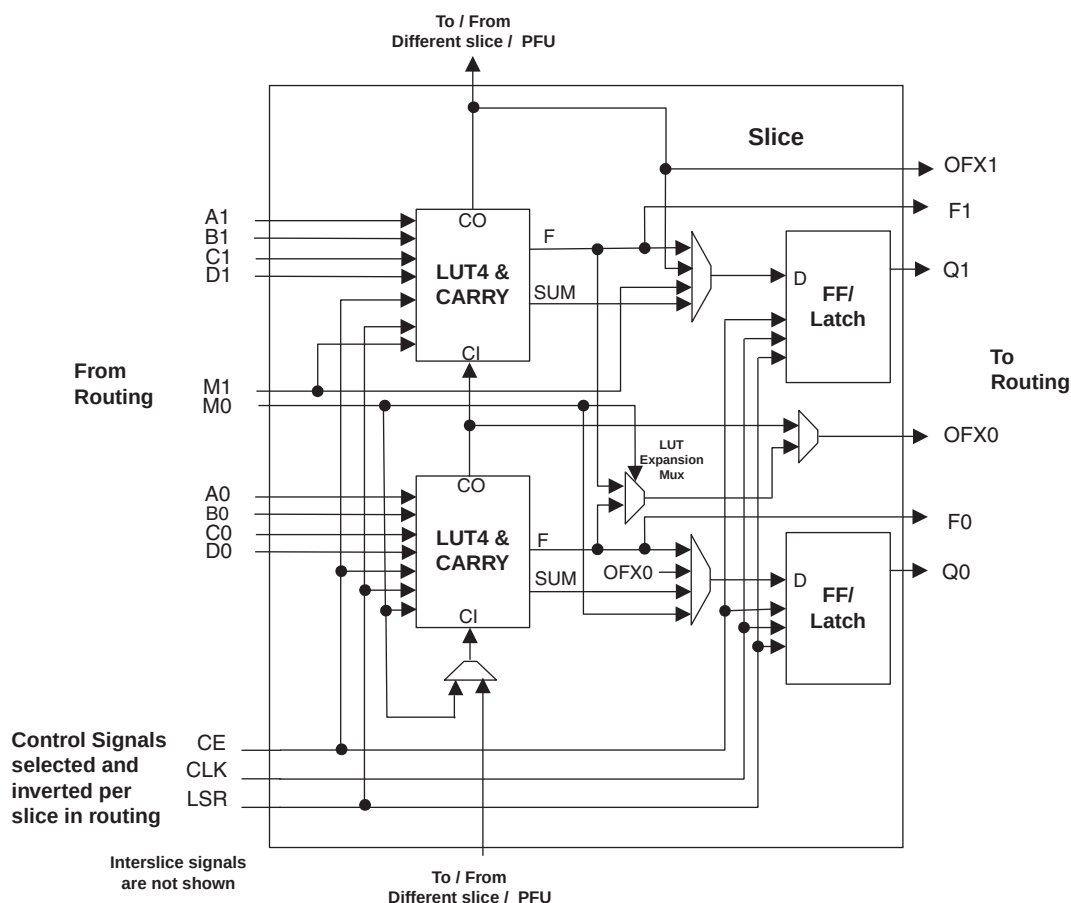


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Table 2-7. Maximum Number of Elements in a Block

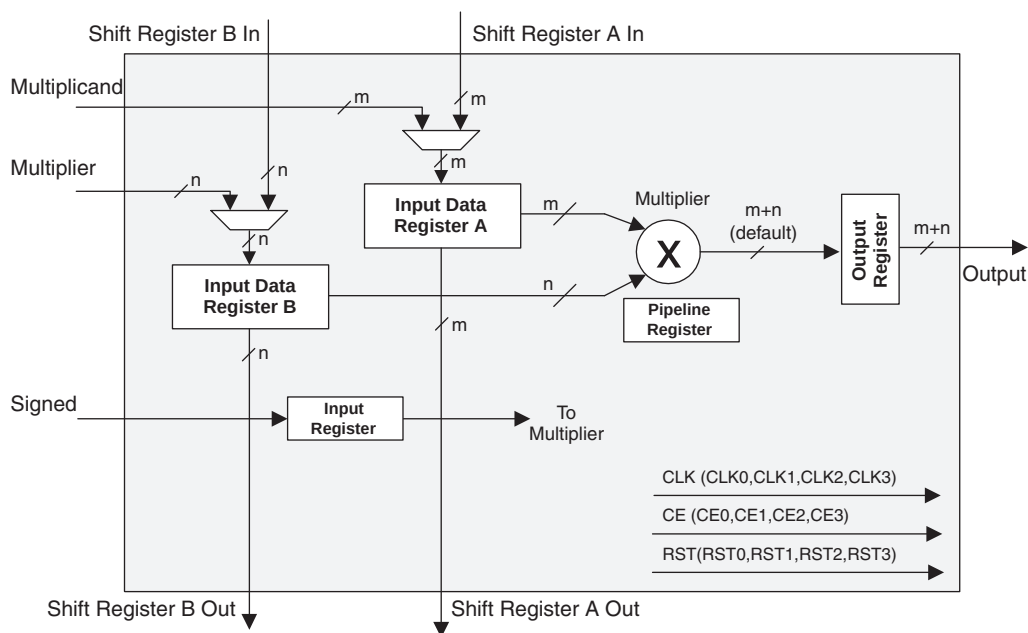
Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADD	4	2	—
MULTADDSUM	2	1	—

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift registers from previous operand registers. In addition by selecting “dynamic operation” in the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle. Similarly by selecting ‘Dynamic operation’ in the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-19 shows the MULT sysDSP element.

Figure 2-19. MULT sysDSP Element



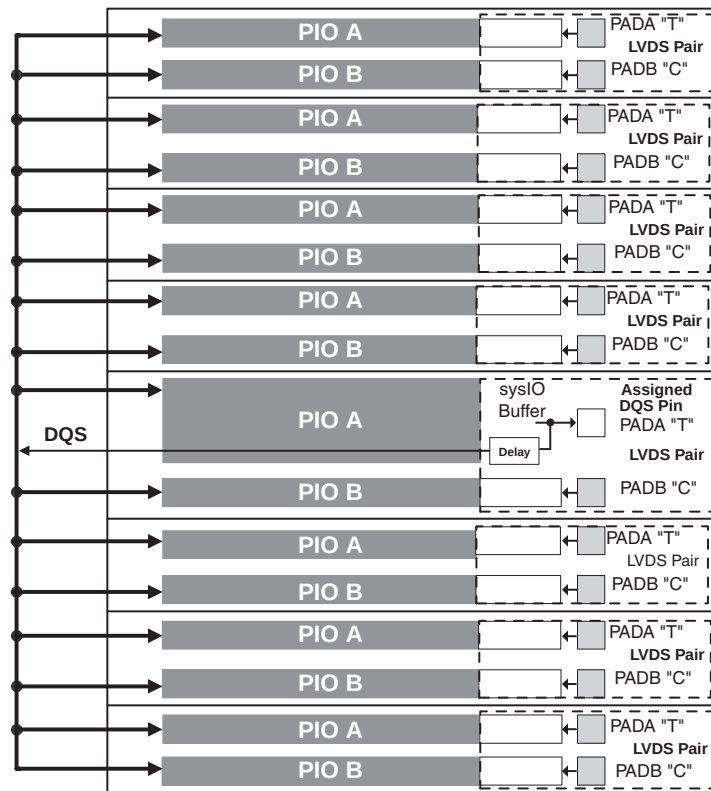
MAC sysDSP Element

In this case the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-20 shows the MAC sysDSP element.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDR _X registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

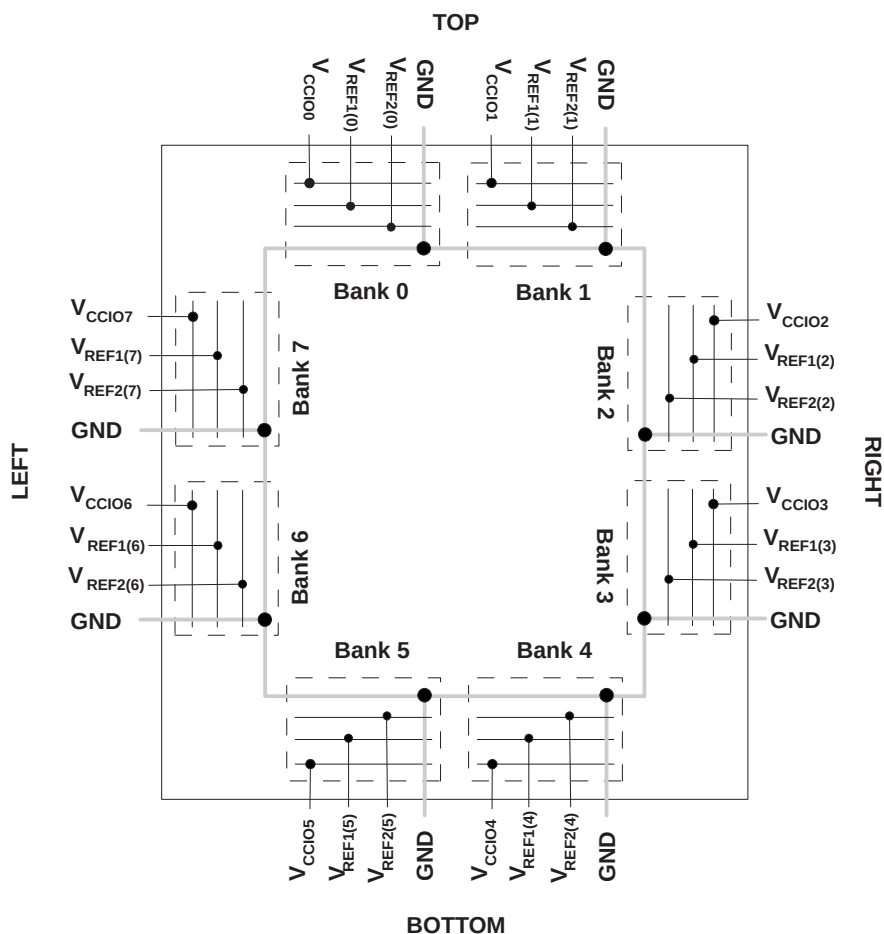
Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Figure 2-34. LatticeECP/EC Banks



LatticeECP/EC devices contain two types of sysI/O buffer pairs.

1. Top and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)

The sysI/O buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps. These I/O banks also support hot socketing with I_{DK} less than 1mA. Note that the PCI clamp is enabled after V_{CC} , V_{CCAUX} and V_{CCIO} are at valid operating levels and the device has been configured.

2. Left and Right sysI/O Buffer Pairs (Differential and Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Only the left and right banks have LVDS differential output drivers. See the I_{DK} specification for I/O leakage current during power-up.

Table 2-14. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3
RSDS ¹	N/A	2.5

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}^1	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) \leq V_{IH} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHLH}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, $f = 1.0MHz$

3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO} .

Initialization Supply Current^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Symbol	Parameter	Devices	Typ. ⁶	Units
I _{CC}	Core Power Supply Current	LFEC1	25	mA
		LFEC3	40	mA
		LFEC6/LFEC6	50	mA
		LFEC10/LFEC10	60	mA
		LFEC15/LFEC15	70	mA
		LFEC20/LFEC20	150	mA
		LFEC33/LFEC33	220	mA
I _{CCAUX}	Auxiliary Power Supply Current	LFEC1	30	mA
		LFEC3	30	mA
		LFEC6/LFEC6	30	mA
		LFEC10/LFEC10	35	mA
		LFEC15/LFEC15	35	mA
		LFEC20/LFEC20	40	mA
		LFEC33/LFEC33	40	mA
I _{CCPLL}	PLL Power Supply Current		12	mA
I _{CCIO}	Bank Power Supply Current ⁷	LFEC1	4	mA
		LFEC3	5	mA
		LFEC6/LFEC6	6	mA
		LFEC10/LFEC10	6	mA
		LFEC15/LFEC15	7	mA
		LFEC20/LFEC20	8	mA
		LFEC33/LFEC33	8	mA
I _{CCJ}	V _{CCJ} Power Supply Current		20	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.

6. T_J=25°C, power supplies at nominal voltage.

7. Per bank.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

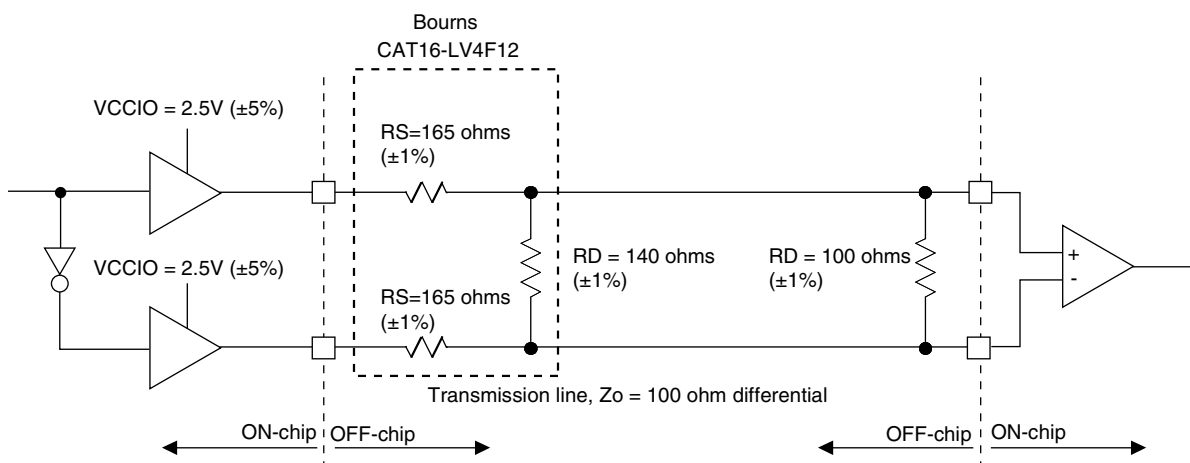


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{OH}	Output high voltage	1.42	V
V _{OL}	Output low voltage	1.08	V
V _{OD}	Output differential voltage	0.35	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	100	Ω

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL) ¹									
t _{CO} ⁷	Clock to Output - PIO Output Register	LFEC1	—	5.09	—	6.11	—	7.13	ns
		LFEC3	—	5.71	—	6.85	—	7.99	ns
		LFEC6	—	5.60	—	6.72	—	7.84	ns
		LFEC10	—	5.47	—	6.57	—	7.66	ns
		LFEC15	—	5.67	—	6.81	—	7.94	ns
		LFEC20	—	5.89	—	7.07	—	8.25	ns
		LFEC33	—	6.19	—	7.42	—	8.66	ns
t _{SU} ⁷	Clock to Data Setup - PIO Input Register	LFEC1	-0.08	—	-0.10	—	-0.12	—	ns
		LFEC3	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC6	-0.63	—	-0.76	—	-0.89	—	ns
		LFEC10	-0.43	—	-0.52	—	-0.61	—	ns
		LFEC15	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC20	-0.88	—	-1.06	—	-1.24	—	ns
		LFEC33	-1.12	—	-1.34	—	-1.56	—	ns
t _H ⁷	Clock to Data Hold - PIO Input Register	LFEC1	2.19	—	2.62	—	3.06	—	ns
		LFEC3	2.80	—	3.36	—	3.92	—	ns
		LFEC6	2.69	—	3.23	—	3.77	—	ns
		LFEC10	2.56	—	3.08	—	3.59	—	ns
		LFEC15	2.76	—	3.32	—	3.87	—	ns
		LFEC20	2.99	—	3.58	—	4.18	—	ns
		LFEC33	3.28	—	3.93	—	4.59	—	ns
t _{SU_DEL} ⁷	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC1	3.36	—	4.03	—	4.70	—	ns
		LFEC3	2.74	—	3.29	—	3.84	—	ns
		LFEC6	2.81	—	3.37	—	3.93	—	ns
		LFEC10	3.01	—	3.61	—	4.21	—	ns
		LFEC15	2.74	—	3.29	—	3.83	—	ns
		LFEC20	2.56	—	3.07	—	3.58	—	ns
		LFEC33	2.32	—	2.79	—	3.25	—	ns
t _{H_DEL} ⁷	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC1	-1.31	—	-1.57	—	-1.83	—	ns
		LFEC3	-0.70	—	-0.83	—	-0.97	—	ns
		LFEC6	-0.80	—	-0.96	—	-1.12	—	ns
		LFEC10	-0.93	—	-1.12	—	-1.30	—	ns
		LFEC15	-0.73	—	-0.88	—	-1.02	—	ns
		LFEC20	-0.51	—	-0.61	—	-0.71	—	ns
		LFEC33	-0.22	—	-0.26	—	-0.30	—	ns
f _{MAX_IO} ²	Clock Frequency of I/O and PFU Register	All	—	420	—	378	—	340	Mhz
DDR I/O Pin Parameters ^{3, 4, 5}									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI



LatticeECP/EC Family Data Sheet

Pinout Information

September 2012

Data Sheet

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins.
V _{CCIOx}	—	Power supply pins for I/O bank x. Dedicated pins.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES	—	10K ohm +/-1% resistor must be connected between this pad and ground.
V _{CCPLL}	—	Power supply pin for PLL. Applicable to ECP/EC33 device.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	I	Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_PLL[T, C]_FB_A	I	Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.

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Pin Information Summary (Cont.)

		LFEC/EC15		LFEC/EC20		LFEC/EC33	
Pin Type		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V _{CC}		10	20	20	32	16	28
V _{CCAUX}		2	12	12	20	12	20
V _{CCPLL}		0	0	0	0	4	4
V _{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V _{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

Power Supply and NC Connections (Cont.)

Signals	484 fpBGA	672 fpBGA
VCC	J16, J7, K16, K17, K6, K7, L17, L6, M17, M6, N16, N17, N6, N7, P16, P7, J6, J17, P6, P17	H10, H11, H16, H17, H18, H19, H8, H9, J18, J9, K8, L19, M19, N7, R20, R7, T19, V18, V8, V9, W10, W11, W16, W17, W18, W19, W8, W9, K19, L8, U19, U8
VCCIO0	G11, H10, H11, H9	H12, H13, J10, J11, J12, J13
VCCIO1	G12, H12, H13, H14	H14, H15, J14, J15, J16, J17
VCCIO2	J15, K15, L15, L16	K17, K18, L18, M18, N18, N19
VCCIO3	M15, M16, N15, P15	P18, P19, R18, R19, T18, U18
VCCIO4	R12, R13, R14, T12	V14, V15, V16, V17, W14, W15
VCCIO5	R10, R11, R9, T11	V10, V11, V12, V13, W12, W13
VCCIO6	M7, M8, N8, P8	P8, P9, R8, R9, T9, U9
VCCIO7	J8, K8, L7, L8	K9, L9, M8, M9, N8, N9
VCCJ	U2	U6
VCCAUX	G15, G16, G7, G8, H16, H7, R16, R7, T15, T16, T7, T8	G13, H20, H7, J19, J8, K7, L20, M20, M7, N20, P20, P7, T20, T7, T8, V19, V7, W20, Y13, Y7
VCCPLL	ECP/EC20: None ECP/EC33: J6, J17, P6, P17	ECP/EC20: None ECP/EC33: K19, L8, U19, U8
GND, GND0-GND7	A1, A22, AB1, AB22, H15, H8, J10, J11, J12, J13, J14, J9, K10, K11, K12, K13, K14, K9, L10, L11, L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R15, R8	K10, K11, K12, K13, K14, K15, K16, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17
NC	ECP/EC6: C3, B2, E5, F5, D3, C2, F4, G4, E3, D2, B1, C1, F3, E2, G5, H6, G3, H4, J5, H5, F2, F1, E1, D1, R6, P5, P3, P4, R1, R2, R5, R4, T1, T2, R3, T3, V7, T6, V8, U7, W5, U6, AA3, AB3, Y6, V6, AA5, W6, Y5, Y4, AA4, AB4, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, E21, D22, G21, G20, J18, H19, J19, H20, H17, H18, D21, C22, G19, G18, F20, F19, E20, D20, C21, C20, F18, E18, B22, B21, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A4, B4, C4, C5, D6, B5, E6, C6, A3, B3, F6, D5, F7, E8, G6, E7, A2, AB2, A21 ECP/EC10: G5, H6, G3, H4, J5, H5, F2, F1, R6, P5, P3, P4, R2, R1, R5, R4, T1, T2, R3, T3, W16, U15, V16, U16, Y17, V17, AB20, AA19, Y16, W17, AA20, Y19, Y18, W18, T17, U17, T18, R17, R19, R18, U22, T22, R21, R22, P20, N20, P19, P18, G21, G20, J18, H19, J19, H20, H17, H18, G17, F17, D18, C18, C19, B20, D17, C16, B19, A20, E17, C17, F16, E16, F15, D16, A2, AB2, A21 ECP/EC15: T1, T2, R3, T3, T18, R17, R19, R18, A2, AB2, A21 ECP/EC20: A2, AB2, A21 ECP/EC33: A2, AB2, A21	ECP/EC20: E5, D5, F4, F5, C3, D3, C2, B2, H6, J7, G5, H5, H3, J3, H2, J2, AA2, AA3, W5, Y5, Y6, W7, AA4, AB3, AC2, AC3, AA5, AB5, AD3, AD2, AE1, AD1, AD19, AD20, AC19, AB19, AD21, AC20, AF25, AE25, AB21, AB20, AE24, AD23, AD22, AC21, AC22, AB22, AD24, AD25, AE26, AD26, Y20, Y19, AA23, AA22, AB23, AB24, Y21, AA21, Y23, Y22, AA24, Y24, J21, J22, J23, H22, G26, F26, E26, E25, F24, F23, E24, D24, E22, F22, E21, D22, G20, F20, D21, C21, C23, C22, B23, C24, D20, E19, B25, B24, B26, A25, C20, C19 ECP/EC33: None

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N16	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
N15	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
M15	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
M16	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
L16	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
K16	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
J16	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
	-	-			GND3	3		
H16	NC	-			PR18B	3	C	
H15	NC	-			PR18A	3	T	
G16	NC	-			PR17B	3	C	
G15	NC	-			PR17A	3	T	
K12	NC	-			PR16B	3	C	
J12	NC	-			PR16A	3	T	
J14	NC	-			PR15B	3	C	
J15	NC	-			PR15A	3	T	RDQS15
F16	NC	-			PR14B	3	C	
-	-	-			GND3	3		
F15	NC	-			PR14A	3	T	
J13	NC	-			PR13B	3	C	
H13	NC	-			PR13A	3	T	
H14	NC	-			PR12B	3	C	
G14	NC	-			PR12A	3	T	
E16	NC	-			PR11B	3	C	
E15	NC	-			PR11A	3	T	
H12	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
GND	GND2	2			GND2			
G12	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
G13	PR8B	2	C		PR8B	2	C	
F13	PR8A	2	T		PR8A	2	T	
F12	PR7B	2	C		PR7B	2	C	
E13	PR7A	2	T		PR7A	2	T	
D16	PR6B	2	C		PR6B	2	C	
D15	PR6A	2	T	RDQS6	PR6A	2	T	RDQS6
F14	PR5B	2	C		PR5B	2	C	
E14	PR5A	2	T		PR5A	2	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
N22	PR30A	3	T		N22	PR42A	3	T	
N19	PR29B	3	C		N19	PR41B	3	C	
N18	PR29A	3	T		N18	PR41A	3	T	
M21	PR28B	3	C		M21	PR40B	3	C	
L20	PR28A	3	T	RDQS28	L20	PR40A	3	T	RDQS40
L21	PR27B	3	C		L21	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M20	PR27A	3	T		M20	PR39A	3	T	
M18	PR26B	3	C		M18	PR38B	3	C	
M19	PR26A	3	T		M19	PR38A	3	T	
M22	PR25B	3	C		M22	PR37B	3	C	
L22	PR25A	3	T		L22	PR37A	3	T	
K22	PR24B	3	C		K22	PR36B	3	C	
K21	PR24A	3	T		K21	PR36A	3	T	
J22	PR22B	2	C	PCLKC2_0	J22	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
J21	PR22A	2	T	PCLKT2_0	J21	PR34A	2	T	PCLKT2_0
H22	PR21B	2	C		H22	PR33B	2	C	
H21	PR21A	2	T		H21	PR33A	2	T	
L19	PR20B	2	C		L19	PR32B	2	C	
L18	PR20A	2	T		L18	PR32A	2	T	
K20	PR19B	2	C		K20	PR31B	2	C	
J20	PR19A	2	T	RDQS19	J20	PR31A	2	T	RDQS31
K19	PR18B	2	C		K19	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
K18	PR18A	2	T		K18	PR30A	2	T	
G22	PR17B	2	C		G22	PR29B	2	C	
F22	PR17A	2	T		F22	PR29A	2	T	
F21	PR16B	2	C		F21	PR28B	2	C	
E22	PR16A	2	T		E22	PR28A	2	T	
E21	PR15B	2	C		E21	PR27B	2	C	
D22	PR15A	2	T		D22	PR27A	2	T	
G21	PR14B	2	C		G21	PR26B	2	C	
G20	PR14A	2	T		G20	PR26A	2	T	
GND	GND2	2			GND	GND2	2		
J18	PR13B	2	C		J18	PR25B	2	C	
H19	PR13A	2	T		H19	PR25A	2	T	
J19	PR12B	2	C		J19	PR24B	2	C	
H20	PR12A	2	T		H20	PR24A	2	T	
H17	PR11B	2	C		H17	PR23B	2	C	
H18	PR11A	2	T		H18	PR23A	2	T	RDQS23
D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
GND	-	-			GND	GND2	2		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

Conventional Packaging
LatticeEC Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208C	112	-3	PQFP	208	COM	1.5K
LFEC1E-4Q208C	112	-4	PQFP	208	COM	1.5K
LFEC1E-5Q208C	112	-5	PQFP	208	COM	1.5K
LFEC1E-3T144C	97	-3	TQFP	144	COM	1.5K
LFEC1E-4T144C	97	-4	TQFP	144	COM	1.5K
LFEC1E-5T144C	97	-5	TQFP	144	COM	1.5K
LFEC1E-3T100C	67	-3	TQFP	100	COM	1.5K
LFEC1E-4T100C	67	-4	TQFP	100	COM	1.5K
LFEC1E-5T100C	67	-5	TQFP	100	COM	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256C	160	-3	fpBGA	256	COM	3.1K
LFEC3E-4F256C	160	-4	fpBGA	256	COM	3.1K
LFEC3E-5F256C	160	-5	fpBGA	256	COM	3.1K
LFEC3E-3Q208C	145	-3	PQFP	208	COM	3.1K
LFEC3E-4Q208C	145	-4	PQFP	208	COM	3.1K
LFEC3E-5Q208C	145	-5	PQFP	208	COM	3.1K
LFEC3E-3T144C	97	-3	TQFP	144	COM	3.1K
LFEC3E-4T144C	97	-4	TQFP	144	COM	3.1K
LFEC3E-5T144C	97	-5	TQFP	144	COM	3.1K
LFEC3E-3T100C	67	-3	TQFP	100	COM	3.1K
LFEC3E-4T100C	67	-4	TQFP	100	COM	3.1K
LFEC3E-5T100C	67	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFEC6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFEC6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFEC6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFEC6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFEC6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFEC6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFEC6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFEC6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFEC6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFEC6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFEC6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFEC10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFEC10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFEC10E-3F256C	195	-3	fpBGA	256	COM	10.2K

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFCEP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFCEP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFCEP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFCEP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFCEP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFCEP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFCEP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFCEP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFCEP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFCEP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFCEP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFCEP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFCEP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFCEP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFCEP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFCEP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFCEP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFCEP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFCEP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFCEP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFCEP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFCEP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFCEP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFCEP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFCEP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFCEP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFCEP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFCEP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFCEP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFCEP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFCEP33E-5F672C	496	-5	fpBGA	672	COM	32.8K

LatticeECP Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672I	400	-3	fpBGA	672	IND	19.7K
LFCEP20E-4F672I	400	-4	fpBGA	672	IND	19.7K
LFCEP20E-3F484I	360	-3	fpBGA	484	IND	19.7K
LFCEP20E-4F484I	360	-4	fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672I	496	-3	fpBGA	672	IND	32.8K
LFCEP33E-4F672I	496	-4	fpBGA	672	IND	32.8K
LFCEP33E-3F484I	360	-3	fpBGA	484	IND	32.8K
LFCEP33E-4F484I	360	-4	fpBGA	484	IND	32.8K