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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	32800
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp33e-3fn484c

Figure 2-4. Slice Diagram

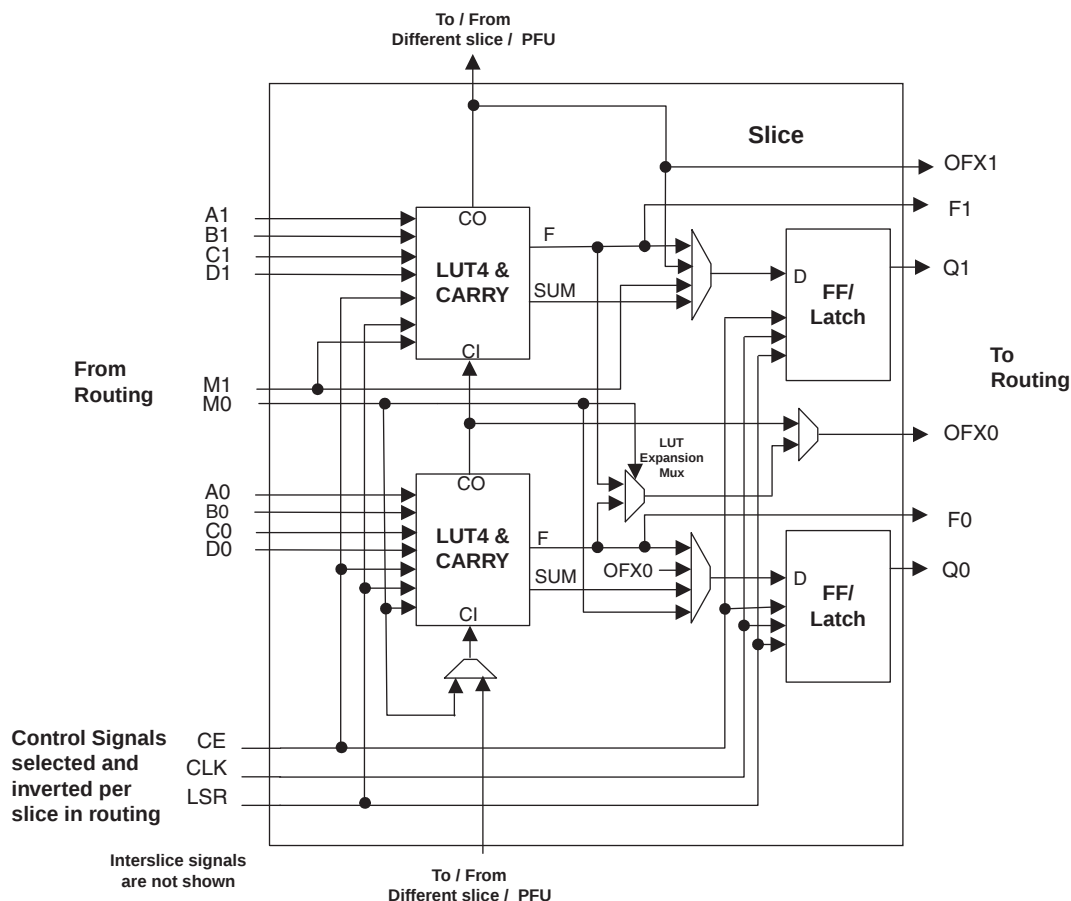


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, the routing of both short and long connections between PFUs.

The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

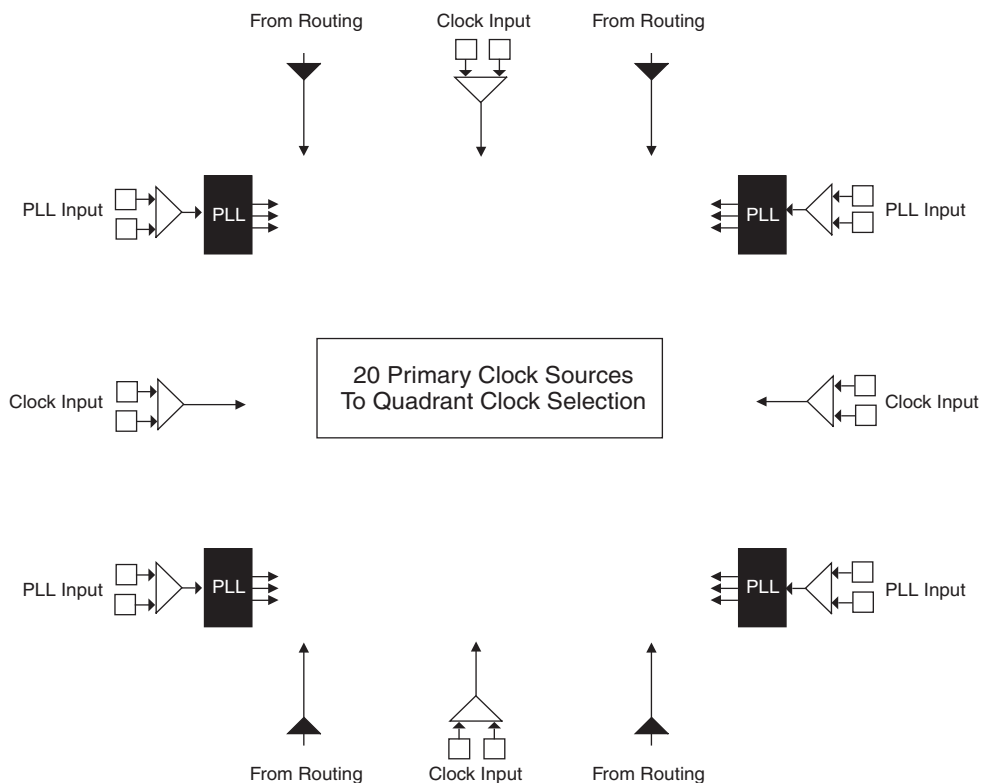
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Primary Clock Sources



Note: Smaller devices have two PLLs.

Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

Figure 2-13. DCS Block Primitive

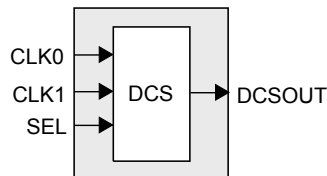
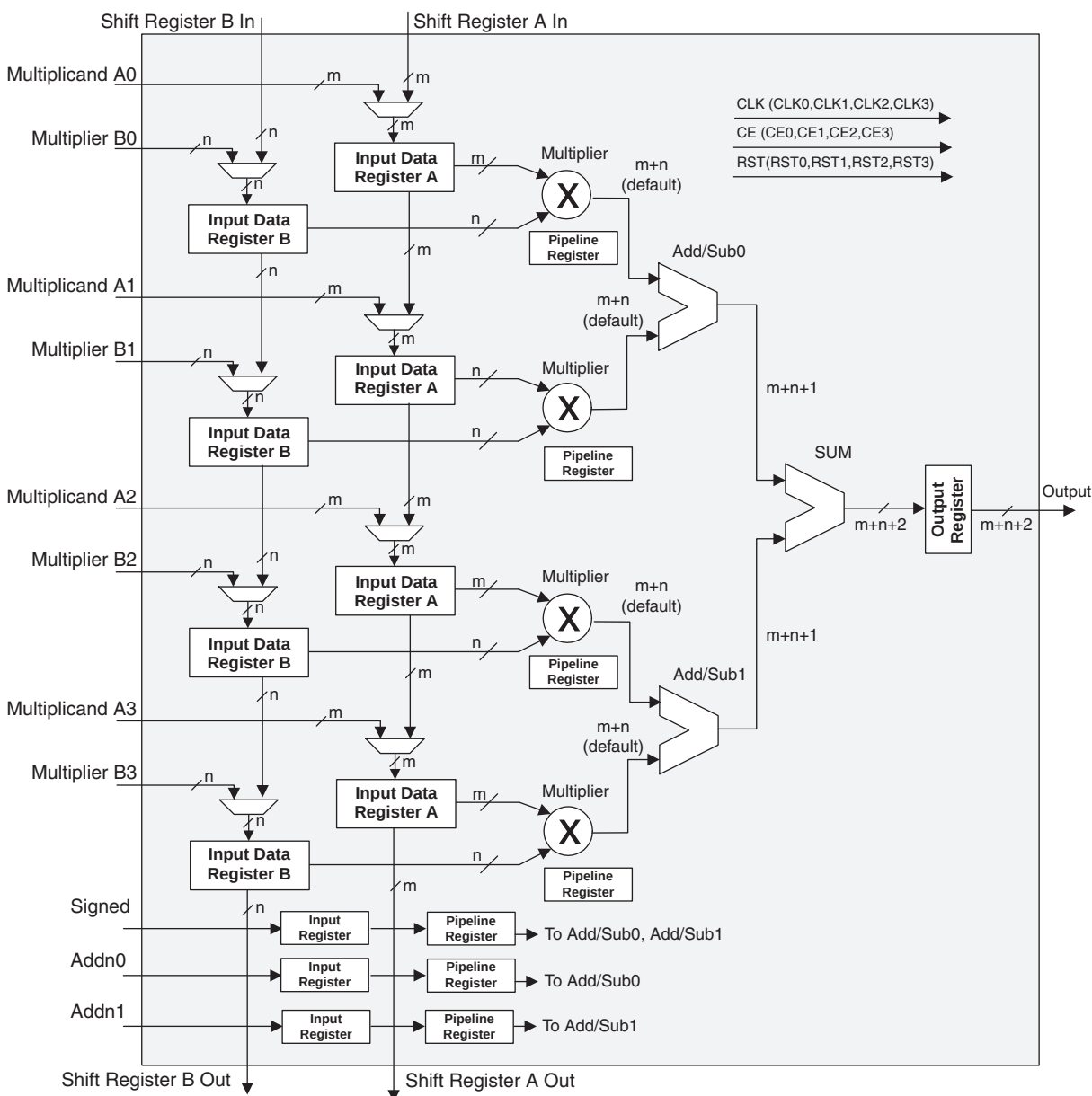


Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUM sysDSP element.

Figure 2-22. MULTADDSUM



Clock, Clock Enable and Reset Resources

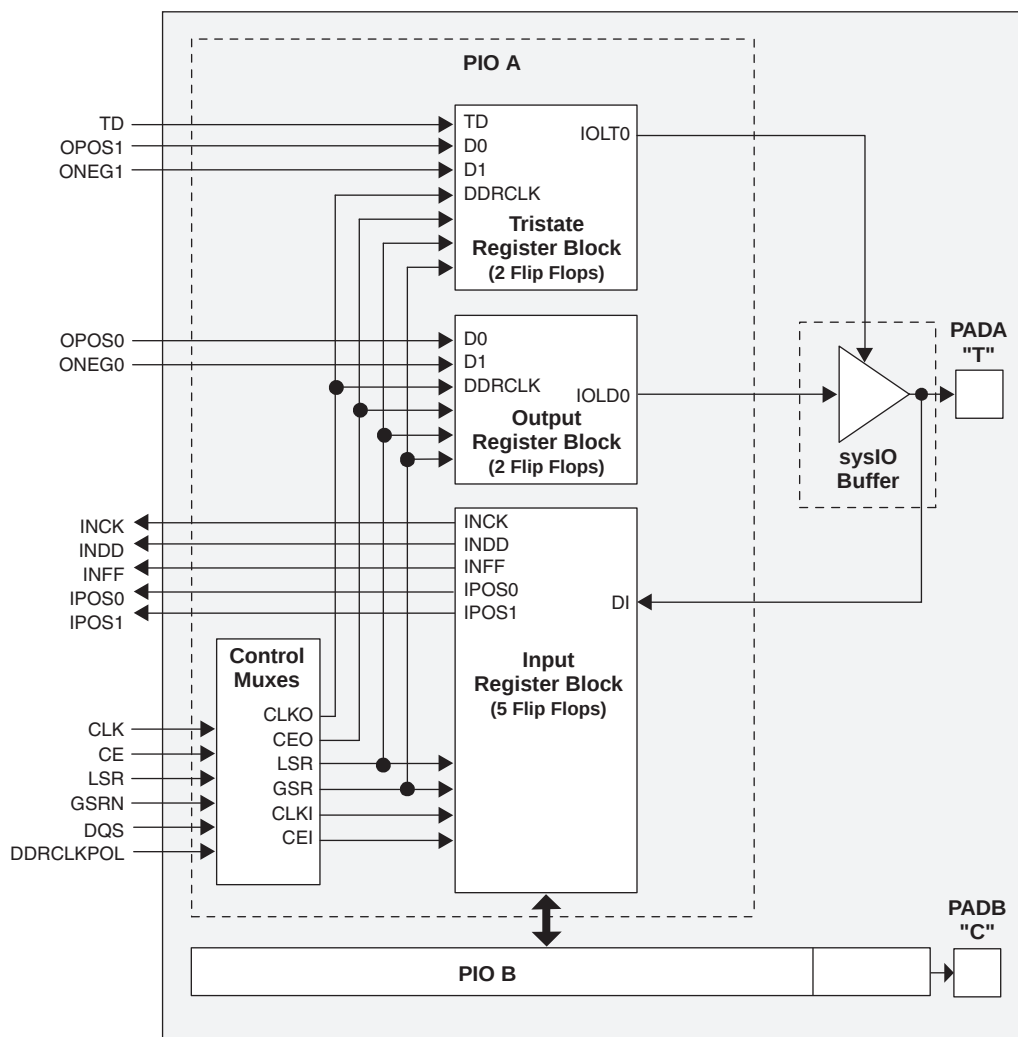
Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master clock for configuration. The oscillator and the master clock run continuously. The default value of the master clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information about the use of this oscillator for configuration, please see the list of technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5*	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

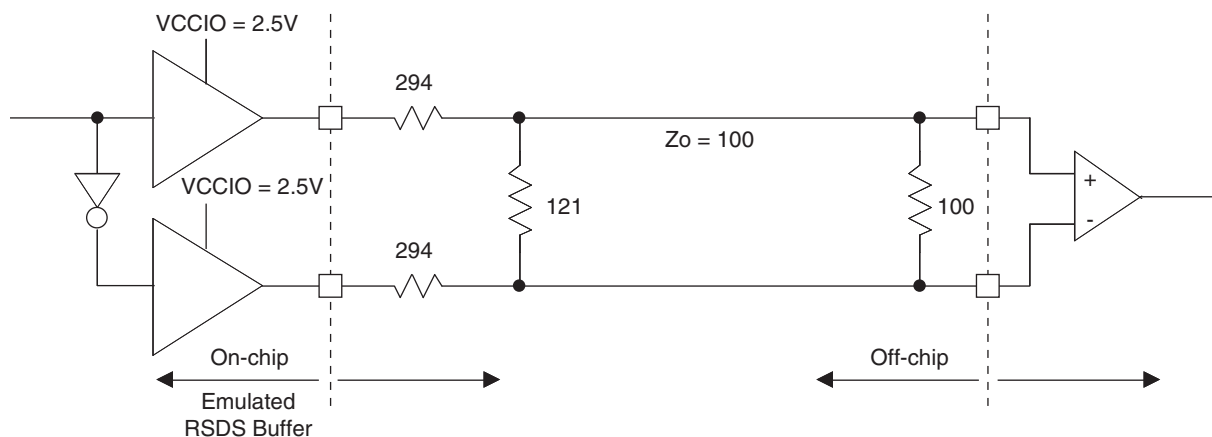


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	ohm
R _S	Driver series resistor	294	ohm
R _P	Driver parallel resistor	121	ohm
R _T	Receiver termination	100	ohm
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	101.5	ohm
I _{DC}	DC output current	3.66	mA

LatticeECP/EC Family Timing Adders^{1, 2, 3}
Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25	LVDS	0.41	0.50	0.58	ns
BLVDS25	BLVDS	0.41	0.50	0.58	ns
LVPECL33	LVPECL	0.50	0.60	0.70	ns
HSTL18_I	HSTL_18 class I	0.41	0.49	0.57	ns
HSTL18_II	HSTL_18 class II	0.41	0.49	0.57	ns
HSTL18_III	HSTL_18 class III	0.41	0.49	0.57	ns
HSTL18D_I	Differential HSTL 18 class I	0.37	0.44	0.52	ns
HSTL18D_II	Differential HSTL 18 class II	0.37	0.44	0.52	ns
HSTL18D_III	Differential HSTL 18 class III	0.37	0.44	0.52	ns
HSTL15_I	HSTL_15 class I	0.40	0.48	0.56	ns
HSTL15_III	HSTL_15 class III	0.40	0.48	0.56	ns
HSTL15D_I	Differential HSTL 15 class I	0.37	0.44	0.51	ns
HSTL15D_III	Differential HSTL 15 class III	0.37	0.44	0.51	ns
SSTL33_I	SSTL_3 class I	0.46	0.55	0.64	ns
SSTL33_II	SSTL_3 class II	0.46	0.55	0.64	ns
SSTL33D_I	Differential SSTL_3 class I	0.39	0.47	0.55	ns
SSTL33D_II	Differential SSTL_3 class II	0.39	0.47	0.55	ns
SSTL25_I	SSTL_2 class I	0.43	0.51	0.60	ns
SSTL25_II	SSTL_2 class II	0.43	0.51	0.60	ns
SSTL25D_I	Differential SSTL_2 class I	0.38	0.45	0.53	ns
SSTL25D_II	Differential SSTL_2 class II	0.38	0.45	0.53	ns
SSTL18_I	SSTL_18 class I	0.40	0.48	0.56	ns
SSTL18D_I	Differential SSTL_18 class I	0.37	0.44	0.51	ns
LVTTL33	LVTTL	0.07	0.09	0.10	ns
LVC MOS33	LVC MOS 3.3	0.07	0.09	0.10	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	0.07	0.09	0.10	ns
LVC MOS15	LVC MOS 1.5	0.24	0.29	0.33	ns
LVC MOS12	LVC MOS 1.2	1.27	1.52	1.77	ns
PCI33	PCI	0.07	0.09	0.10	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	0.12	0.14	0.17	ns
LVDS25	LVDS 2.5	-0.44	-0.53	-0.62	ns
BLVDS25	BLVDS 2.5	0.33	0.40	0.46	ns
LVPECL33	LVPECL 3.3	0.20	0.24	0.28	ns
HSTL18_I	HSTL_18 class I	-0.10	-0.12	-0.14	ns
HSTL18_II	HSTL_18 class II	0.06	0.07	0.08	ns
HSTL18_III	HSTL_18 class III	0.15	0.19	0.22	ns
HSTL18D_I	Differential HSTL 18 class I	-0.10	-0.12	-0.14	ns
HSTL18D_II	Differential HSTL 18 class II	0.06	0.07	0.08	ns
HSTL18D_III	Differential HSTL 18 class III	0.15	0.19	0.22	ns
HSTL15_I	HSTL_15 class I	0.08	0.10	0.11	ns

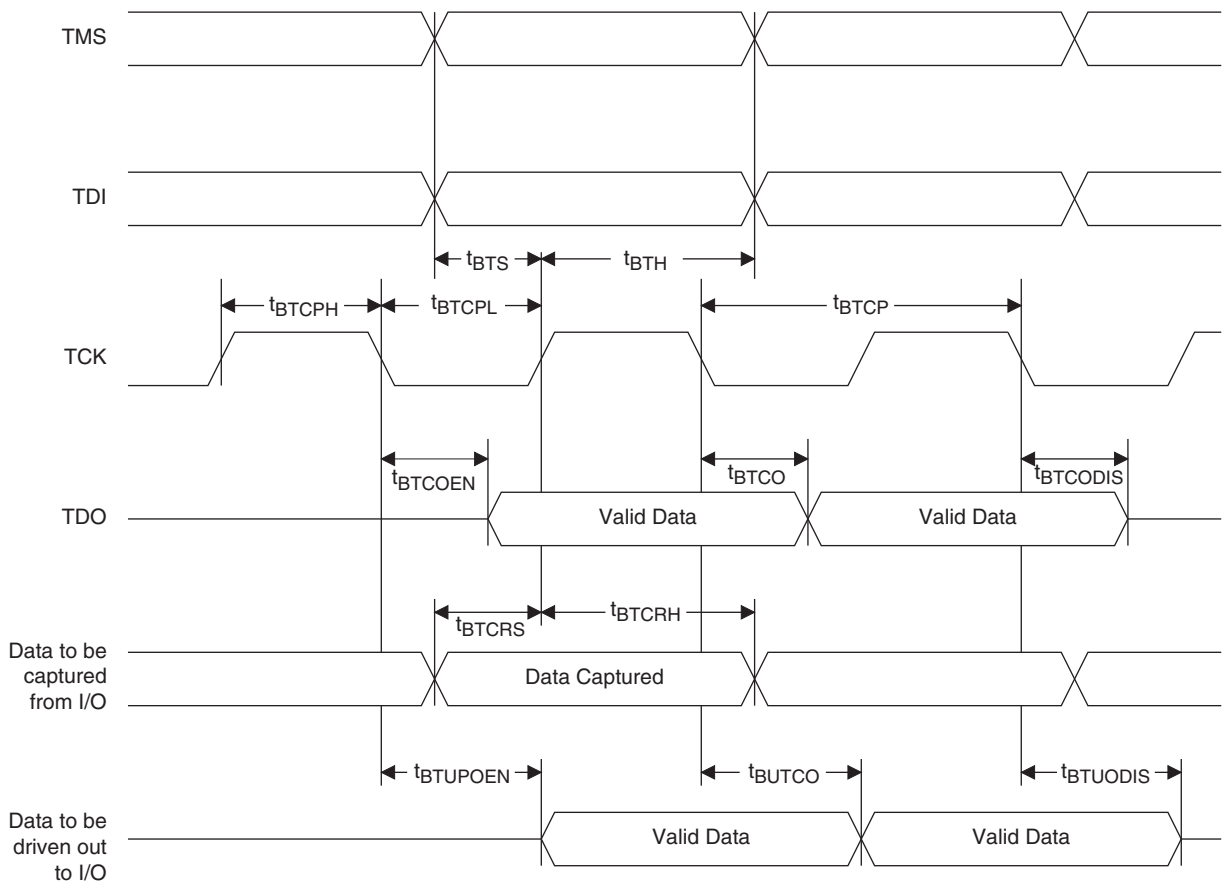
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.G 0.30

Figure 3-20. JTAG Port Timing Waveforms



LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
169	PT13A	1	T		PT21A	1	T	
170	PT12B	1	C		PT20B	1	C	
171	PT12A	1	T		PT20A	1	T	
172	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
173	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
174	PT10B	1	C		PT18B	1	C	
175	PT10A	1	T		PT18A	1	T	
176	VCCIO1	1			VCCIO1	1		
177	VCCAUX	-			VCCAUX	-		
178	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
179	GND0	0			GND0	0		
180	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
181	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
182	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
183	PT7B	0	C		PT15B	0	C	
184	PT7A	0	T		PT15A	0	T	
185	PT6B	0	C		PT14B	0	C	
186	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
187	VCCIO0	0			VCCIO0	0		
188	PT5B	0	C		PT13B	0	C	
189	NC	-			GND0	0		
190	PT5A	0	T		PT13A	0	T	
191	PT4B	0	C		PT12B	0	C	
192	PT4A	0	T		PT12A	0	T	
193	PT3B	0	C		PT11B	0	C	
194	PT3A	0	T		PT11A	0	T	
195	PT2B	0	C		PT10B	0	C	
196	PT2A	0	T		PT10A	0	T	
197	NC	-			VCCIO0	0		
198	NC	-			PT6B	0	C	
199	NC	-			PT6A	0	T	TDQS6
200	NC	-			PT5B	0	C	
201	NC	-			PT5A	0	T	
202	NC	-			PT4B	0	C	
203	NC	-			PT4A	0	T	
204	NC	-			PT3B	0	C	
205	NC	-			PT3A	0	T	
206	NC	-			PT2B	0	C	
207	NC	-			PT2A	0	T	
208	VCCIO0	0			VCCIO0	0		

* Double bonded to the pin.

LFEC6/EC6, LFEC6/EC10 Logic Signal Connections: 208 PQFP

Pin Number	LFEC6/LFEC6				LFEC10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N16	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
N15	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
M15	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
M16	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
L16	PR12A	3	T	DOUT/CSON	PR21A	3	T	DOUT/CSON
K16	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
J16	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
L12	CFG2	3			CFG2	3		
L14	CFG1	3			CFG1	3		
L13	CFG0	3			CFG0	3		
K13	PROGRAMN	3			PROGRAMN	3		
L15	CCLK	3			CCLK	3		
K15	INITN	3			INITN	3		
K14	DONE	3			DONE	3		
	-	-			GND3	3		
H16	NC	-			PR18B	3	C	
H15	NC	-			PR18A	3	T	
G16	NC	-			PR17B	3	C	
G15	NC	-			PR17A	3	T	
K12	NC	-			PR16B	3	C	
J12	NC	-			PR16A	3	T	
J14	NC	-			PR15B	3	C	
J15	NC	-			PR15A	3	T	RDQS15
F16	NC	-			PR14B	3	C	
-	-	-			GND3	3		
F15	NC	-			PR14A	3	T	
J13	NC	-			PR13B	3	C	
H13	NC	-			PR13A	3	T	
H14	NC	-			PR12B	3	C	
G14	NC	-			PR12A	3	T	
E16	NC	-			PR11B	3	C	
E15	NC	-			PR11A	3	T	
H12	PR9B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
GND	GND2	2			GND2			
G12	PR9A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
G13	PR8B	2	C		PR8B	2	C	
F13	PR8A	2	T		PR8A	2	T	
F12	PR7B	2	C		PR7B	2	C	
E13	PR7A	2	T		PR7A	2	T	
D16	PR6B	2	C		PR6B	2	C	
D15	PR6A	2	T	RDQS6	PR6A	2	T	RDQS6
F14	PR5B	2	C		PR5B	2	C	
E14	PR5A	2	T		PR5A	2	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
V12	PB16B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5
AB10	PB17A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB11	PB17B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0
Y12	PB18A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN
U11	PB18B	4	C	CS1N	U11	PB26B	4	C	CS1N	U11	PB26B	4	C	CS1N
W12	PB19A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4
U12	PB19B	4	C	CSN	U12	PB27B	4	C	CSN	U12	PB27B	4	C	CSN
W13	PB20A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4
U13	PB20B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7
AA12	PB21A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB12	PB21B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6
T13	PB22A	4	T	BDQS22	T13	PB30A	4	T	BDQS30	T13	PB30A	4	T	BDQS30
V13	PB22B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4
W14	PB23A	4	T		W14	PB31A	4	T		W14	PB31A	4	T	
U14	PB23B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3
Y13	PB24A	4	T		Y13	PB32A	4	T		Y13	PB32A	4	T	
V14	PB24B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2
AA13	PB25A	4	T		AA13	PB33A	4	T		AA13	PB33A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB13	PB25B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1
AA14	PB26A	4	T		AA14	PB34A	4	T		AA14	PB34A	4	T	
Y14	PB26B	4	C		Y14	PB34B	4	C		Y14	PB34B	4	C	
Y15	PB27A	4	T		Y15	PB35A	4	T		Y15	PB35A	4	T	
W15	PB27B	4	C		W15	PB35B	4	C		W15	PB35B	4	C	
V15	PB28A	4	T		V15	PB36A	4	T		V15	PB36A	4	T	
T14	PB28B	4	C		T14	PB36B	4	C		T14	PB36B	4	C	
AB14	PB29A	4	T		AB14	PB37A	4	T		AB14	PB37A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB15	PB29B	4	C		AB15	PB37B	4	C		AB15	PB37B	4	C	
AB16	PB30A	4	T	BDQS30	AB16	PB38A	4	T	BDQS38	AB16	PB38A	4	T	BDQS38
AA15	PB30B	4	C		AA15	PB38B	4	C		AA15	PB38B	4	C	
AB17	PB31A	4	T		AB17	PB39A	4	T		AB17	PB39A	4	T	
AA16	PB31B	4	C		AA16	PB39B	4	C		AA16	PB39B	4	C	
AB18	PB32A	4	T		AB18	PB40A	4	T		AB18	PB40A	4	T	
AA17	PB32B	4	C		AA17	PB40B	4	C		AA17	PB40B	4	C	
AB19	PB33A	4	T		AB19	PB41A	4	T		AB19	PB41A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA18	PB33B	4	C		AA18	PB41B	4	C		AA18	PB41B	4	C	
W16	NC	-			W16	NC	-			W16	PB42A	4	T	
U15	NC	-			U15	NC	-			U15	PB42B	4	C	
V16	NC	-			V16	NC	-			V16	PB43A	4	T	
U16	NC	-			U16	NC	-			U16	PB43B	4	C	
Y17	NC	-			Y17	NC	-			Y17	PB44A	4	T	
V17	NC	-			V17	NC	-			V17	PB44B	4	C	
AB20	NC	-			AB20	NC	-			AB20	PB45A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA19	NC	-			AA19	NC	-			AA19	PB45B	4	C	
Y16	NC	-			Y16	NC	-			Y16	PB46A	4	T	BDQS46

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
U9	PB20B	5	C		U9	PB20B	5	C	
Y8	PB21A	5	T		Y8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
Y9	PB21B	5	C		Y9	PB21B	5	C	
V9	PB22A	5	T	BDQS22	V9	PB22A	5	T	BDQS22
T9	PB22B	5	C		T9	PB22B	5	C	
W10	PB23A	5	T		W10	PB23A	5	T	
U10	PB23B	5	C		U10	PB23B	5	C	
V10	PB24A	5	T		V10	PB24A	5	T	
T10	PB24B	5	C		T10	PB24B	5	C	
AA6	PB25A	5	T		AA6	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AB5	PB25B	5	C		AB5	PB25B	5	C	
AA8	PB26A	5	T		AA8	PB26A	5	T	
AA7	PB26B	5	C		AA7	PB26B	5	C	
AB6	PB27A	5	T		AB6	PB27A	5	T	
AB7	PB27B	5	C		AB7	PB27B	5	C	
Y10	PB28A	5	T		Y10	PB28A	5	T	
W11	PB28B	5	C		W11	PB28B	5	C	
AB8	PB29A	5	T		AB8	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AB9	PB29B	5	C		AB9	PB29B	5	C	
AA10	PB30A	5	T	BDQS30	AA10	PB30A	5	T	BDQS30
AA9	PB30B	5	C		AA9	PB30B	5	C	
Y11	PB31A	5	T		Y11	PB31A	5	T	
AA11	PB31B	5	C		AA11	PB31B	5	C	
V11	PB32A	5	T	VREF2_5	V11	PB32A	5	T	VREF2_5
V12	PB32B	5	C	VREF1_5	V12	PB32B	5	C	VREF1_5
AB10	PB33A	5	T	PCLKT5_0	AB10	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AB11	PB33B	5	C	PCLKC5_0	AB11	PB33B	5	C	PCLKC5_0
Y12	PB34A	4	T	WRITEN	Y12	PB34A	4	T	WRITEN
U11	PB34B	4	C	CS1N	U11	PB34B	4	C	CS1N
W12	PB35A	4	T	VREF1_4	W12	PB35A	4	T	VREF1_4
U12	PB35B	4	C	CSN	U12	PB35B	4	C	CSN
W13	PB36A	4	T	VREF2_4	W13	PB36A	4	T	VREF2_4
U13	PB36B	4	C	D0/SPID7	U13	PB36B	4	C	D0/SPID7
AA12	PB37A	4	T	D2/SPID5	AA12	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AB12	PB37B	4	C	D1/SPID6	AB12	PB37B	4	C	D1/SPID6
T13	PB38A	4	T	BDQS38	T13	PB38A	4	T	BDQS38
V13	PB38B	4	C	D3/SPID4	V13	PB38B	4	C	D3/SPID4
W14	PB39A	4	T		W14	PB39A	4	T	
U14	PB39B	4	C	D4/SPID3	U14	PB39B	4	C	D4/SPID3

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFEC20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF4	PB13B	5	C		AF4	PB13B	5	C	
AE5	PB14A	5	T	BDQS14	AE5	PB14A	5	T	BDQS14
AA9	PB14B	5	C		AA9	PB14B	5	C	
AF5	PB15A	5	T		AF5	PB15A	5	T	
Y10	PB15B	5	C		Y10	PB15B	5	C	
AD6	PB16A	5	T		AD6	PB16A	5	T	
AC10	PB16B	5	C		AC10	PB16B	5	C	
AF6	PB17A	5	T		AF6	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AE6	PB17B	5	C		AE6	PB17B	5	C	
AF7	PB18A	5	T		AF7	PB18A	5	T	
AB10	PB18B	5	C		AB10	PB18B	5	C	
AE7	PB19A	5	T		AE7	PB19A	5	T	
AD10	PB19B	5	C		AD10	PB19B	5	C	
AD7	PB20A	5	T		AD7	PB20A	5	T	
AA10	PB20B	5	C		AA10	PB20B	5	C	
AF8	PB21A	5	T		AF8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
AF9	PB21B	5	C		AF9	PB21B	5	C	
AD11	PB22A	5	T	BDQS22	AD11	PB22A	5	T	BDQS22
Y11	PB22B	5	C		Y11	PB22B	5	C	
AE8	PB23A	5	T		AE8	PB23A	5	T	
AC11	PB23B	5	C		AC11	PB23B	5	C	
AF10	PB24A	5	T		AF10	PB24A	5	T	
AB11	PB24B	5	C		AB11	PB24B	5	C	
AE10	PB25A	5	T		AE10	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AE9	PB25B	5	C		AE9	PB25B	5	C	
AA11	PB26A	5	T		AA11	PB26A	5	T	
Y12	PB26B	5	C		Y12	PB26B	5	C	
AE11	PB27A	5	T		AE11	PB27A	5	T	
AF11	PB27B	5	C		AF11	PB27B	5	C	
AF12	PB28A	5	T		AF12	PB28A	5	T	
AE12	PB28B	5	C		AE12	PB28B	5	C	
AD12	PB29A	5	T		AD12	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AC12	PB29B	5	C		AC12	PB29B	5	C	
AA12	PB30A	5	T	BDQS30	AA12	PB30A	5	T	BDQS30
AB12	PB30B	5	C		AB12	PB30B	5	C	
AE13	PB31A	5	T		AE13	PB31A	5	T	
AF13	PB31B	5	C		AF13	PB31B	5	C	
AD13	PB32A	5	T	VREF2_5	AD13	PB32A	5	T	VREF2_5

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A5	PT13B	0	C		A5	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
A4	PT13A	0	T		A4	PT13A	0	T	
F9	PT12B	0	C		F9	PT12B	0	C	
B6	PT12A	0	T		B6	PT12A	0	T	
E9	PT11B	0	C		E9	PT11B	0	C	
C8	PT11A	0	T		C8	PT11A	0	T	
G8	PT10B	0	C		G8	PT10B	0	C	
B5	PT10A	0	T		B5	PT10A	0	T	
A3	PT9B	0	C		A3	PT9B	0	C	
GND	GND0	0			GND	GND0	0		
A2	PT9A	0	T		A2	PT9A	0	T	
F8	PT8B	0	C		F8	PT8B	0	C	
B4	PT8A	0	T		B4	PT8A	0	T	
E8	PT7B	0	C		E8	PT7B	0	C	
B3	PT7A	0	T		B3	PT7A	0	T	
D8	PT6B	0	C		D8	PT6B	0	C	
G7	PT6A	0	T	TDQS6	G7	PT6A	0	T	TDQS6
C4	PT5B	0	C		C4	PT5B	0	C	
C5	PT5A	0	T		C5	PT5A	0	T	
E7	PT4B	0	C		E7	PT4B	0	C	
D4	PT4A	0	T		D4	PT4A	0	T	
F7	PT3B	0	C		F7	PT3B	0	C	
D6	PT3A	0	T		D6	PT3A	0	T	
D7	PT2B	0	C		D7	PT2B	0	C	
E6	PT2A	0	T		E6	PT2A	0	T	
GND	GND0	0			GND	GND0	0		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K15	GND	-			K15	GND	-		
K16	GND	-			K16	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-		
L15	GND	-			L15	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		

LatticeEC Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFEC10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFEC10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFEC10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFEC15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFEC15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFEC20E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	19.7K
LFEC20E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K
LFEC33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFEC33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K