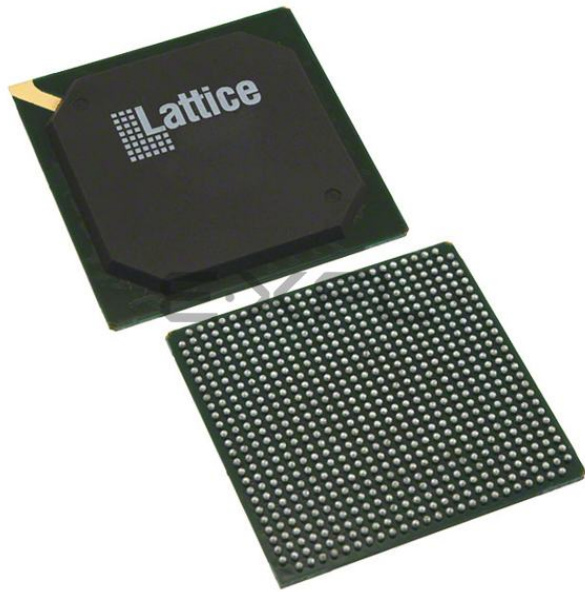




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	32800
Total RAM Bits	434176
Number of I/O	496
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp33e-4fn672c

Features

■ Extensive Density and Package Options

- 1.5K to 32.8K LUT4s
- 65 to 496 I/Os
- Density migration supported

■ sysDSP™ Block (LatticeECP™ Versions)

- High performance multiply and accumulate
- 4 to 8 blocks
 - 4 to 8 36x36 multipliers or
 - 16 to 32 18x18 multipliers or
 - 32 to 64 9x9 multipliers

■ Embedded and Distributed Memory

- 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
- Up to 131 Kbits distributed RAM
- Flexible memory resources:
 - Distributed and block memory

■ Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:

- LVCMOS 3.3/2.5/1.8/1.5/1.2
- LVTTTL
- SSTL 3/2 Class I, II, SSTL18 Class I
- HSTL 18 Class I, II, III, HSTL15 Class I, III
- PCI
- LVDS, Bus-LVDS, LVPECL, RSDS

■ Dedicated DDR Memory Support

- Implements interface up to DDR400 (200MHz)

■ sysCLOCK™ PLLs

- Up to four analog PLLs per device
- Clock multiply, divide and phase shifting

■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- SPI boot flash interface
- 1.2V power supply

■ Low Cost FPGA

- Features optimized for mainstream applications
- Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFCEP6	LFEC10/ LFCEP10	LFEC15/ LFCEP15	LFEC20/ LFCEP20	LFEC33/ LFCEP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks ¹	—	—	4	5	6	7	8
18x18 Multipliers ¹	—	—	16	20	24	28	32
V _{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

1. LatticeECP devices only.

Figure 2-8. Per Quadrant Primary Clock Selection

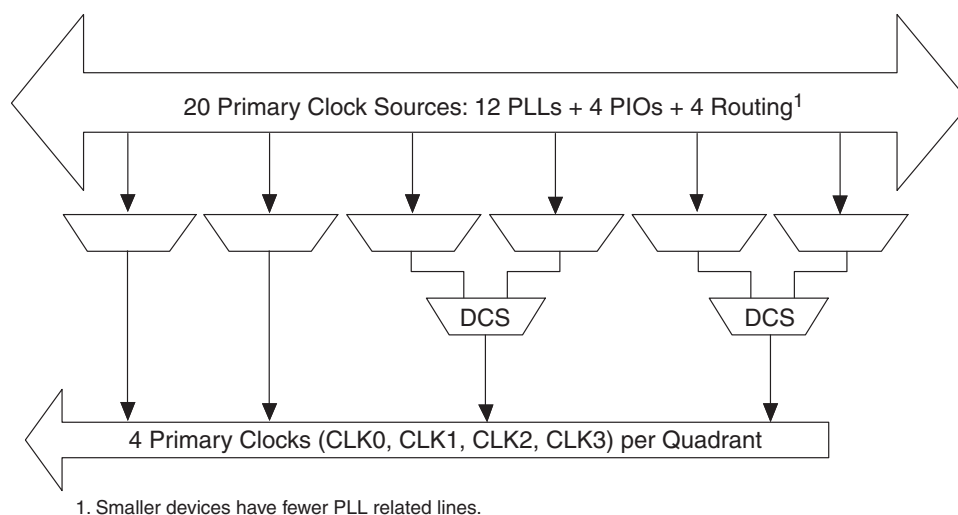


Figure 2-9. Per Quadrant Secondary Clock Selection

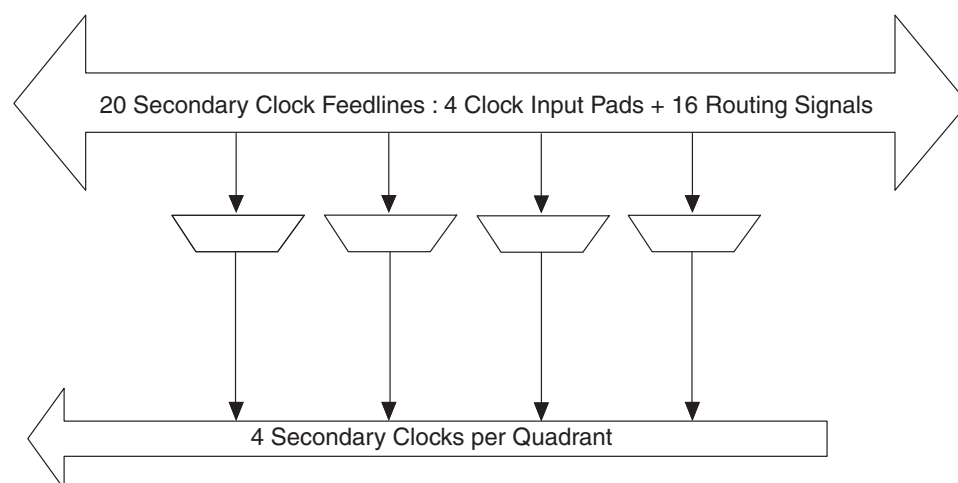
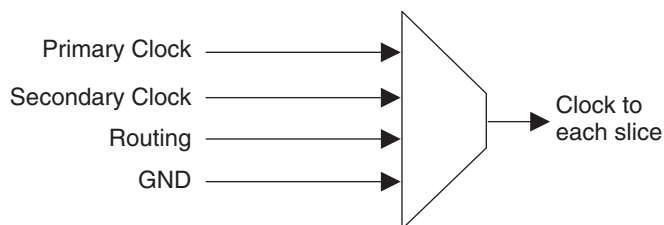


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

Figure 2-13. DCS Block Primitive

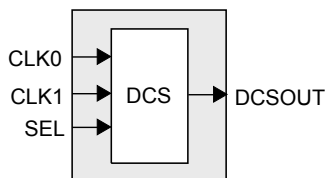
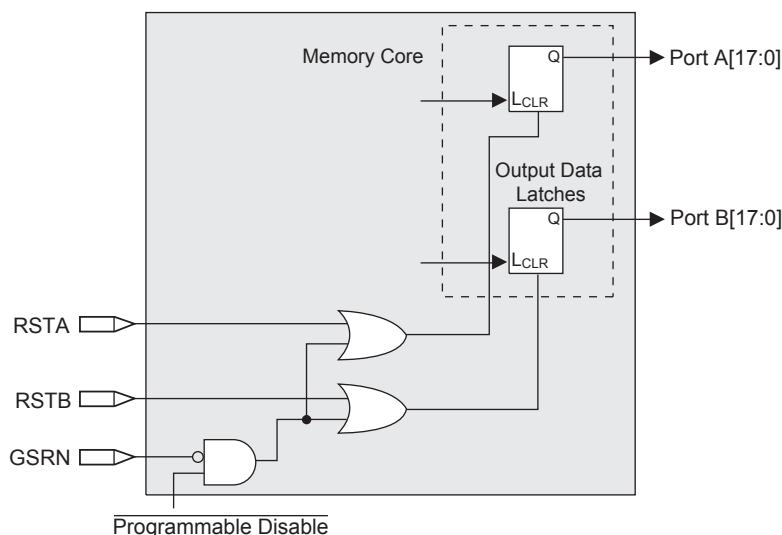


Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Figure 2-16. Memory Core Reset

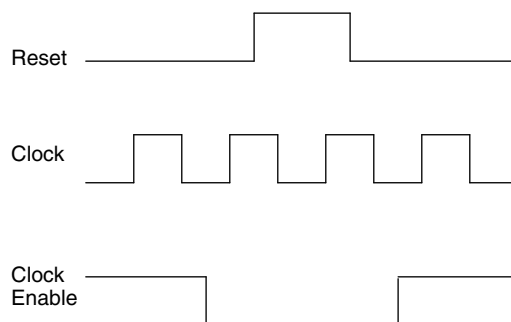


For further information about sysMEM EBR block, please see the the list of technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-17. The GSR input to the EBR is always asynchronous.

Figure 2-17. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP Block

The LatticeECP-DSP family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP/EC devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeECP/EC sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}^1 (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33 ²	—	—
LVCMOS25 ²	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12 ²	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL, BLVDS, RSDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.

2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ} .

LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

Figure 3-14. sysCONFIG Master Serial Port Timing

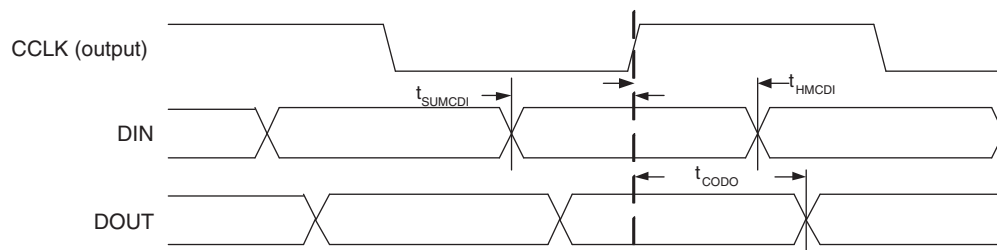


Figure 3-15. sysCONFIG Slave Serial Port Timing

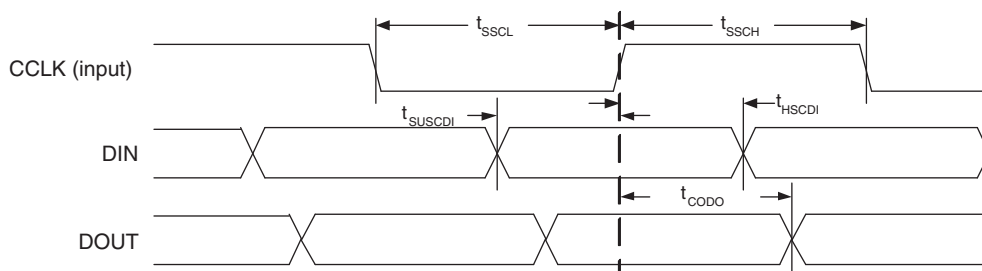
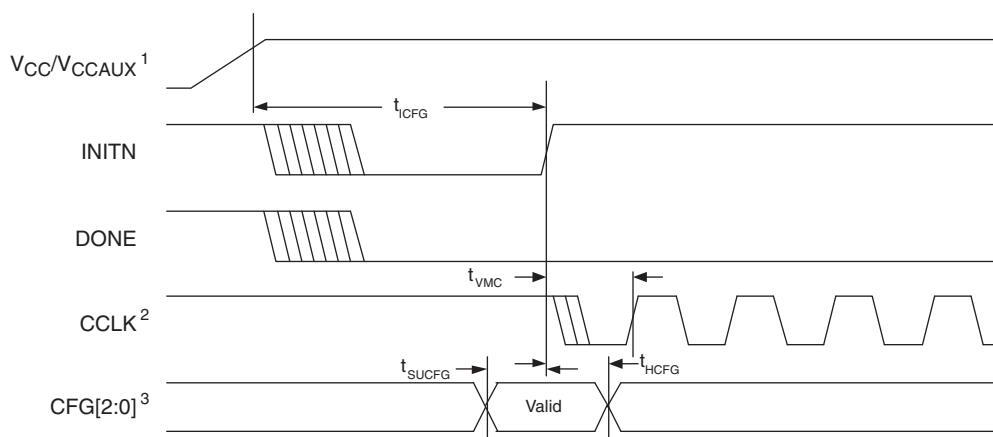
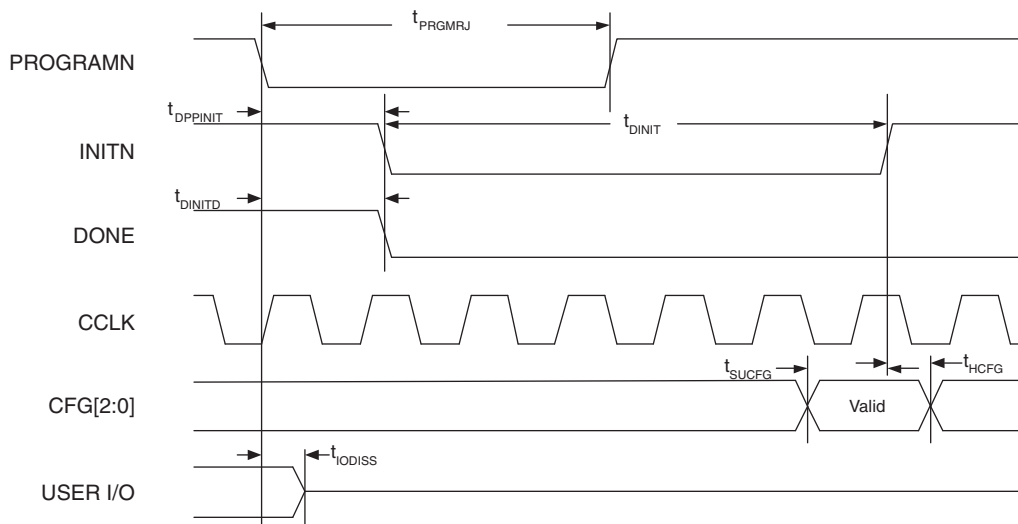


Figure 3-16. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX} , whichever is the last to reach its V_{MIN} .
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

Figure 3-17. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-18. Wake-Up Timing

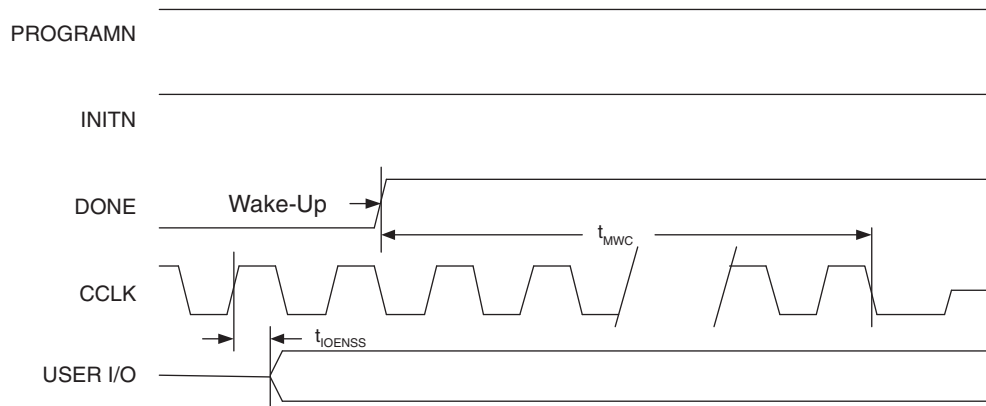
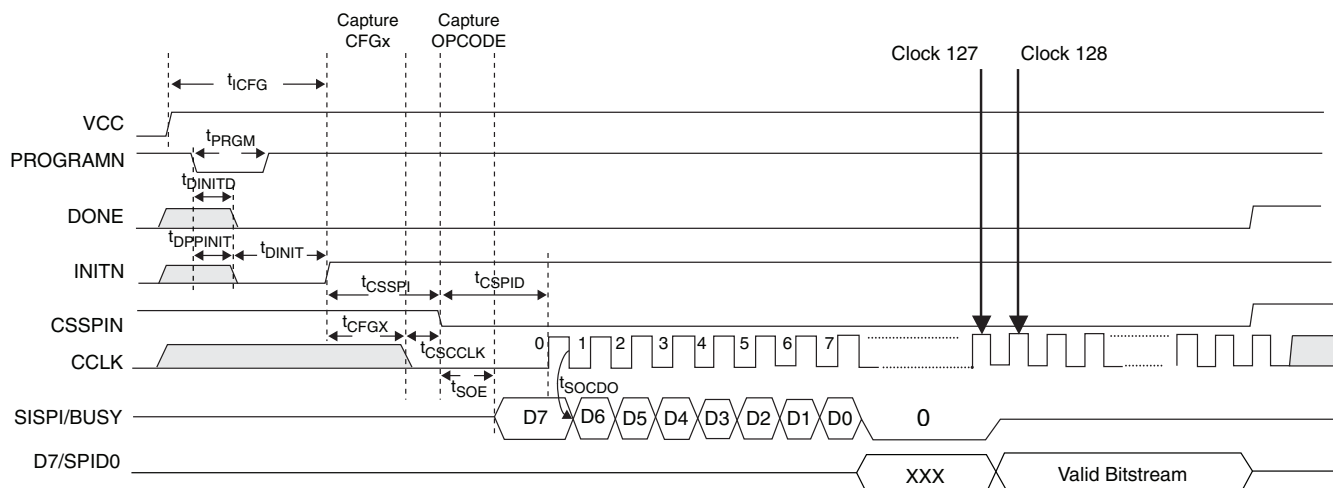


Figure 3-19. sysCONFIG SPI Port Sequence



Pin Information Summary (Cont.)

		LFEC/EC15		LFEC/EC20		LFEC/EC33	
Pin Type		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V _{CC}		10	20	20	32	16	28
V _{CCAUX}		2	12	12	20	12	20
V _{CCPLL}		0	0	0	0	4	4
V _{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V _{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
41	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
42	PB11B	4	C	CSN	PB19B	4	C	CSN
43	PB12B	4		D0/SPID7	PB20B	4		D0/SPID7
44	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
45	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
46	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
47	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
48	PB15B	4		D4/SPID3	PB23B	4		D4/SPID3
49	PB16B	4		D5/SPID2	PB24B	4		D5/SPID2
50	PB17B	4		D6/SPID1	PB25B	4		D6/SPID1
51*	GND3 GND4	-			GND3 GND4	-		
52	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
53	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
54	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
55	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
56	VCCIO3	3			VCCIO3	3		
57	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
58	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
59	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
60	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
61	CFG2	3			CFG2	3		
62	CFG1	3			CFG1	3		
63	CFG0	3			CFG0	3		
64	VCC	-			VCC	-		
65	PROGRAMN	3			PROGRAMN	3		
66	CCLK	3			CCLK	3		
67	INITN	3			INITN	3		
68	GND	-			GND	-		
69	DONE	3			DONE	3		
70	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
71	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
72	PR2B	2		VREF1_2	PR2B	2		VREF1_2
73	VCCIO2	2			VCCIO2	2		
74	GND2	2			GND2	2		
75	PT17B	1	C		PT25B	1	C	
76	PT17A	1	T		PT25A	1	T	
77	PT14B	1	C		PT22B	1	C	
78	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
79	PT13A	1			PT21A	1		
80	PT12B	1	C		PT20B	1	C	
81	PT12A	1	T		PT20A	1	T	

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N7	PB18B	5	C		PB18B	5	C	
R7	PB19A	5	T		PB19A	5	T	
R8	PB19B	5	C		PB19B	5	C	
M7	PB20A	5	T		PB20A	5	T	
M8	PB20B	5	C		PB20B	5	C	
T8	PB21A	5	T		PB21A	5	T	
GND	GND5	5			GND5	5		
T9	PB21B	5	C		PB21B	5	C	
P8	PB22A	5	T	BDQS22	PB22A	5	T	BDQS22
N8	PB22B	5	C		PB22B	5	C	
R9	PB23A	5	T		PB23A	5	T	
R10	PB23B	5	C		PB23B	5	C	
P9	PB24A	5	T	VREF2_5	PB24A	5	T	VREF2_5
N9	PB24B	5	C	VREF1_5	PB24B	5	C	VREF1_5
T10	PB25A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB25B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
T12	PB26A	4	T	WRITEN	PB26A	4	T	WRITEN
T13	PB26B	4	C	CS1N	PB26B	4	C	CS1N
P10	PB27A	4	T	VREF1_4	PB27A	4	T	VREF1_4
N10	PB27B	4	C	CSN	PB27B	4	C	CSN
T14	PB28A	4	T	VREF2_4	PB28A	4	T	VREF2_4
T15	PB28B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
M10	PB29A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB29B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
R11	PB30A	4	T	BDQS30	PB30A	4	T	BDQS30
P11	PB30B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
R13	PB31A	4	T		PB31A	4	T	
R14	PB31B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
P12	PB32A	4	T		PB32A	4	T	
P13	PB32B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
N11	PB33A	4	T		PB33A	4	T	
GND	GND4	4			GND4	4		
N12	PB33B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
R12	PB34A	4			PB34A	4		
GND	GND4	4			GND4	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR36B	3	C	VREF2_3	PR44B	3	C	VREF2_3
N14	PR36A	3	T	VREF1_3	PR44A	3	T	VREF1_3

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA

LFEC6/LFEC6					LFEC6/EC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
C3	NC	-			C3	PL3A	7	T		C3	PL3A	7	T	
B2	NC	-			B2	PL3B	7	C		B2	PL3B	7	C	
E5	NC	-			E5	PL4A	7	T		E5	PL4A	7	T	
F5	NC	-			F5	PL4B	7	C		F5	PL4B	7	C	
D3	NC	-			D3	PL5A	7	T		D3	PL5A	7	T	
C2	NC	-			C2	PL5B	7	C		C2	PL5B	7	C	
F4	NC	-			F4	PL6A	7	T	LDQS6	F4	PL6A	7	T	LDQS6
G4	NC	-			G4	PL6B	7	C		G4	PL6B	7	C	
E3	NC	-			E3	PL7A	7	T		E3	PL7A	7	T	
D2	NC	-			D2	PL7B	7	C		D2	PL7B	7	C	
B1	NC	-			B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL8A	7	T	LUM0_PLLT_IN_A
C1	NC	-			C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL8B	7	C	LUM0_PLLC_IN_A
F3	NC	-			F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL9A	7	T	LUM0_PLLT_FB_A
GND	-	-			GND	GND7	7			GND	GND7	7		
E2	NC	-			E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL9B	7	C	LUM0_PLLC_FB_A
G5	NC	-			G5	NC	-			G5	PL11A	7	T	
H6	NC	-			H6	NC	-			H6	PL11B	7	C	
G3	NC	-			G3	NC	-			G3	PL12A	7	T	
H4	NC	-			H4	NC	-			H4	PL12B	7	C	
J5	NC	-			J5	NC	-			J5	PL13A	7	T	
H5	NC	-			H5	NC	-			H5	PL13B	7	C	
F2	NC	-			F2	NC	-			F2	PL14A	7	T	
GND	-	-			GND	-	-			GND	GND7	7		
F1	NC	-			F1	NC	-			F1	PL14B	7	C	
E1	NC	-			E1	PL11A	7	T		E1	PL15A	7	T	
D1	NC	-			D1	PL11B	7	C		D1	PL15B	7	C	
H3	PL3A	7	T		H3	PL12A	7	T		H3	PL16A	7	T	
G2	PL3B	7	C		G2	PL12B	7	C		G2	PL16B	7	C	
H2	PL4A	7	T		H2	PL13A	7	T		H2	PL17A	7	T	
G1	PL4B	7	C		G1	PL13B	7	C		G1	PL17B	7	C	
J4	PL5A	7	T		J4	PL14A	7	T		J4	PL18A	7	T	
GND	-	-			GND	GND7	7			GND	GND7	7		
J3	PL5B	7	C		J3	PL14B	7	C		J3	PL18B	7	C	
J2	PL6A	7	T	LDQS6	J2	PL15A	7	T	LDQS15	J2	PL19A	7	T	LDQS19
H1	PL6B	7	C		H1	PL15B	7	C		H1	PL19B	7	C	
K4	PL7A	7	T		K4	PL16A	7	T		K4	PL20A	7	T	
K5	PL7B	7	C		K5	PL16B	7	C		K5	PL20B	7	C	
K3	PL8A	7	T		K3	PL17A	7	T		K3	PL21A	7	T	
K2	PL8B	7	C		K2	PL17B	7	C		K2	PL21B	7	C	
J1	PL9A	7	T	PCLKT7_0	J1	PL18A	7	T	PCLKT7_0	J1	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7			GND	GND7	7		
K1	PL9B	7	C	PCLKC7_0	K1	PL18B	7	C	PCLKC7_0	K1	PL22B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6			L3	XRES	6		
L4	PL11A	6	T		L4	PL20A	6	T		L4	PL24A	6	T	
L5	PL11B	6	C		L5	PL20B	6	C		L5	PL24B	6	C	
L2	PL12A	6	T		L2	PL21A	6	T		L2	PL25A	6	T	
L1	PL12B	6	C		L1	PL21B	6	C		L1	PL25B	6	C	

LFEC6P/EC6, LFEC6P/EC10, LFEC6P/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6P/EC6					LFEC6P/EC10					LFEC6P/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFEC6/EC6, LFEC6/EC10, LFEC6/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC6/LFEC6					LFEC10/LFEC10					LFEC6/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLT_FB_A	C22	PR9A	2	T	RUM0_PLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLT_IN_A	G18	PR8A	2	T	RUM0_PLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
V2	PL41B	6	C	LLM0_PLLC_IN_A	V2	PL53B	6	C	LLM0_PLLC_IN_A
U3	PL42A	6	T	LLM0_PLLT_FB_A	U3	PL54A	6	T	LLM0_PLLT_FB_A
V3	PL42B	6	C	LLM0_PLLC_FB_A	V3	PL54B	6	C	LLM0_PLLC_FB_A
U4	PL43A	6	T		U4	PL55A	6	T	
V5	PL43B	6	C		V5	PL55B	6	C	
W1	PL44A	6	T		W1	PL56A	6	T	
GND	GND6	6			GND	GND6	6		
W2	PL44B	6	C		W2	PL56B	6	C	
Y1	PL45A	6	T	LDQS45	Y1	PL57A	6	T	LDQS57
Y2	PL45B	6	C		Y2	PL57B	6	C	
AA1	PL46A	6	T		AA1	PL58A	6	T	
AA2	PL46B	6	C		AA2	PL58B	6	C	
W4	PL47A	6	T		W4	PL59A	6	T	
V4	PL47B	6	C		V4	PL59B	6	C	
W3	PL48A	6	T	VREF1_6	W3	PL68A	6	T	VREF1_6
Y3	PL48B	6	C	VREF2_6	Y3	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND6	6		
GND	-				GND	GND6	6		
GND	-				GND	GND5	5		
GND	GND5	5			GND	GND5	5		
V7	PB10A	5	T		V7	PB10A	5	T	
T6	PB10B	5	C		T6	PB10B	5	C	
V8	PB11A	5	T		V8	PB11A	5	T	
U7	PB11B	5	C		U7	PB11B	5	C	
W5	PB12A	5	T		W5	PB12A	5	T	
U6	PB12B	5	C		U6	PB12B	5	C	
AA3	PB13A	5	T		AA3	PB13A	5	T	
GND	GND5	5			GND	GND5	5		
AB3	PB13B	5	C		AB3	PB13B	5	C	
Y6	PB14A	5	T	BDQS14	Y6	PB14A	5	T	BDQS14
V6	PB14B	5	C		V6	PB14B	5	C	
AA5	PB15A	5	T		AA5	PB15A	5	T	
W6	PB15B	5	C		W6	PB15B	5	C	
Y5	PB16A	5	T		Y5	PB16A	5	T	
Y4	PB16B	5	C		Y4	PB16B	5	C	
AA4	PB17A	5	T		AA4	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AB4	PB17B	5	C		AB4	PB17B	5	C	
Y7	PB18A	5	T		Y7	PB18A	5	T	
W8	PB18B	5	C		W8	PB18B	5	C	
W7	PB19A	5	T		W7	PB19A	5	T	
U8	PB19B	5	C		U8	PB19B	5	C	
W9	PB20A	5	T		W9	PB20A	5	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF22	PB51A	4	T		AF22	PB51A	4	T	
AB17	PB51B	4	C		AB17	PB51B	4	C	
AE22	PB52A	4	T		AE22	PB52A	4	T	
AA18	PB52B	4	C		AA18	PB52B	4	C	
AE19	PB53A	4	T		AE19	PB53A	4	T	
GND	GND4	4			GND	GND4	4		
AE20	PB53B	4	C		AE20	PB53B	4	C	
AA19	PB54A	4	T	BDQS54	AA19	PB54A	4	T	BDQS54
Y18	PB54B	4	C		Y18	PB54B	4	C	
AF23	PB55A	4	T		AF23	PB55A	4	T	
AA20	PB55B	4	C		AA20	PB55B	4	C	
AC18	PB56A	4	T		AC18	PB56A	4	T	
AB18	PB56B	4	C		AB18	PB56B	4	C	
AF24	PB57A	4	T		AF24	PB57A	4	T	
-	-	-			GND	GND4	4		
AE23	PB57B	4	C		AE23	PB57B	4	C	
AD19	NC	-			AD19	PB58A	4	T	
AD20	NC	-			AD20	PB58B	4	C	
AC19	NC	-			AC19	PB59A	4	T	
AB19	NC	-			AB19	PB59B	4	C	
AD21	NC	-			AD21	PB60A	4	T	
AC20	NC	-			AC20	PB60B	4	C	
AF25	NC	-			AF25	PB61A	4	T	
-	-	-			GND	GND4	4		
AE25	NC	-			AE25	PB61B	4	C	
AB21	NC	-			AB21	PB62A	4	T	BDQS62
AB20	NC	-			AB20	PB62B	4	C	
AE24	NC	-			AE24	PB63A	4	T	
AD23	NC	-			AD23	PB63B	4	C	
AD22	NC	-			AD22	PB64A	4	T	
AC21	NC	-			AC21	PB64B	4	C	
AC22	NC	-			AC22	PB65A	4	T	
AB22	NC	-			AB22	PB65B	4	C	
GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3		
AC23	PR48B	3	C	VREF2_3	AC23	PR68B	3	C	VREF2_3
AC24	PR48A	3	T	VREF1_3	AC24	PR68A	3	T	VREF1_3
AD24	NC	-			AD24	PR67B	3	C	
AD25	NC	-			AD25	PR67A	3	T	
AE26	NC	-			AE26	PR66B	3	C	
AD26	NC	-			AD26	PR66A	3	T	
Y20	NC	-			Y20	PR65B	3	C	

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

Conventional Packaging
LatticeEC Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208C	112	-3	PQFP	208	COM	1.5K
LFEC1E-4Q208C	112	-4	PQFP	208	COM	1.5K
LFEC1E-5Q208C	112	-5	PQFP	208	COM	1.5K
LFEC1E-3T144C	97	-3	TQFP	144	COM	1.5K
LFEC1E-4T144C	97	-4	TQFP	144	COM	1.5K
LFEC1E-5T144C	97	-5	TQFP	144	COM	1.5K
LFEC1E-3T100C	67	-3	TQFP	100	COM	1.5K
LFEC1E-4T100C	67	-4	TQFP	100	COM	1.5K
LFEC1E-5T100C	67	-5	TQFP	100	COM	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256C	160	-3	fpBGA	256	COM	3.1K
LFEC3E-4F256C	160	-4	fpBGA	256	COM	3.1K
LFEC3E-5F256C	160	-5	fpBGA	256	COM	3.1K
LFEC3E-3Q208C	145	-3	PQFP	208	COM	3.1K
LFEC3E-4Q208C	145	-4	PQFP	208	COM	3.1K
LFEC3E-5Q208C	145	-5	PQFP	208	COM	3.1K
LFEC3E-3T144C	97	-3	TQFP	144	COM	3.1K
LFEC3E-4T144C	97	-4	TQFP	144	COM	3.1K
LFEC3E-5T144C	97	-5	TQFP	144	COM	3.1K
LFEC3E-3T100C	67	-3	TQFP	100	COM	3.1K
LFEC3E-4T100C	67	-4	TQFP	100	COM	3.1K
LFEC3E-5T100C	67	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFEC6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFEC6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFEC6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFEC6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFEC6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFEC6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFEC6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFEC6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFEC6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFEC6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFEC6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFEC10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFEC10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFEC10E-3F256C	195	-3	fpBGA	256	COM	10.2K

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFCEP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFCEP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFCEP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFCEP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFCEP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFCEP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFCEP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFCEP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFCEP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFCEP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFCEP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFCEP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFCEP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFCEP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFCEP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFCEP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFCEP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFCEP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFCEP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFCEP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFCEP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFCEP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFCEP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFCEP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFCEP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFCEP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFCEP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFCEP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFCEP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFCEP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFCEP33E-5F672C	496	-5	fpBGA	672	COM	32.8K