Lattice Semiconductor Corporation - LFECP33E-5FN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	32800
Total RAM Bits	434176
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp33e-5fn484c

Figure 2-1. Simplified Block Diagram, LatticeEC Device (Top Level)

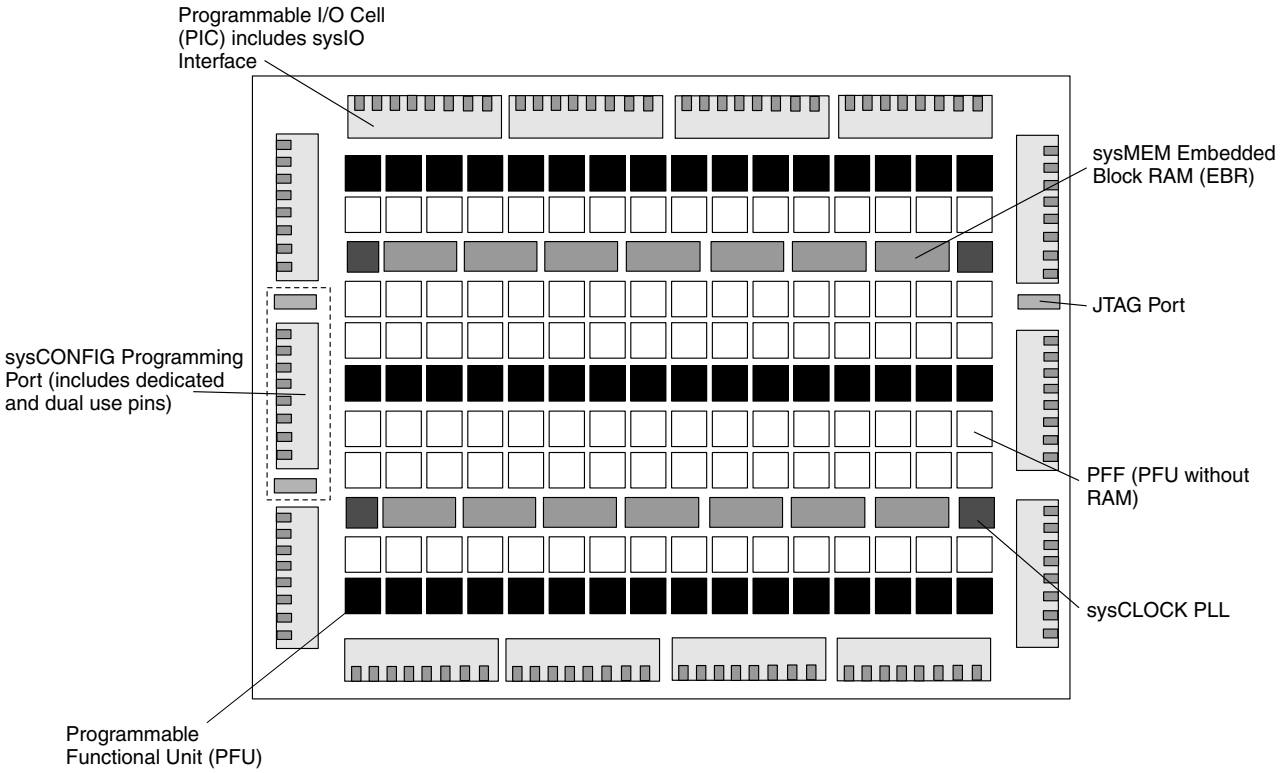
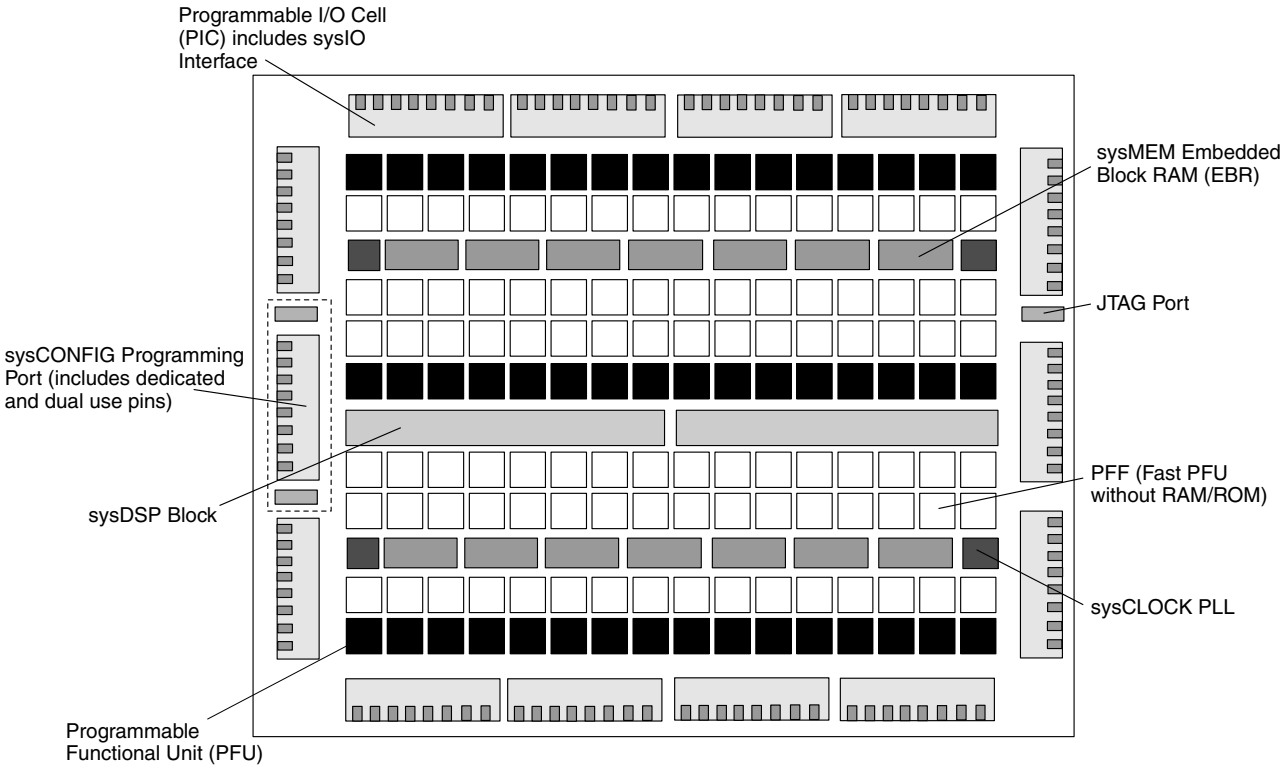


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)



IPexpress™

The user can access the sysDSP block via the IPexpress configuration tool, included with the ispLEVER design tool suite. IPexpress has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
LFECP6	4	32	16	4
LFECP10	5	40	20	5
LFECP15	6	48	24	6
LFECP20	7	56	28	7
LFECP33	8	64	32	8

Table 2-10. Embedded SRAM in LatticeECP Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LFECP6	10	92
LFECP10	30	276
LFECP15	38	350
LFECP20	46	424
LFECP33	54	498

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

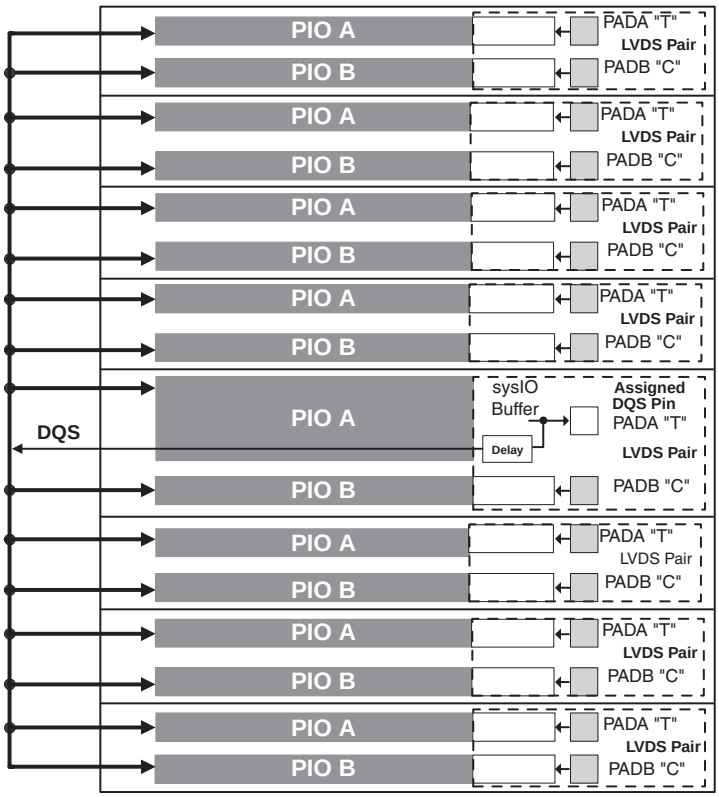
Table 2-11. DSP Block Performance of LatticeECP Family

Device	DSP Block	DSP Performance MMAC
LFECP6	4	3680
LFECP10	5	4600
LFECP15	6	5520
LFECP20	7	6440
LFECP33	8	7360

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Figure 2-27. Input Register DDR Waveforms

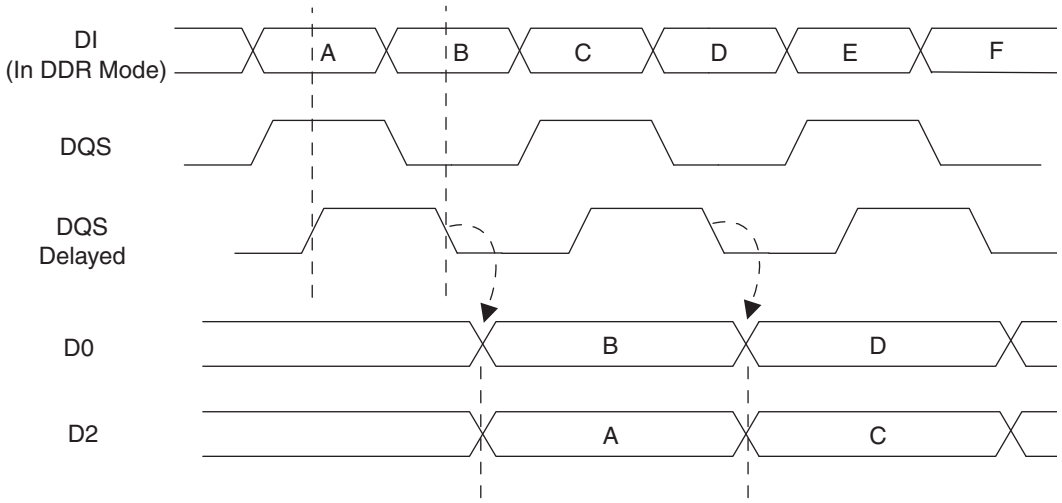
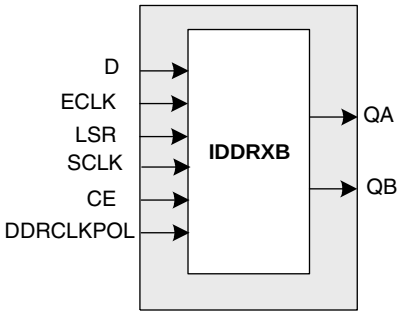


Figure 2-28. INDDRXB Primitive



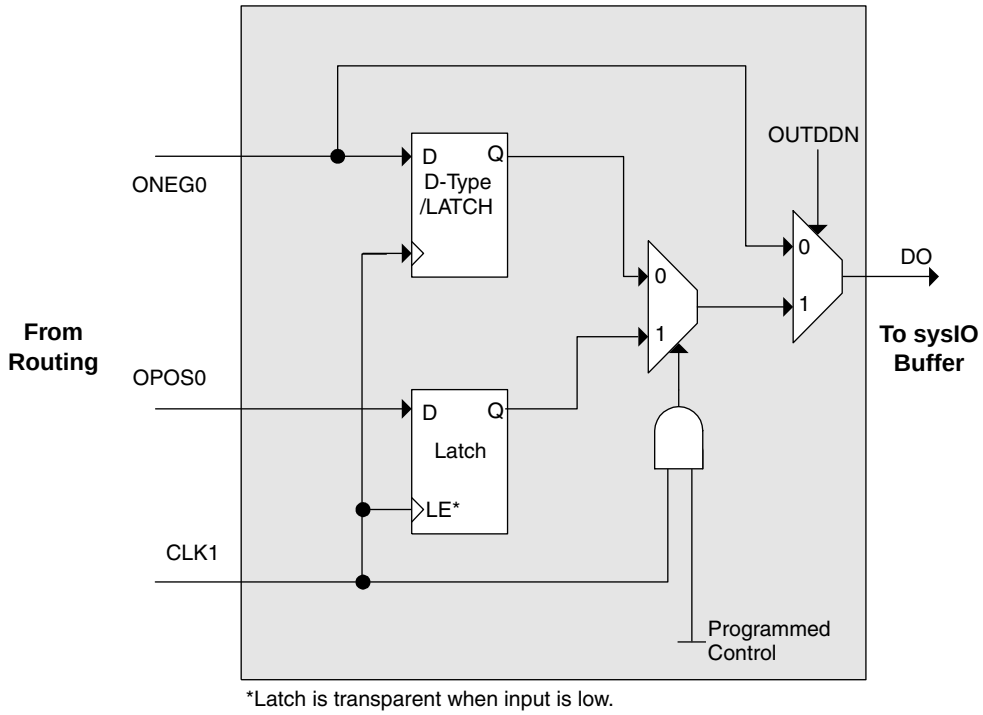
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

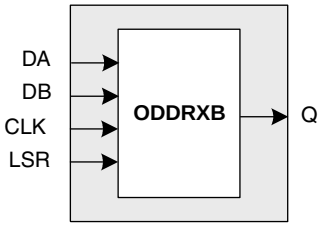
Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-29. Output Register Block



*Latch is transparent when input is low.

Figure 2-30. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.90	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—

1. Outputs are implemented with the addition of external resistors. V_{CCIO} applies to outputs only.

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold		+/-100	—	—	mV
V_{CM}	Input common mode voltage	100mV ð V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ð V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ð V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

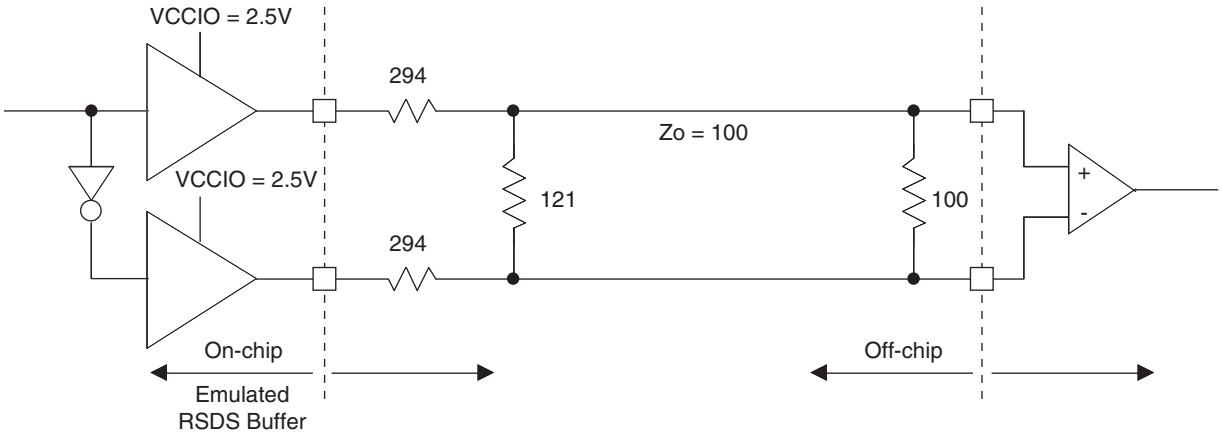


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohm
R_S	Driver series resistor	294	ohm
R_P	Driver parallel resistor	121	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohm
I_{DC}	DC output current	3.66	mA

LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
sysCONFIG Byte Data Flow					
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7		—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	1		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7		—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		12	ns
t_{CORD}	Clock to Out for Read Data	—		12	ns
sysCONFIG Byte Slave Clocking					
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6		—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	9		—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15		—	ns
t_{SUSCDI}	Din Setup time to CCLK Slave Mode	7		—	ns
t_{HSCDI}	Din Hold Time to CCLK Slave Mode	1		—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—		12	ns
sysCONFIG Serial (Bit) Data Flow					
t_{SUMCDI}	Din Setup time to CCLK Master Mode	7		—	ns
t_{HMCDI}	Din Hold Time to CCLK Master Mode	1		—	ns
sysCONFIG Serial Slave Clocking					
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6		—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6		—	ns
sysCONFIG POR, Initialization and Wake Up					
t_{ICFG}	Minimum Vcc to INIT High	—		50	ms
t_{VMC}	Time from tICFG to Valid Master Clock	—		2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—		8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25		—	ns
t_{DINIT}	INIT Low Time	—		1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—		37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—		37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake Up Sequence	—		25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120		—	cycles
t_{SUCFG}	CFG to INITN Setup Time	100		—	ns
t_{HCFG}	CFG to INITN Hold Time	100		—	ns
sysCONFIG SPI Port					
t_{CFGX}	Init High to CCLK Low	—		80	ns
t_{CSSPI}	Init High to CSSPIN Low	—		2	us
t_{CSCCLK}	CCLK Low Before CSSPIN Low	0		-	ns
t_{SOCDO}	CCLK Low to Output Valid	—		15	ns

Power Supply and NC Connections

Signals	100 TQFP	144 TQFP	208 PQFP	256 fpBGA
VCC	12, 64	**EC1, EC3:** 13, 92, 99 **ECP/EC6:** 11, 13, 92, 99	**EC1, EC3:** 26, 128, 135 **ECP/EC6:** 24, 26, 128, 135 **ECP/EC10:** 5, 24, 26, 128, 135, 152	E12, E5, E8, M12, M5, M9, F6, F11, L11, L6
VCCIO0	100	136, 143	**EC1:** 187, 208 **EC3, ECP/EC6, ECP/EC10:** 187, 197, 208	F7, F8
VCCIO1	86	110, 125	157, 176	F9, F10
VCCIO2	73	108	**EC1:** 155 **EC3, ECP/EC6, ECP/EC10:** 145, 155	G11, H11
VCCIO3	56	73, 84	106, 120	J11, K11
VCCIO4	38	55, 71	85, 104	L9, L10
VCCIO5	26	38, 44	**EC1:** 53, 74 **EC2, ECP/EC6, ECP/EC10:** 53, 64, 74	L7, L8
VCCIO6	24	24, 36	37, 51	J6, K6
VCCIO7	2	1	**EC1:** 2 **EC3, ECP/EC6, ECP/EC10:** 2, 13	G6, H6
VCCJ	18	19	32	L4
VCCAUX	37, 87	54, 126	**EC1:** 84, 177 **EC3, ECP/EC6, ECP/EC10:** 22, 84, 136, 177	B15, R2
VCCPLL	—	—	—	—
GND, GND0-GND7	1, 14, 25, 35, 51, 68, 74, 89	**EC1, EC3:** 15, 28, 37, 52, 63, 72, 80, 96, 98, 109, 117, 128, 144 **ECP/EC6:** 12, 15, 28, 37, 52, 63, 72, 80, 96, 98, 109, 117, 128, 144	**EC1:** 1, 28, 41, 52, 82, 93, 105, 116, 132, 134, 156, 168, 179 **EC3:** 1, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 156, 168, 179, 189 **ECP/EC6:** 1, 18, 25, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 156, 168, 179, 189 ECP/EC10: 1, 6, 18, 25, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 151, 156, 168, 179, 189	A1, A16, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, T1, T16
NC	—	**EC1, EC3:** 11, 12 **ECP6/EC6:** None	**EC1:** 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 18, 22, 24, 25, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 72, 103, 136, 138, 144, 145, 146, 147, 148, 149, 150, 151, 152, 158, 189, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207 **EC3:** 5, 6, 18, 24, 25, 103, 151, 152, 158 **ECP/EC6:** 5, 6, 151, 152 **ECP/EC10:** None	**EC3:** G5, H5, F2, F1, H4, H3, G2, G1, J4, J3, J5, K5, H2, H1, J2, J1, R12, H16, H15, G16, G15, K12, J12, J14, J15, F16, F15, J13, H13, H14, G14, E16, E15, B13, C13 **ECP/EC10:** None **ECP/EC15:** None

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
41	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
42	PB11B	4	C	CSN	PB19B	4	C	CSN
43	PB12B	4		D0/SPID7	PB20B	4		D0/SPID7
44	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
45	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
46	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
47	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
48	PB15B	4		D4/SPID3	PB23B	4		D4/SPID3
49	PB16B	4		D5/SPID2	PB24B	4		D5/SPID2
50	PB17B	4		D6/SPID1	PB25B	4		D6/SPID1
51*	GND3 GND4	-			GND3 GND4	-		
52	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
53	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
54	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
55	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
56	VCCIO3	3			VCCIO3	3		
57	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
58	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
59	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
60	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
61	CFG2	3			CFG2	3		
62	CFG1	3			CFG1	3		
63	CFG0	3			CFG0	3		
64	VCC	-			VCC	-		
65	PROGRAMN	3			PROGRAMN	3		
66	CCLK	3			CCLK	3		
67	INITN	3			INITN	3		
68	GND	-			GND	-		
69	DONE	3			DONE	3		
70	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
71	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
72	PR2B	2		VREF1_2	PR2B	2		VREF1_2
73	VCCIO2	2			VCCIO2	2		
74	GND2	2			GND2	2		
75	PT17B	1	C		PT25B	1	C	
76	PT17A	1	T		PT25A	1	T	
77	PT14B	1	C		PT22B	1	C	
78	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
79	PT13A	1			PT21A	1		
80	PT12B	1	C		PT20B	1	C	
81	PT12A	1	T		PT20A	1	T	

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
169	PT21A	1	T		PT29A	1	T	
170	PT20B	1	C		PT28B	1	C	
171	PT20A	1	T		PT28A	1	T	
172	PT19B	1	C	VREF2_1	PT27B	1	C	VREF2_1
173	PT19A	1	T	VREF1_1	PT27A	1	T	VREF1_1
174	PT18B	1	C		PT26B	1	C	
175	PT18A	1	T		PT26A	1	T	
176	VCCIO1	1			VCCIO1	1		
177	VCCAUX	-			VCCAUX	-		
178	PT17B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
179	GND0	0			GND0	0		
180	PT17A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
181	PT16B	0	C	VREF1_0	PT24B	0	C	VREF1_0
182	PT16A	0	T	VREF2_0	PT24A	0	T	VREF2_0
183	PT15B	0	C		PT23B	0	C	
184	PT15A	0	T		PT23A	0	T	
185	PT14B	0	C		PT22B	0	C	
186	PT14A	0	T	TDQS14	PT22A	0	T	TDQS22
187	VCCIO0	0			VCCIO0	0		
188	PT13B	0	C		PT21B	0	C	
189	GND0	0			GND0	0		
190	PT13A	0	T		PT21A	0	T	
191	PT12B	0	C		PT20B	0	C	
192	PT12A	0	T		PT20A	0	T	
193	PT11B	0	C		PT19B	0	C	
194	PT11A	0	T		PT19A	0	T	
195	PT10B	0	C		PT18B	0	C	
196	PT10A	0	T		PT18A	0	T	
197	VCCIO0	0			VCCIO0	0		
198	PT6B	0	C		PT6B	0	C	
199	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
200	PT5B	0	C		PT5B	0	C	
201	PT5A	0	T		PT5A	0	T	
202	PT4B	0	C		PT4B	0	C	
203	PT4A	0	T		PT4A	0	T	
204	PT3B	0	C		PT3B	0	C	
205	PT3A	0	T		PT3A	0	T	
206	PT2B	0	C		PT2B	0	C	
207	PT2A	0	T		PT2A	0	T	
208	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
C3	PL3A	7	T		PL3A	7	T	
C2	PL3B	7	C		PL3B	7	C	
B1	PL4A	7	T		PL4A	7	T	
C1	PL4B	7	C		PL4B	7	C	
E3	PL5A	7	T		PL5A	7	T	
E4	PL5B	7	C		PL5B	7	C	
F4	PL6A	7	T	LDQS6	PL6A	7	T	LDQS6
F5	PL6B	7	C		PL6B	7	C	
G4	PL7A	7	T		PL7A	7	T	
G3	PL7B	7	C		PL7B	7	C	
D2	PL8A	7	T		PL8A	7	T	
D1	PL8B	7	C		PL8B	7	C	
E1	PL9A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL9B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	NC	-			PL11A	6	T	
H5	NC	-			PL11B	6	C	
F2	NC	-			PL12A	6	T	
F1	NC	-			PL12B	6	C	
H4	NC	-			PL13A	6	T	
H3	NC	-			PL13B	6	C	
G2	NC	-			PL14A	6	T	
-	-	-			GND6	6		
G1	NC	-			PL14B	6	C	
J4	NC	-			PL15A	6	T	LDQS15
J3	NC	-			PL15B	6	C	
J5	NC	-			PL16A	6	T	
K5	NC	-			PL16B	6	C	
H2	NC	-			PL17A	6	T	
H1	NC	-			PL17B	6	C	
J2	NC	-			PL18A	6	T	
-	-	-			GND6	6		
J1	NC	-			PL18B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		
L3	TMS	6			TMS	6		
L5	TDO	6			TDO	6		
L4	VCCJ	6			VCCJ	6		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
A10	PT25B	0	C	PCLKC0_0	PT25B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT25A	0	T	PCLKT0_0	PT25A	0	T	PCLKT0_0
C9	PT24B	0	C	VREF1_0	PT24B	0	C	VREF1_0
B9	PT24A	0	T	VREF2_0	PT24A	0	T	VREF2_0
E9	PT23B	0	C		PT23B	0	C	
D9	PT23A	0	T		PT23A	0	T	
D8	PT22B	0	C		PT22B	0	C	
C8	PT22A	0	T	TDQS22	PT22A	0	T	TDQS22
A9	PT21B	0	C		PT21B	0	C	
GND	GND0	0			GND0	0		
A8	PT21A	0	T		PT21A	0	T	
B8	PT20B	0	C		PT20B	0	C	
B7	PT20A	0	T		PT20A	0	T	
D7	PT19B	0	C		PT19B	0	C	
C7	PT19A	0	T		PT19A	0	T	
A7	PT18B	0	C		PT18B	0	C	
A6	PT18A	0	T		PT18A	0	T	
E7	PT17B	0	C		PT17B	0	C	
GND	GND0	0			GND0	0		
E6	PT17A	0	T		PT17A	0	T	
D6	PT16B	0	C		PT16B	0	C	
C6	PT16A	0	T		PT16A	0	T	
B6	PT15B	0	C		PT15B	0	C	
B5	PT15A	0	T		PT15A	0	T	
A5	PT14B	0	C		PT14B	0	C	
A4	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A3	PT13B	0	C		PT13B	0	C	
-	GND0	0			GND0	0		
A2	PT13A	0	T		PT13A	0	T	
B2	PT12B	0	C		PT12B	0	C	
B3	PT12A	0	T		PT12A	0	T	
D5	PT11B	0	C		PT11B	0	C	
C5	PT11A	0	T		PT11A	0	T	
C4	PT10B	0	C		PT10B	0	C	
B4	PT10A	0	T		PT10A	0	T	
GND	GND0	0			GND0	0		
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W17	NC	-			W17	NC	-			W17	PB46B	4	C	
AA20	NC	-			AA20	NC	-			AA20	PB47A	4	T	
Y19	NC	-			Y19	NC	-			Y19	PB47B	4	C	
Y18	NC	-			Y18	NC	-			Y18	PB48A	4	T	
W18	NC	-			W18	NC	-			W18	PB48B	4	C	
T17	NC	-			T17	NC	-			T17	PB49A	4	T	
U17	NC	-			U17	NC	-			U17	PB49B	4	C	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3			GND	GND3	3		
W20	PR27B	3	C	VREF2_3	W20	PR36B	3	C	VREF2_3	W20	PR44B	3	C	VREF2_3
Y20	PR27A	3	T	VREF1_3	Y20	PR36A	3	T	VREF1_3	Y20	PR44A	3	T	VREF1_3
AA21	PR26B	3	C		AA21	PR35B	3	C		AA21	PR43B	3	C	
AB21	PR26A	3	T		AB21	PR35A	3	T		AB21	PR43A	3	T	
W19	PR25B	3	C		W19	PR34B	3	C		W19	PR42B	3	C	
V19	PR25A	3	T		V19	PR34A	3	T		V19	PR42A	3	T	
Y21	PR24B	3	C		Y21	PR33B	3	C		Y21	PR41B	3	C	
AA22	PR24A	3	T	RDQS24	AA22	PR33A	3	T	RDQS33	AA22	PR41A	3	T	RDQS41
V20	PR23B	3	C	RLM0_PLLC_FB_A	V20	PR32B	3	C	RLM0_PLLC_FB_A	V20	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND	GND3	3			GND	GND3	3		
U20	PR23A	3	T	RLM0_PLLT_FB_A	U20	PR32A	3	T	RLM0_PLLT_FB_A	U20	PR40A	3	T	RLM0_PLLT_FB_A
W21	PR22B	3	C	RLM0_PLLC_IN_A	W21	PR31B	3	C	RLM0_PLLC_IN_A	W21	PR39B	3	C	RLM0_PLLC_IN_A
Y22	PR22A	3	T	RLM0_PLLT_IN_A	Y22	PR31A	3	T	RLM0_PLLT_IN_A	Y22	PR39A	3	T	RLM0_PLLT_IN_A
V21	PR21B	3	C	DI/CSSPIN	V21	PR30B	3	C	DI/CSSPIN	V21	PR38B	3	C	DI/CSSPIN
W22	PR21A	3	T	DOUT/CSON	W22	PR30A	3	T	DOUT/CSON	W22	PR38A	3	T	DOUT/CSON
U21	PR20B	3	C	BUSY/SISPI	U21	PR29B	3	C	BUSY/SISPI	U21	PR37B	3	C	BUSY/SISPI
V22	PR20A	3	T	D7/SPID0	V22	PR29A	3	T	D7/SPID0	V22	PR37A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3			R20	DONE	3		
T18	NC	-			T18	NC	-			T18	NC	-		
R17	NC	-			R17	NC	-			R17	NC	-		
R19	NC	-			R19	NC	-			R19	NC	-		
R18	NC	-			R18	NC	-			R18	NC	-		
U22	NC	-			U22	NC	-			U22	PR35B	3	C	
GND	-	-			GND	-	-			GND	GND3	3		
T22	NC	-			T22	NC	-			T22	PR35A	3	T	
R21	NC	-			R21	NC	-			R21	PR34B	3	C	
R22	NC	-			R22	NC	-			R22	PR34A	3	T	
P20	NC	-			P20	NC	-			P20	PR33B	3	C	
N20	NC	-			N20	NC	-			N20	PR33A	3	T	
P19	NC	-			P19	NC	-			P19	PR32B	3	C	
P18	NC	-			P18	NC	-			P18	PR32A	3	T	
P21	PR18B	3	C		P21	PR27B	3	C		P21	PR31B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
P22	PR18A	3	T		P22	PR27A	3	T		P22	PR31A	3	T	
N21	PR17B	3	C		N21	PR26B	3	C		N21	PR30B	3	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF4	PB13B	5	C		AF4	PB13B	5	C	
AE5	PB14A	5	T	BDQS14	AE5	PB14A	5	T	BDQS14
AA9	PB14B	5	C		AA9	PB14B	5	C	
AF5	PB15A	5	T		AF5	PB15A	5	T	
Y10	PB15B	5	C		Y10	PB15B	5	C	
AD6	PB16A	5	T		AD6	PB16A	5	T	
AC10	PB16B	5	C		AC10	PB16B	5	C	
AF6	PB17A	5	T		AF6	PB17A	5	T	
GND	GND5	5			GND	GND5	5		
AE6	PB17B	5	C		AE6	PB17B	5	C	
AF7	PB18A	5	T		AF7	PB18A	5	T	
AB10	PB18B	5	C		AB10	PB18B	5	C	
AE7	PB19A	5	T		AE7	PB19A	5	T	
AD10	PB19B	5	C		AD10	PB19B	5	C	
AD7	PB20A	5	T		AD7	PB20A	5	T	
AA10	PB20B	5	C		AA10	PB20B	5	C	
AF8	PB21A	5	T		AF8	PB21A	5	T	
GND	GND5	5			GND	GND5	5		
AF9	PB21B	5	C		AF9	PB21B	5	C	
AD11	PB22A	5	T	BDQS22	AD11	PB22A	5	T	BDQS22
Y11	PB22B	5	C		Y11	PB22B	5	C	
AE8	PB23A	5	T		AE8	PB23A	5	T	
AC11	PB23B	5	C		AC11	PB23B	5	C	
AF10	PB24A	5	T		AF10	PB24A	5	T	
AB11	PB24B	5	C		AB11	PB24B	5	C	
AE10	PB25A	5	T		AE10	PB25A	5	T	
GND	GND5	5			GND	GND5	5		
AE9	PB25B	5	C		AE9	PB25B	5	C	
AA11	PB26A	5	T		AA11	PB26A	5	T	
Y12	PB26B	5	C		Y12	PB26B	5	C	
AE11	PB27A	5	T		AE11	PB27A	5	T	
AF11	PB27B	5	C		AF11	PB27B	5	C	
AF12	PB28A	5	T		AF12	PB28A	5	T	
AE12	PB28B	5	C		AE12	PB28B	5	C	
AD12	PB29A	5	T		AD12	PB29A	5	T	
GND	GND5	5			GND	GND5	5		
AC12	PB29B	5	C		AC12	PB29B	5	C	
AA12	PB30A	5	T	BDQS30	AA12	PB30A	5	T	BDQS30
AB12	PB30B	5	C		AB12	PB30B	5	C	
AE13	PB31A	5	T		AE13	PB31A	5	T	
AF13	PB31B	5	C		AF13	PB31B	5	C	
AD13	PB32A	5	T	VREF2_5	AD13	PB32A	5	T	VREF2_5

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
D13	PT32B	0	C	VREF1_0	D13	PT32B	0	C	VREF1_0
C13	PT32A	0	T	VREF2_0	C13	PT32A	0	T	VREF2_0
A13	PT31B	0	C		A13	PT31B	0	C	
B13	PT31A	0	T		B13	PT31A	0	T	
F13	PT30B	0	C		F13	PT30B	0	C	
F12	PT30A	0	T	TDQS30	F12	PT30A	0	T	TDQS30
A12	PT29B	0	C		A12	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
B12	PT29A	0	T		B12	PT29A	0	T	
A11	PT28B	0	C		A11	PT28B	0	C	
B11	PT28A	0	T		B11	PT28A	0	T	
D12	PT27B	0	C		D12	PT27B	0	C	
C12	PT27A	0	T		C12	PT27A	0	T	
B10	PT26B	0	C		B10	PT26B	0	C	
A10	PT26A	0	T		A10	PT26A	0	T	
G12	PT25B	0	C		G12	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
A9	PT25A	0	T		A9	PT25A	0	T	
E12	PT24B	0	C		E12	PT24B	0	C	
B9	PT24A	0	T		B9	PT24A	0	T	
F11	PT23B	0	C		F11	PT23B	0	C	
A8	PT23A	0	T		A8	PT23A	0	T	
D11	PT22B	0	C		D11	PT22B	0	C	
C11	PT22A	0	T	TDQS22	C11	PT22A	0	T	TDQS22
B8	PT21B	0	C		B8	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
B7	PT21A	0	T		B7	PT21A	0	T	
E11	PT20B	0	C		E11	PT20B	0	C	
A7	PT20A	0	T		A7	PT20A	0	T	
G11	PT19B	0	C		G11	PT19B	0	C	
C7	PT19A	0	T		C7	PT19A	0	T	
G10	PT18B	0	C		G10	PT18B	0	C	
C6	PT18A	0	T		C6	PT18A	0	T	
C10	PT17B	0	C		C10	PT17B	0	C	
GND	GND0	0			GND	GND0	0		
D10	PT17A	0	T		D10	PT17A	0	T	
F10	PT16B	0	C		F10	PT16B	0	C	
A6	PT16A	0	T		A6	PT16A	0	T	
E10	PT15B	0	C		E10	PT15B	0	C	
C9	PT15A	0	T		C9	PT15A	0	T	
G9	PT14B	0	C		G9	PT14B	0	C	
D9	PT14A	0	T	TDQS14	D9	PT14A	0	T	TDQS14

LatticeECP Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP20E-3FN672I	400	-3	Lead-Free fpBGA	672	IND	19.7K
LFECP20E-4FN672I	400	-4	Lead-Free fpBGA	672	IND	19.7K
LFECP20E-3FN484I	400	-3	Lead-Free fpBGA	484	IND	19.7K
LFECP20E-4FN484I	400	-4	Lead-Free fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN672I	496	-3	Lead-Free fpBGA	672	IND	32.8K
LFECP33E-4FN672I	496	-4	Lead-Free fpBGA	672	IND	32.8K
LFECP33E-3FN484I	360	-3	Lead-Free fpBGA	484	IND	32.8K
LFECP33E-4FN484I	360	-4	Lead-Free fpBGA	484	IND	32.8K

LatticeECP/EC Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: ww.pcisig.com