Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6100 |
| Total RAM Bits | 94208 |
| Number of I/O | 195 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp6e-3fn256i |

# Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (EConomy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (EConomy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (EConomy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

*Figure 2-4. Slice Diagram*

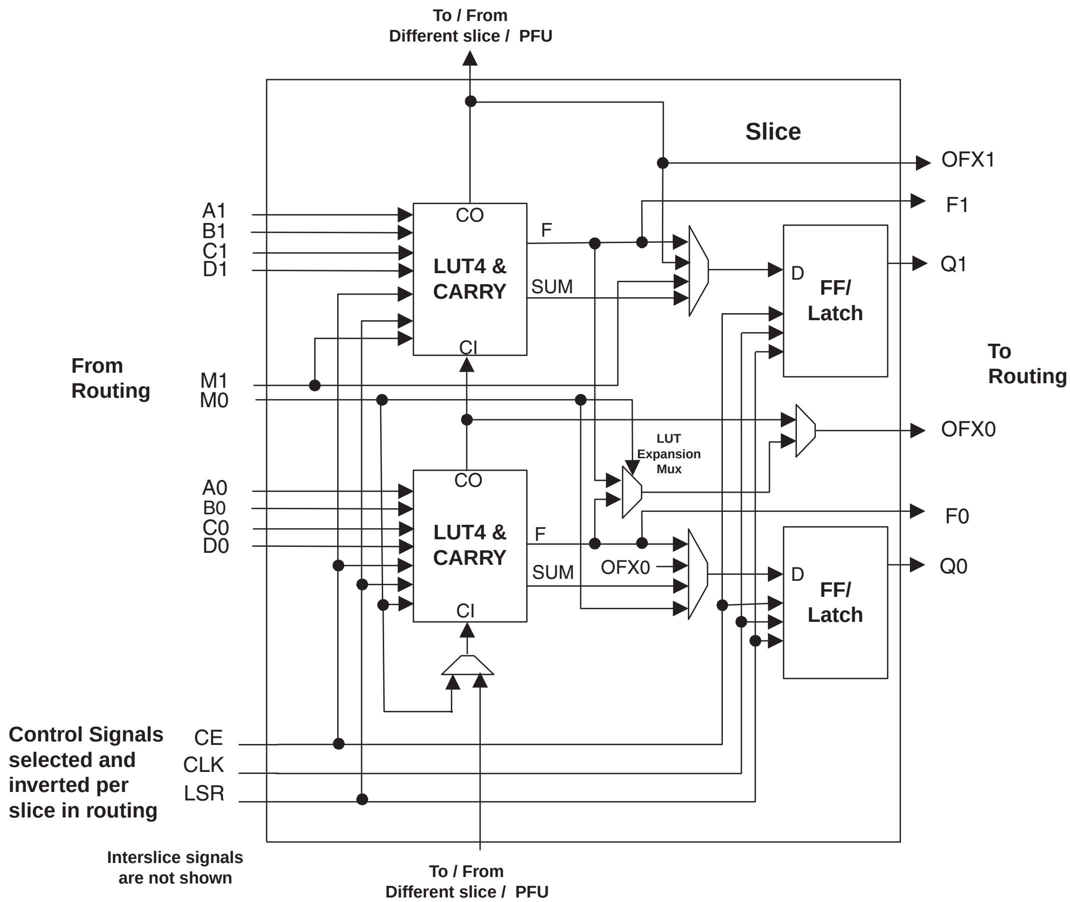



*Table 2-1. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

### Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

***Table 2-2. Slice Modes***

| | Logic | Ripple | RAM | ROM |
|---|---|---|---|---|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SPR16x2 | ROM16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A | ROM16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

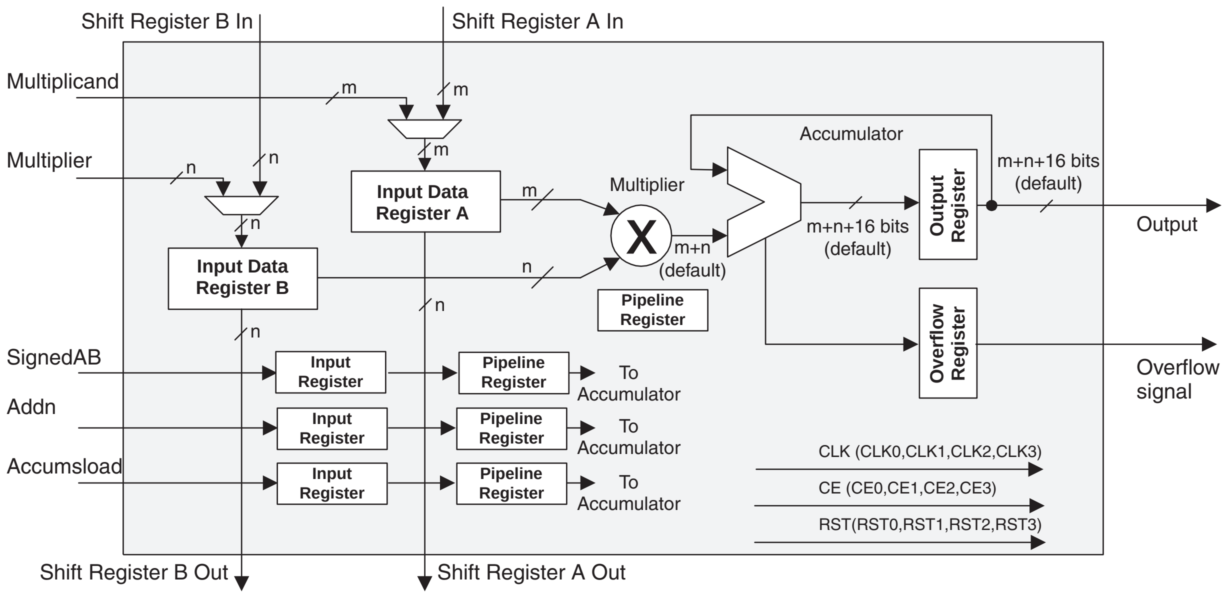
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information about using RAM in LatticeECP/EC devices, please see the list of technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

*Figure 2-20. MAC sysDSP Element*




## MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-21 shows the MULTADD sysDSP element.

*Figure 2-21. MULTADD*

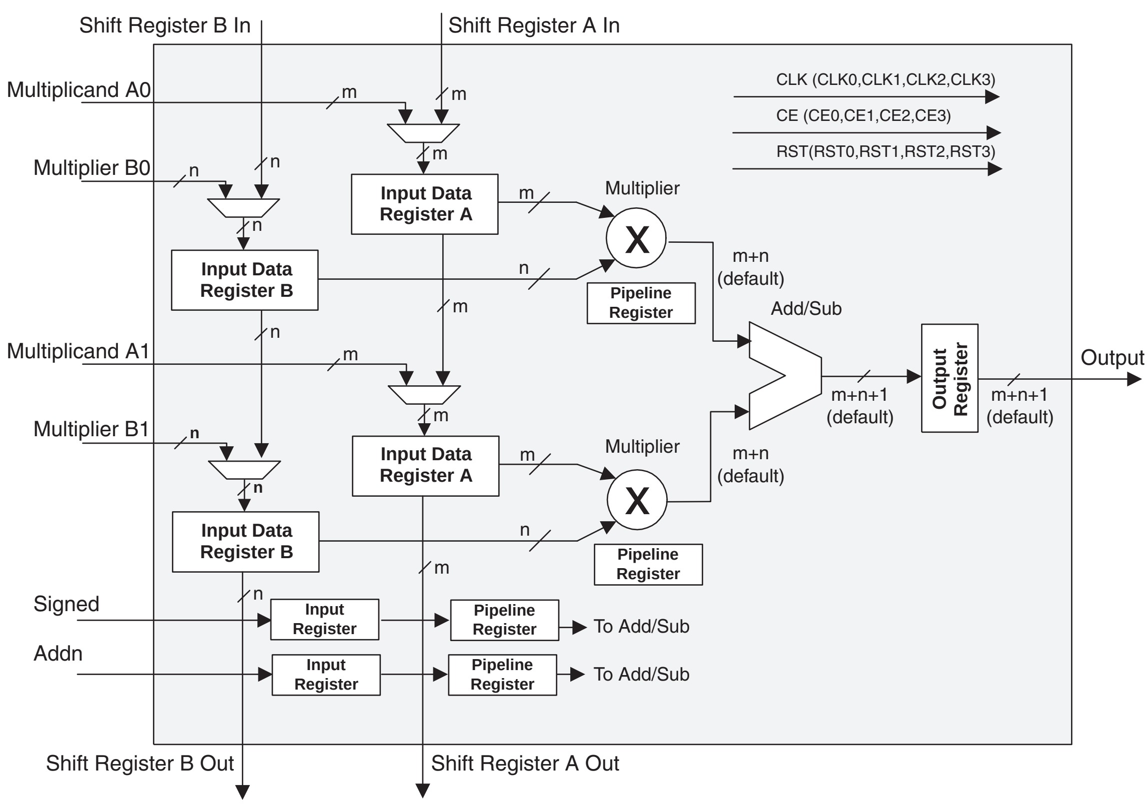


*Figure 2-27. Input Register DDR Waveforms*

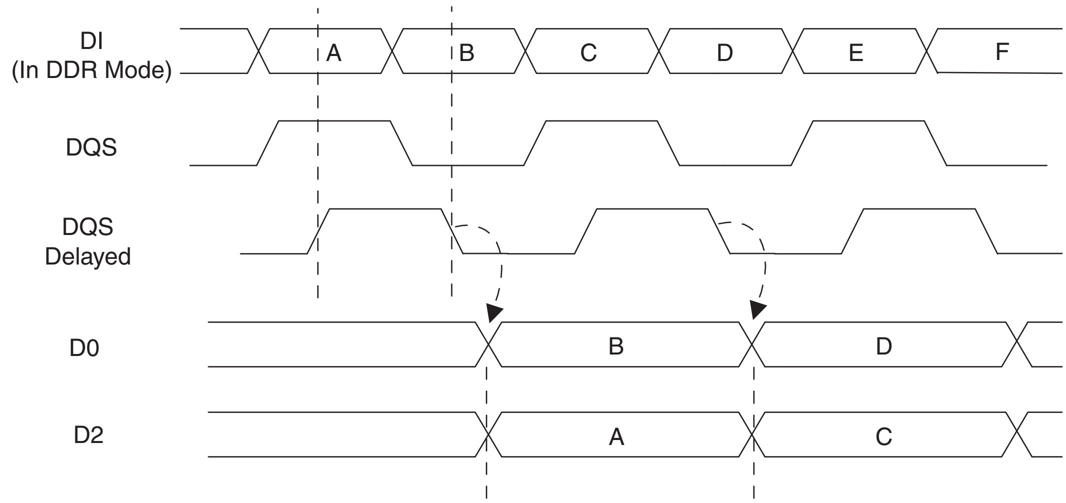
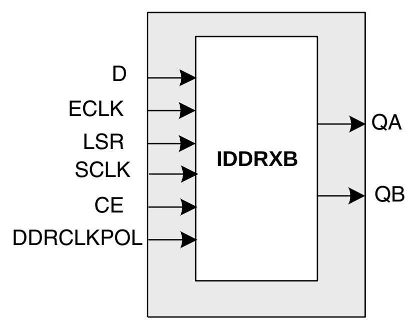



*Figure 2-28. INDDRXB Primitive*



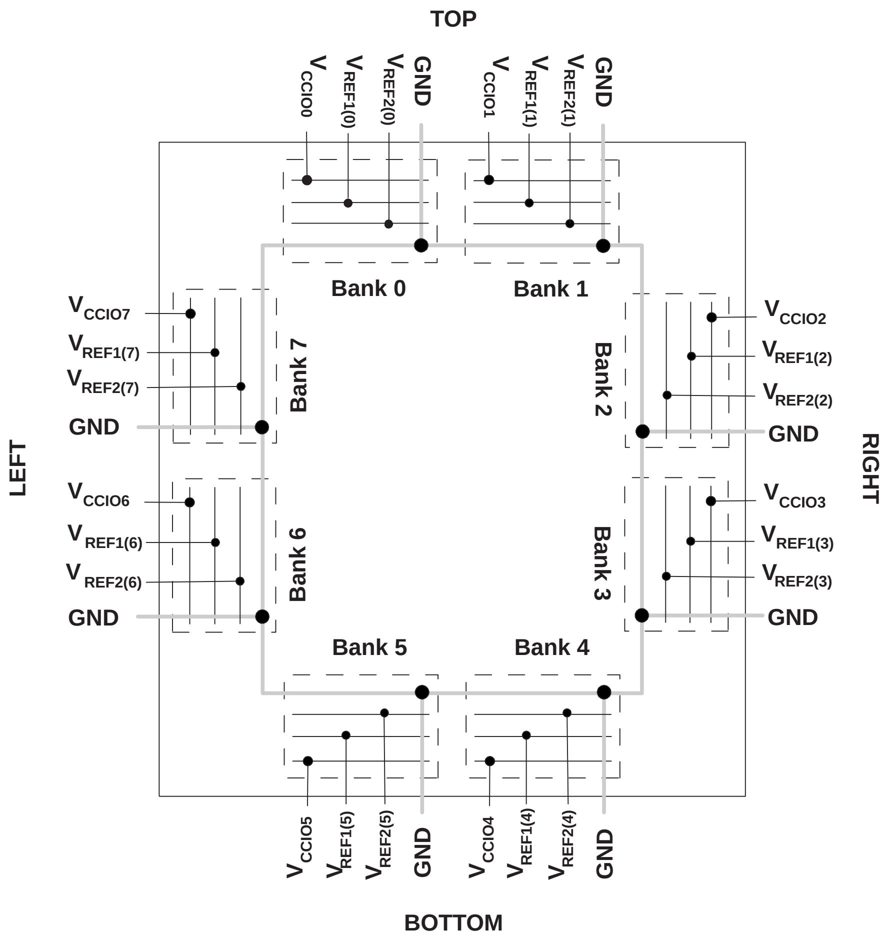

**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

*Figure 2-34. LatticeECP/EC Banks*




LatticeECP/EC devices contain two types of sysI/O buffer pairs.

1. **Top and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have programmable PCI clamps. These I/O banks also support hot socketing with IDK less than 1mA. Note that the PCI clamp is enabled after $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

2. **Left and Right sysI/O Buffer Pairs (Differential and Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Only the left and right banks have LVDS differential output drivers. See the $I_{DK}$ specification for I/O leakage current during power-up.

## Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP/EC devices, see the list of technical documentation at the end of this data sheet.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

## Supported Standards

The LatticeECP/EC sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of technical information at the end of this data sheet.

***Table 2-13. Supported Input Standards***

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33[2] | — | — |
| LVCMOS25[2] | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12[2] | — | — |
| PCI | — | 3.3 |
| HSTL18 Class I, II | 0.9 | — |
| HSTL18 Class III | 1.08 | — |
| HSTL15 Class I | 0.75 | — |
| HSTL15 Class III | 0.9 | — |
| SSTL3 Class I, II | 1.5 | — |
| SSTL2 Class I, II | 1.25 | — |
| SSTL18 Class I | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I | — | — |
| Differential SSTL2 Class I, II | — | — |
| Differential SSTL3 Class I, II | — | — |
| Differential HSTL15 Class I, III | — | — |
| Differential HSTL18 Class I, II, III | — | — |
| LVDS, LVPECL, BLVDS, RSDS | — | — |

1. When not specified $V_{CCIO}$ can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow $V_{CCJ}$.

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

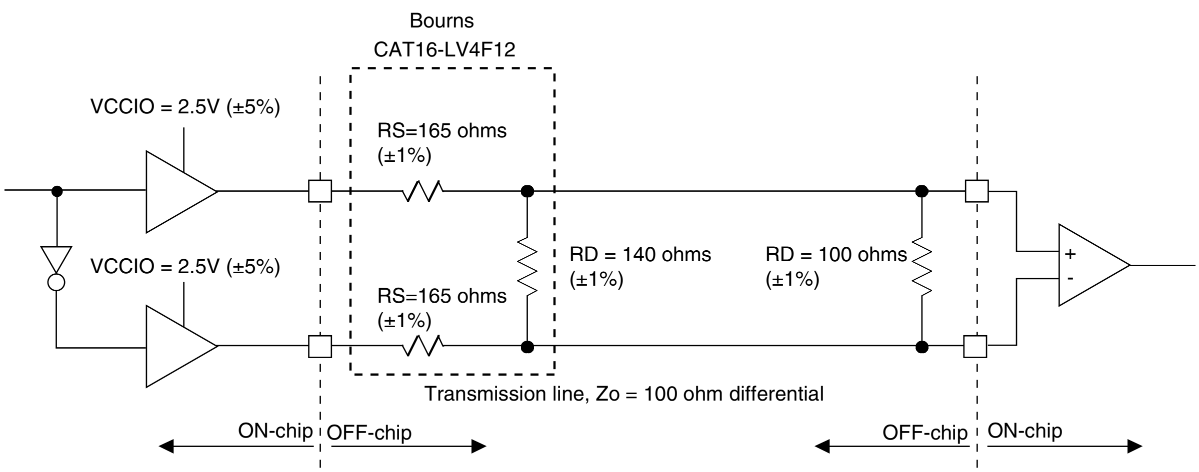



***Table 3-1. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.42 | V |
| $V_{OL}$ | Output low voltage | 1.08 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | ¾ |

# LatticeECP/EC Family Timing Adders[1, 2, 3] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| HSTL15_II | HSTL_15 class II | 0.10 | 0.12 | 0.14 | ns |
| HSTL15_III | HSTL_15 class III | 0.10 | 0.12 | 0.14 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.08 | 0.10 | 0.11 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.10 | 0.12 | 0.14 | ns |
| SSTL33_I | SSTL_3 class I | -0.05 | -0.06 | -0.07 | ns |
| SSTL33_II | SSTL_3 class II | 0.40 | 0.48 | 0.56 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.05 | -0.06 | -0.07 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.40 | 0.48 | 0.56 | ns |
| SSTL25_I | SSTL_2 class I | 0.05 | 0.07 | 0.08 | ns |
| SSTL25_II | SSTL_2 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.05 | 0.07 | 0.08 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL18_I | SSTL_1.8 class I | 0.01 | 0.01 | 0.01 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.01 | 0.01 | 0.01 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.09 | 0.11 | 0.13 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | -0.03 | -0.04 | -0.05 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.36 | 0.43 | 0.51 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | 0.28 | 0.33 | 0.39 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.09 | 0.11 | 0.13 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | -0.03 | -0.04 | -0.05 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.36 | 0.43 | 0.51 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | 0.28 | 0.33 | 0.39 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.18 | 0.21 | 0.25 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.10 | 0.12 | 0.14 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.22 | 0.26 | 0.31 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | 0.14 | 0.16 | 0.19 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.15 | 0.18 | 0.21 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.06 | 0.08 | 0.09 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | 0.01 | 0.01 | 0.01 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.16 | 0.19 | 0.22 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.26 | 0.31 | 0.36 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.04 | 0.04 | 0.05 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.36 | 0.43 | 0.50 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.08 | 0.10 | 0.11 | ns |
| LVCMOS12_4mA | LVCMOS 1.2 4mA drive | 0.36 | 0.43 | 0.50 | ns |
| PCI33 | PCI33 | 1.05 | 1.26 | 1.46 | ns |

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Conditions table of this document.
3. All other standards according to the appropriate specification.

Timing v.G 0.30

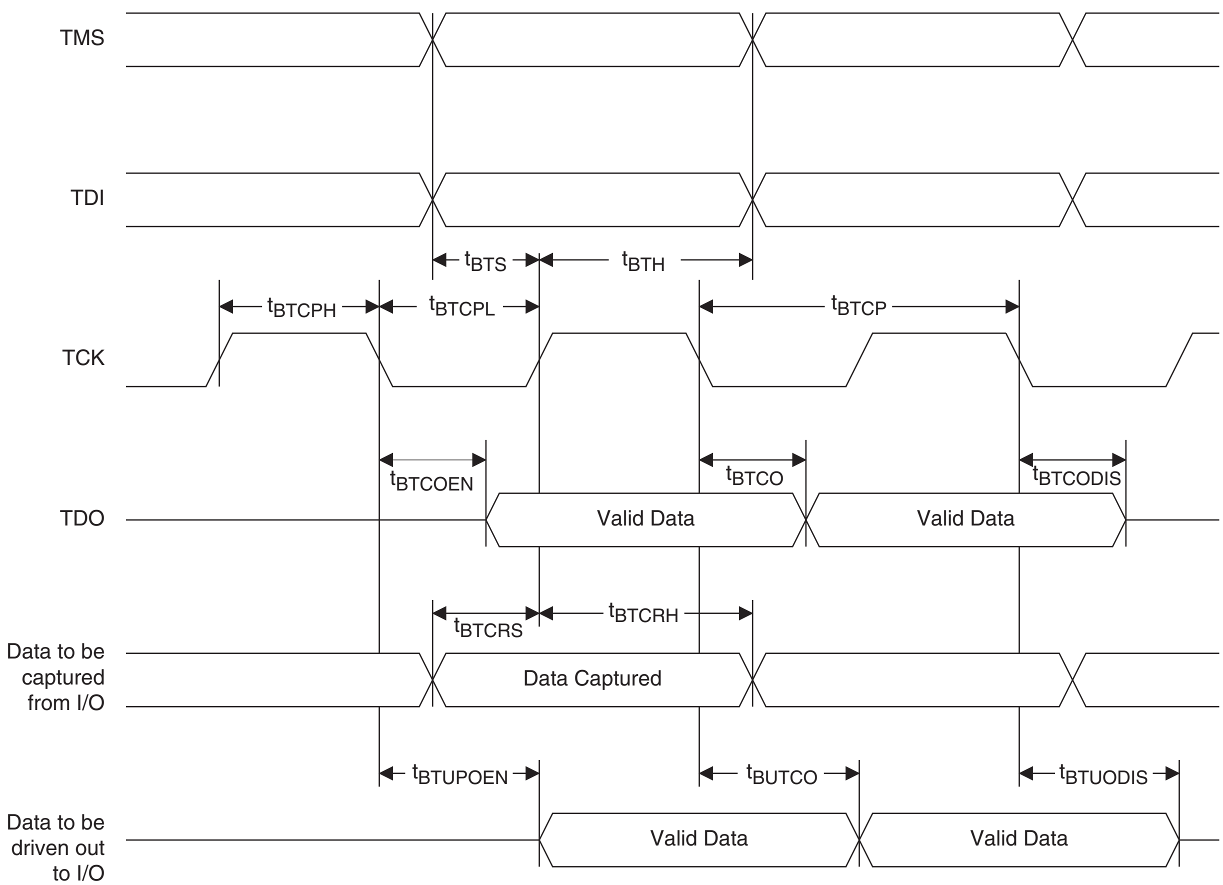
# JTAG Port Timing Specifications

**Over Recommended Operating Conditions**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 10 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

Timing v.G 0.30

***Figure 3-20. JTAG Port Timing Waveforms***



# LatticeECP/EC Family Data Sheet
# Pinout Information



## Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected.<br><br>Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.<br><br>During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins. |
| $V_{CCIOx}$ | — | Power supply pins for I/O bank x. Dedicated pins. |
| $V_{REF1\_x}$, $V_{REF2\_x}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| XRES | — | 10K ohm +/-1% resistor must be connected between this pad and ground. |
| $V_{CCPLL}$ | — | Power supply pin for PLL.bApplicable to ECP/EC33 device. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN_A | I | Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_PLL[T, C]_FB_A | I | Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |
| [LOC]DQS[num] | I | DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output. |
| **Test and Programming** (Dedicated pins) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |

## LFEC1, LFEC3 Logic Signal Connections: 208 PQFP

| | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 1* | GND0<br>GND7 | - | | | GND0<br>GND7 | - | | |
| 2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 3 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 |
| 4 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 |
| 5 | NC | - | | | NC | - | | |
| 6 | NC | - | | | NC | - | | |
| 7 | NC | - | | | PL3B | 7 | | |
| 8 | NC | - | | | PL4A | 7 | T | |
| 9 | NC | - | | | PL4B | 7 | C | |
| 10 | NC | - | | | PL5A | 7 | T | |
| 11 | NC | - | | | PL5B | 7 | C | |
| 12 | NC | - | | | PL6A | 7 | T | LDQS6 |
| 13 | NC | - | | | VCCIO7 | 7 | | |
| 14 | NC | - | | | PL6B | 7 | C | |
| 15 | PL3A | 7 | T | | PL7A | 7 | T | |
| 16 | PL3B | 7 | C | | PL7B | 7 | C | |
| 17 | PL4A | 7 | T | | PL8A | 7 | T | |
| 18 | NC | - | | | NC | - | | |
| 19 | PL4B | 7 | C | | PL8B | 7 | C | |
| 20 | PL5A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 |
| 21 | PL5B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 |
| 22 | NC | - | | | VCCAUX | - | | |
| 23 | XRES | 6 | | | XRES | 6 | | |
| 24 | NC | - | | | NC | - | | |
| 25 | NC | - | | | NC | - | | |
| 26 | VCC | - | | | VCC | - | | |
| 27 | TCK | 6 | | | TCK | 6 | | |
| 28 | GND | - | | | GND | - | | |
| 29 | TDI | 6 | | | TDI | 6 | | |
| 30 | TMS | 6 | | | TMS | 6 | | |
| 31 | TDO | 6 | | | TDO | 6 | | |
| 32 | VCCJ | 6 | | | VCCJ | 6 | | |
| 33 | PL7A | 6 | T | LLM0_PLLT_IN_A | PL11A | 6 | T | LLM0_PLLT_IN_A |
| 34 | PL7B | 6 | C | LLM0_PLLC_IN_A | PL11B | 6 | C | LLM0_PLLC_IN_A |
| 35 | PL8A | 6 | T | LLM0_PLLT_FB_A | PL12A | 6 | T | LLM0_PLLT_FB_A |
| 36 | PL8B | 6 | C | LLM0_PLLC_FB_A | PL12B | 6 | C | LLM0_PLLC_FB_A |
| 37 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 38 | PL9A | 6 | T | | PL13A | 6 | T | |
| 39 | PL9B | 6 | C | | PL13B | 6 | C | |
| 40 | PL10A | 6 | T | | PL14A | 6 | T | |
| 41 | GND6 | 6 | | | GND6 | 6 | | |
| 42 | PL10B | 6 | C | | PL14B | 6 | C | |

## LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFECP6/LFEC6 | | | | LFECP10/LFEC10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 43 | PL24A | 6 | T | LDQS24 | PL33A | 6 | T | LDQS33 |
| 44 | PL24B | 6 | C | | PL33B | 6 | C | |
| 45 | PL25A | 6 | T | | PL34A | 6 | T | |
| 46 | PL25B | 6 | C | | PL34B | 6 | C | |
| 47 | PL26A | 6 | T | | PL35A | 6 | T | |
| 48 | PL26B | 6 | C | | PL35B | 6 | C | |
| 49 | PL27A | 6 | T | VREF1_6 | PL36A | 6 | T | VREF1_6 |
| 50 | PL27B | 6 | C | VREF2_6 | PL36B | 6 | C | VREF2_6 |
| 51 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 52* | GND5<br>GND6 | - | | | GND5<br>GND6 | - | | |
| 53 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 54 | PB2A | 5 | T | | PB2A | 5 | T | |
| 55 | PB2B | 5 | C | | PB2B | 5 | C | |
| 56 | PB3A | 5 | T | | PB3A | 5 | T | |
| 57 | PB3B | 5 | C | | PB3B | 5 | C | |
| 58 | PB4A | 5 | T | | PB4A | 5 | T | |
| 59 | PB4B | 5 | C | | PB4B | 5 | C | |
| 60 | PB5A | 5 | T | | PB5A | 5 | T | |
| 61 | PB5B | 5 | C | | PB5B | 5 | C | |
| 62 | PB6A | 5 | T | BDQS6 | PB6A | 5 | T | BDQS6 |
| 63 | PB6B | 5 | C | | PB6B | 5 | C | |
| 64 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 65 | PB10A | 5 | T | | PB18A | 5 | T | |
| 66 | PB10B | 5 | C | | PB18B | 5 | C | |
| 67 | PB11A | 5 | T | | PB19A | 5 | T | |
| 68 | PB11B | 5 | C | | PB19B | 5 | C | |
| 69 | PB12A | 5 | T | | PB20A | 5 | T | |
| 70 | PB12B | 5 | C | | PB20B | 5 | C | |
| 71 | PB13A | 5 | T | | PB21A | 5 | T | |
| 72 | GND5 | 5 | | | GND5 | 5 | | |
| 73 | PB13B | 5 | C | | PB21B | 5 | C | |
| 74 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 75 | PB14A | 5 | T | BDQS14 | PB22A | 5 | T | BDQS22 |
| 76 | PB14B | 5 | C | | PB22B | 5 | C | |
| 77 | PB15A | 5 | T | | PB23A | 5 | T | |
| 78 | PB15B | 5 | C | | PB23B | 5 | C | |
| 79 | PB16A | 5 | T | VREF2_5 | PB24A | 5 | T | VREF2_5 |
| 80 | PB16B | 5 | C | VREF1_5 | PB24B | 5 | C | VREF1_5 |
| 81 | PB17A | 5 | T | PCLKT5_0 | PB25A | 5 | T | PCLKT5_0 |
| 82 | GND5 | 5 | | | GND5 | 5 | | |
| 83 | PB17B | 5 | C | PCLKC5_0 | PB25B | 5 | C | PCLKC5_0 |
| 84 | VCCAUX | - | | | VCCAUX | - | | |

## LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFECP10/LFEC10 | | | | LFECP15/LFEC15 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | LVDS | Dual Function | Ball Function | Bank | LVDS | Dual Function |
| P14 | PR35B | 3 | C | | PR43B | 3 | C | |
| P15 | PR35A | 3 | T | | PR43A | 3 | T | |
| R15 | PR34B | 3 | C | | PR42B | 3 | C | |
| R16 | PR34A | 3 | T | | PR42A | 3 | T | |
| M13 | PR33B | 3 | C | | PR41B | 3 | C | |
| M14 | PR33A | 3 | T | RDQS33 | PR41A | 3 | T | RDQS41 |
| P16 | PR32B | 3 | C | RLM0_PLLC_FB_A | PR40B | 3 | C | RLM0_PLLC_FB_A |
| GND | GND3 | 3 | | | GND3 | 3 | | |
| N16 | PR32A | 3 | T | RLM0_PLLT_FB_A | PR40A | 3 | T | RLM0_PLLT_FB_A |
| N15 | PR31B | 3 | C | RLM0_PLLC_IN_A | PR39B | 3 | C | RLM0_PLLC_IN_A |
| M15 | PR31A | 3 | T | RLM0_PLLT_IN_A | PR39A | 3 | T | RLM0_PLLT_IN_A |
| M16 | PR30B | 3 | C | DI/CSSPIN | PR38B | 3 | C | DI/CSSPIN |
| L16 | PR30A | 3 | T | DOUT/CSON | PR38A | 3 | T | DOUT/CSON |
| K16 | PR29B | 3 | C | BUSY/SISPI | PR37B | 3 | C | BUSY/SISPI |
| J16 | PR29A | 3 | T | D7/SPID0 | PR37A | 3 | T | D7/SPID0 |
| L12 | CFG2 | 3 | | | CFG2 | 3 | | |
| L14 | CFG1 | 3 | | | CFG1 | 3 | | |
| L13 | CFG0 | 3 | | | CFG0 | 3 | | |
| K13 | PROGRAMN | 3 | | | PROGRAMN | 3 | | |
| L15 | CCLK | 3 | | | CCLK | 3 | | |
| K15 | INITN | 3 | | | INITN | 3 | | |
| K14 | DONE | 3 | | | DONE | 3 | | |
| GND | GND3 | 3 | | | GND3 | 3 | | |
| H16 | PR27B | 3 | C | | PR31B | 3 | C | |
| - | - | - | | | GND3 | 3 | | |
| H15 | PR27A | 3 | T | | PR31A | 3 | T | |
| G16 | PR26B | 3 | C | | PR30B | 3 | C | |
| G15 | PR26A | 3 | T | | PR30A | 3 | T | |
| K12 | PR25B | 3 | C | | PR29B | 3 | C | |
| J12 | PR25A | 3 | T | | PR29A | 3 | T | |
| J14 | PR24B | 3 | C | | PR28B | 3 | C | |
| J15 | PR24A | 3 | T | RDQS24 | PR28A | 3 | T | RDQS28 |
| F16 | PR23B | 3 | C | | PR27B | 3 | C | |
| GND | GND3 | 3 | | | GND3 | 3 | | |
| F15 | PR23A | 3 | T | | PR27A | 3 | T | |
| J13 | PR22B | 3 | C | | PR26B | 3 | C | |
| H13 | PR22A | 3 | T | | PR26A | 3 | T | |
| H14 | PR21B | 3 | C | | PR25B | 3 | C | |
| G14 | PR21A | 3 | T | | PR25A | 3 | T | |
| E16 | PR20B | 3 | C | | PR24B | 3 | C | |
| E15 | PR20A | 3 | T | | PR24A | 3 | T | |
| H12 | PR18B | 2 | C | PCLKC2_0 | PR22B | 2 | C | PCLKC2_0 |
| GND | GND2 | 2 | | | GND2 | 2 | | |

# LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP6/LFEC6 | | | | | LFECP10/LFEC10 | | | | | LFECP/LFEC15 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| F14 | PT23B | 1 | C | | F14 | PT31B | 1 | C | | F14 | PT31B | 1 | C | |
| D14 | PT23A | 1 | T | | D14 | PT31A | 1 | T | | D14 | PT31A | 1 | T | |
| E13 | PT22B | 1 | C | | E13 | PT30B | 1 | C | | E13 | PT30B | 1 | C | |
| G13 | PT22A | 1 | T | TDQS22 | G13 | PT30A | 1 | T | TDQS30 | G13 | PT30A | 1 | T | TDQS30 |
| A12 | PT21B | 1 | C | | A12 | PT29B | 1 | C | | A12 | PT29B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B12 | PT21A | 1 | T | | B12 | PT29A | 1 | T | | B12 | PT29A | 1 | T | |
| F13 | PT20B | 1 | C | | F13 | PT28B | 1 | C | | F13 | PT28B | 1 | C | |
| D13 | PT20A | 1 | T | | D13 | PT28A | 1 | T | | D13 | PT28A | 1 | T | |
| F12 | PT19B | 1 | C | VREF2_1 | F12 | PT27B | 1 | C | VREF2_1 | F12 | PT27B | 1 | C | VREF2_1 |
| D12 | PT19A | 1 | T | VREF1_1 | D12 | PT27A | 1 | T | VREF1_1 | D12 | PT27A | 1 | T | VREF1_1 |
| F11 | PT18B | 1 | C | | F11 | PT26B | 1 | C | | F11 | PT26B | 1 | C | |
| C12 | PT18A | 1 | T | | C12 | PT26A | 1 | T | | C12 | PT26A | 1 | T | |
| A11 | PT17B | 0 | C | PCLKC0_0 | A11 | PT25B | 0 | C | PCLKC0_0 | A11 | PT25B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A10 | PT17A | 0 | T | PCLKT0_0 | A10 | PT25A | 0 | T | PCLKT0_0 | A10 | PT25A | 0 | T | PCLKT0_0 |
| E12 | PT16B | 0 | C | VREF1_0 | E12 | PT24B | 0 | C | VREF1_0 | E12 | PT24B | 0 | C | VREF1_0 |
| E11 | PT16A | 0 | T | VREF2_0 | E11 | PT24A | 0 | T | VREF2_0 | E11 | PT24A | 0 | T | VREF2_0 |
| B11 | PT15B | 0 | C | | B11 | PT23B | 0 | C | | B11 | PT23B | 0 | C | |
| C11 | PT15A | 0 | T | | C11 | PT23A | 0 | T | | C11 | PT23A | 0 | T | |
| B9 | PT14B | 0 | C | | B9 | PT22B | 0 | C | | B9 | PT22B | 0 | C | |
| B10 | PT14A | 0 | T | TDQS14 | B10 | PT22A | 0 | T | TDQS22 | B10 | PT22A | 0 | T | TDQS22 |
| A9 | PT13B | 0 | C | | A9 | PT21B | 0 | C | | A9 | PT21B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A8 | PT13A | 0 | T | | A8 | PT21A | 0 | T | | A8 | PT21A | 0 | T | |
| D11 | PT12B | 0 | C | | D11 | PT20B | 0 | C | | D11 | PT20B | 0 | C | |
| C10 | PT12A | 0 | T | | C10 | PT20A | 0 | T | | C10 | PT20A | 0 | T | |
| A7 | PT11B | 0 | C | | A7 | PT19B | 0 | C | | A7 | PT19B | 0 | C | |
| A6 | PT11A | 0 | T | | A6 | PT19A | 0 | T | | A6 | PT19A | 0 | T | |
| B7 | PT10B | 0 | C | | B7 | PT18B | 0 | C | | B7 | PT18B | 0 | C | |
| B8 | PT10A | 0 | T | | B8 | PT18A | 0 | T | | B8 | PT18A | 0 | T | |
| A5 | PT9B | 0 | C | | A5 | PT17B | 0 | C | | A5 | PT17B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| B6 | PT9A | 0 | T | | B6 | PT17A | 0 | T | | B6 | PT17A | 0 | T | |
| G10 | PT8B | 0 | C | | G10 | PT16B | 0 | C | | G10 | PT16B | 0 | C | |
| E10 | PT8A | 0 | T | | E10 | PT16A | 0 | T | | E10 | PT16A | 0 | T | |
| F10 | PT7B | 0 | C | | F10 | PT15B | 0 | C | | F10 | PT15B | 0 | C | |
| D10 | PT7A | 0 | T | | D10 | PT15A | 0 | T | | D10 | PT15A | 0 | T | |
| G9 | PT6B | 0 | C | | G9 | PT14B | 0 | C | | G9 | PT14B | 0 | C | |
| E9 | PT6A | 0 | T | TDQS6 | E9 | PT14A | 0 | T | TDQS14 | E9 | PT14A | 0 | T | TDQS14 |
| C9 | PT5B | 0 | C | | C9 | PT13B | 0 | C | | C9 | PT13B | 0 | C | |
| GND | - | - | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| C8 | PT5A | 0 | T | | C8 | PT13A | 0 | T | | C8 | PT13A | 0 | T | |
| F9 | PT4B | 0 | C | | F9 | PT12B | 0 | C | | F9 | PT12B | 0 | C | |
| D9 | PT4A | 0 | T | | D9 | PT12A | 0 | T | | D9 | PT12A | 0 | T | |
| F8 | PT3B | 0 | C | | F8 | PT11B | 0 | C | | F8 | PT11B | 0 | C | |
| D7 | PT3A | 0 | T | | D7 | PT11A | 0 | T | | D7 | PT11A | 0 | T | |
| D8 | PT2B | 0 | C | | D8 | PT10B | 0 | C | | D8 | PT10B | 0 | C | |
| C7 | PT2A | 0 | T | | C7 | PT10A | 0 | T | | C7 | PT10A | 0 | T | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | | GND | GND0 | 0 | | |

## LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| Y13 | PB40A | 4 | T | | Y13 | PB40A | 4 | T | |
| V14 | PB40B | 4 | C | D5/SPID2 | V14 | PB40B | 4 | C | D5/SPID2 |
| AA13 | PB41A | 4 | T | | AA13 | PB41A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AB13 | PB41B | 4 | C | D6/SPID1 | AB13 | PB41B | 4 | C | D6/SPID1 |
| AA14 | PB42A | 4 | T | | AA14 | PB42A | 4 | T | |
| Y14 | PB42B | 4 | C | | Y14 | PB42B | 4 | C | |
| Y15 | PB43A | 4 | T | | Y15 | PB43A | 4 | T | |
| W15 | PB43B | 4 | C | | W15 | PB43B | 4 | C | |
| V15 | PB44A | 4 | T | | V15 | PB44A | 4 | T | |
| T14 | PB44B | 4 | C | | T14 | PB44B | 4 | C | |
| AB14 | PB45A | 4 | T | | AB14 | PB45A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AB15 | PB45B | 4 | C | | AB15 | PB45B | 4 | C | |
| AB16 | PB46A | 4 | T | BDQS46 | AB16 | PB46A | 4 | T | BDQS46 |
| AA15 | PB46B | 4 | C | | AA15 | PB46B | 4 | C | |
| AB17 | PB47A | 4 | T | | AB17 | PB47A | 4 | T | |
| AA16 | PB47B | 4 | C | | AA16 | PB47B | 4 | C | |
| AB18 | PB48A | 4 | T | | AB18 | PB48A | 4 | T | |
| AA17 | PB48B | 4 | C | | AA17 | PB48B | 4 | C | |
| AB19 | PB49A | 4 | T | | AB19 | PB49A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AA18 | PB49B | 4 | C | | AA18 | PB49B | 4 | C | |
| W16 | PB50A | 4 | T | | W16 | PB50A | 4 | T | |
| U15 | PB50B | 4 | C | | U15 | PB50B | 4 | C | |
| V16 | PB51A | 4 | T | | V16 | PB51A | 4 | T | |
| U16 | PB51B | 4 | C | | U16 | PB51B | 4 | C | |
| Y17 | PB52A | 4 | T | | Y17 | PB52A | 4 | T | |
| V17 | PB52B | 4 | C | | V17 | PB52B | 4 | C | |
| AB20 | PB53A | 4 | T | | AB20 | PB53A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AA19 | PB53B | 4 | C | | AA19 | PB53B | 4 | C | |
| Y16 | PB54A | 4 | T | BDQS54 | Y16 | PB54A | 4 | T | BDQS54 |
| W17 | PB54B | 4 | C | | W17 | PB54B | 4 | C | |
| AA20 | PB55A | 4 | T | | AA20 | PB55A | 4 | T | |
| Y19 | PB55B | 4 | C | | Y19 | PB55B | 4 | C | |
| Y18 | PB56A | 4 | T | | Y18 | PB56A | 4 | T | |
| W18 | PB56B | 4 | C | | W18 | PB56B | 4 | C | |
| T17 | PB57A | 4 | T | | T17 | PB57A | 4 | T | |
| U17 | PB57B | 4 | C | | U17 | PB57B | 4 | C | |
| GND | - | - | | | GND | GND4 | 4 | | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| GND | GND3 | 3 | | | GND | GND4 | 4 | | |
| GND | - | - | | | GND | GND3 | 3 | | |

## LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| C22 | PR9A | 2 | T | RUM0_PLLT_FB_A | C22 | PR17A | 2 | T | RUM0_PLLT_FB_A |
| G19 | PR8B | 2 | C | RUM0_PLLC_IN_A | G19 | PR16B | 2 | C | RUM0_PLLC_IN_A |
| G18 | PR8A | 2 | T | RUM0_PLLT_IN_A | G18 | PR16A | 2 | T | RUM0_PLLT_IN_A |
| F20 | PR7B | 2 | C | | F20 | PR15B | 2 | C | |
| F19 | PR7A | 2 | T | | F19 | PR15A | 2 | T | |
| E20 | PR6B | 2 | C | | E20 | PR14B | 2 | C | |
| D20 | PR6A | 2 | T | RDQS6 | D20 | PR14A | 2 | T | RDQS14 |
| C21 | PR5B | 2 | C | | C21 | PR13B | 2 | C | |
| GND | - | - | | | GND | GND2 | 2 | | |
| C20 | PR5A | 2 | T | | C20 | PR13A | 2 | T | |
| F18 | PR4B | 2 | C | | F18 | PR12B | 2 | C | |
| E18 | PR4A | 2 | T | | E18 | PR12A | 2 | T | |
| B22 | PR3B | 2 | C | | B22 | PR11B | 2 | C | |
| B21 | PR3A | 2 | T | | B21 | PR11A | 2 | T | |
| GND | - | - | | | GND | GND2 | 2 | | |
| E19 | PR2B | 2 | C | VREF1_2 | E19 | PR2B | 2 | C | VREF1_2 |
| D19 | PR2A | 2 | T | VREF2_2 | D19 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| GND | - | - | | | GND | GND1 | 1 | | |
| G17 | PT57B | 1 | C | | G17 | PT57B | 1 | C | |
| GND | - | - | | | GND | GND1 | 1 | | |
| F17 | PT57A | 1 | T | | F17 | PT57A | 1 | T | |
| D18 | PT56B | 1 | C | | D18 | PT56B | 1 | C | |
| C18 | PT56A | 1 | T | | C18 | PT56A | 1 | T | |
| C19 | PT55B | 1 | C | | C19 | PT55B | 1 | C | |
| B20 | PT55A | 1 | T | | B20 | PT55A | 1 | T | |
| D17 | PT54B | 1 | C | | D17 | PT54B | 1 | C | |
| C16 | PT54A | 1 | T | TDQS54 | C16 | PT54A | 1 | T | TDQS54 |
| B19 | PT53B | 1 | C | | B19 | PT53B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A20 | PT53A | 1 | T | | A20 | PT53A | 1 | T | |
| E17 | PT52B | 1 | C | | E17 | PT52B | 1 | C | |
| C17 | PT52A | 1 | T | | C17 | PT52A | 1 | T | |
| F16 | PT51B | 1 | C | | F16 | PT51B | 1 | C | |
| E16 | PT51A | 1 | T | | E16 | PT51A | 1 | T | |
| F15 | PT50B | 1 | C | | F15 | PT50B | 1 | C | |
| D16 | PT50A | 1 | T | | D16 | PT50A | 1 | T | |
| B18 | PT49B | 1 | C | | B18 | PT49B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A19 | PT49A | 1 | T | | A19 | PT49A | 1 | T | |
| B17 | PT48B | 1 | C | | B17 | PT48B | 1 | C | |
| A18 | PT48A | 1 | T | | A18 | PT48A | 1 | T | |
| B16 | PT47B | 1 | C | | B16 | PT47B | 1 | C | |

## LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| A17 | PT47A | 1 | T | | A17 | PT47A | 1 | T | |
| B15 | PT46B | 1 | C | | B15 | PT46B | 1 | C | |
| A16 | PT46A | 1 | T | TDQS46 | A16 | PT46A | 1 | T | TDQS46 |
| A15 | PT45B | 1 | C | | A15 | PT45B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A14 | PT45A | 1 | T | | A14 | PT45A | 1 | T | |
| G14 | PT44B | 1 | C | | G14 | PT44B | 1 | C | |
| E15 | PT44A | 1 | T | | E15 | PT44A | 1 | T | |
| D15 | PT43B | 1 | C | | D15 | PT43B | 1 | C | |
| C15 | PT43A | 1 | T | | C15 | PT43A | 1 | T | |
| C14 | PT42B | 1 | C | | C14 | PT42B | 1 | C | |
| B14 | PT42A | 1 | T | | B14 | PT42A | 1 | T | |
| A13 | PT41B | 1 | C | | A13 | PT41B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B13 | PT41A | 1 | T | | B13 | PT41A | 1 | T | |
| E14 | PT40B | 1 | C | | E14 | PT40B | 1 | C | |
| C13 | PT40A | 1 | T | | C13 | PT40A | 1 | T | |
| F14 | PT39B | 1 | C | | F14 | PT39B | 1 | C | |
| D14 | PT39A | 1 | T | | D14 | PT39A | 1 | T | |
| E13 | PT38B | 1 | C | | E13 | PT38B | 1 | C | |
| G13 | PT38A | 1 | T | TDQS38 | G13 | PT38A | 1 | T | TDQS38 |
| A12 | PT37B | 1 | C | | A12 | PT37B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B12 | PT37A | 1 | T | | B12 | PT37A | 1 | T | |
| F13 | PT36B | 1 | C | | F13 | PT36B | 1 | C | |
| D13 | PT36A | 1 | T | | D13 | PT36A | 1 | T | |
| F12 | PT35B | 1 | C | VREF2_1 | F12 | PT35B | 1 | C | VREF2_1 |
| D12 | PT35A | 1 | T | VREF1_1 | D12 | PT35A | 1 | T | VREF1_1 |
| F11 | PT34B | 1 | C | | F11 | PT34B | 1 | C | |
| C12 | PT34A | 1 | T | | C12 | PT34A | 1 | T | |
| A11 | PT33B | 0 | C | PCLKC0_0 | A11 | PT33B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A10 | PT33A | 0 | T | PCLKT0_0 | A10 | PT33A | 0 | T | PCLKT0_0 |
| E12 | PT32B | 0 | C | VREF1_0 | E12 | PT32B | 0 | C | VREF1_0 |
| E11 | PT32A | 0 | T | VREF2_0 | E11 | PT32A | 0 | T | VREF2_0 |
| B11 | PT31B | 0 | C | | B11 | PT31B | 0 | C | |
| C11 | PT31A | 0 | T | | C11 | PT31A | 0 | T | |
| B9 | PT30B | 0 | C | | B9 | PT30B | 0 | C | |
| B10 | PT30A | 0 | T | TDQS30 | B10 | PT30A | 0 | T | TDQS30 |
| A9 | PT29B | 0 | C | | A9 | PT29B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A8 | PT29A | 0 | T | | A8 | PT29A | 0 | T | |
| D11 | PT28B | 0 | C | | D11 | PT28B | 0 | C | |
| C10 | PT28A | 0 | T | | C10 | PT28A | 0 | T | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| D13 | PT32B | 0 | C | VREF1_0 | D13 | PT32B | 0 | C | VREF1_0 |
| C13 | PT32A | 0 | T | VREF2_0 | C13 | PT32A | 0 | T | VREF2_0 |
| A13 | PT31B | 0 | C | | A13 | PT31B | 0 | C | |
| B13 | PT31A | 0 | T | | B13 | PT31A | 0 | T | |
| F13 | PT30B | 0 | C | | F13 | PT30B | 0 | C | |
| F12 | PT30A | 0 | T | TDQS30 | F12 | PT30A | 0 | T | TDQS30 |
| A12 | PT29B | 0 | C | | A12 | PT29B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| B12 | PT29A | 0 | T | | B12 | PT29A | 0 | T | |
| A11 | PT28B | 0 | C | | A11 | PT28B | 0 | C | |
| B11 | PT28A | 0 | T | | B11 | PT28A | 0 | T | |
| D12 | PT27B | 0 | C | | D12 | PT27B | 0 | C | |
| C12 | PT27A | 0 | T | | C12 | PT27A | 0 | T | |
| B10 | PT26B | 0 | C | | B10 | PT26B | 0 | C | |
| A10 | PT26A | 0 | T | | A10 | PT26A | 0 | T | |
| G12 | PT25B | 0 | C | | G12 | PT25B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A9 | PT25A | 0 | T | | A9 | PT25A | 0 | T | |
| E12 | PT24B | 0 | C | | E12 | PT24B | 0 | C | |
| B9 | PT24A | 0 | T | | B9 | PT24A | 0 | T | |
| F11 | PT23B | 0 | C | | F11 | PT23B | 0 | C | |
| A8 | PT23A | 0 | T | | A8 | PT23A | 0 | T | |
| D11 | PT22B | 0 | C | | D11 | PT22B | 0 | C | |
| C11 | PT22A | 0 | T | TDQS22 | C11 | PT22A | 0 | T | TDQS22 |
| B8 | PT21B | 0 | C | | B8 | PT21B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| B7 | PT21A | 0 | T | | B7 | PT21A | 0 | T | |
| E11 | PT20B | 0 | C | | E11 | PT20B | 0 | C | |
| A7 | PT20A | 0 | T | | A7 | PT20A | 0 | T | |
| G11 | PT19B | 0 | C | | G11 | PT19B | 0 | C | |
| C7 | PT19A | 0 | T | | C7 | PT19A | 0 | T | |
| G10 | PT18B | 0 | C | | G10 | PT18B | 0 | C | |
| C6 | PT18A | 0 | T | | C6 | PT18A | 0 | T | |
| C10 | PT17B | 0 | C | | C10 | PT17B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| D10 | PT17A | 0 | T | | D10 | PT17A | 0 | T | |
| F10 | PT16B | 0 | C | | F10 | PT16B | 0 | C | |
| A6 | PT16A | 0 | T | | A6 | PT16A | 0 | T | |
| E10 | PT15B | 0 | C | | E10 | PT15B | 0 | C | |
| C9 | PT15A | 0 | T | | C9 | PT15A | 0 | T | |
| G9 | PT14B | 0 | C | | G9 | PT14B | 0 | C | |
| D9 | PT14A | 0 | T | TDQS14 | D9 | PT14A | 0 | T | TDQS14 |

**LatticeECP Industrial (Continued)**

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP20E-3F672I | 400 | -3 | fpBGA | 672 | IND | 19.7K |
| LFECP20E-4F672I | 400 | -4 | fpBGA | 672 | IND | 19.7K |
| LFECP20E-3F484I | 360 | -3 | fpBGA | 484 | IND | 19.7K |
| LFECP20E-4F484I | 360 | -4 | fpBGA | 484 | IND | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3F672I | 496 | -3 | fpBGA | 672 | IND | 32.8K |
| LFECP33E-4F672I | 496 | -4 | fpBGA | 672 | IND | 32.8K |
| LFECP33E-3F484I | 360 | -3 | fpBGA | 484 | IND | 32.8K |
| LFECP33E-4F484I | 360 | -4 | fpBGA | 484 | IND | 32.8K |