Lattice Semiconductor Corporation - LFECP6E-3FN484I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	224
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp6e-3fn484i

LatticeECP/EC Family Data Sheet
Introduction

September 2012 **Data Sheet**

Features

- **Extensive Density and Package Options**
  - 1.5K to 32.8K LUT4s
  - 65 to 496 I/Os
  - Density migration supported
- **sysDSP™ Block (LatticeECP™ Versions)**
  - High performance multiply and accumulate
  - 4 to 8 blocks
    - 4 to 8 36x36 multipliers or
    - 16 to 32 18x18 multipliers or
    - 32 to 64 9x9 multipliers
- **Embedded and Distributed Memory**
  - 18 Kbits to 498 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 131 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysI/O™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - SPI boot flash interface
  - 1.2V power supply
- **Low Cost FPGA**
  - Features optimized for mainstream applications
  - Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFECP6	LFEC10/ LFECP10	LFEC15/ LFECP15	LFEC20/ LFECP20	LFEC33/ LFECP33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
PFUs/PFFs	192	384	768	1280	1920	2464	4096
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (Kbits)	6	12	25	41	61	79	131
EBR SRAM (Kbits)	18	55	92	276	350	424	498
EBR SRAM Blocks	2	6	10	30	38	46	54
sysDSP Blocks[1]	—	—	4	5	6	7	8
18x18 Multipliers[1]	—	—	16	20	24	28	32
V_{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

[1] LatticeECP devices only.

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Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, the routing of both short and long connections between PFUs.

The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

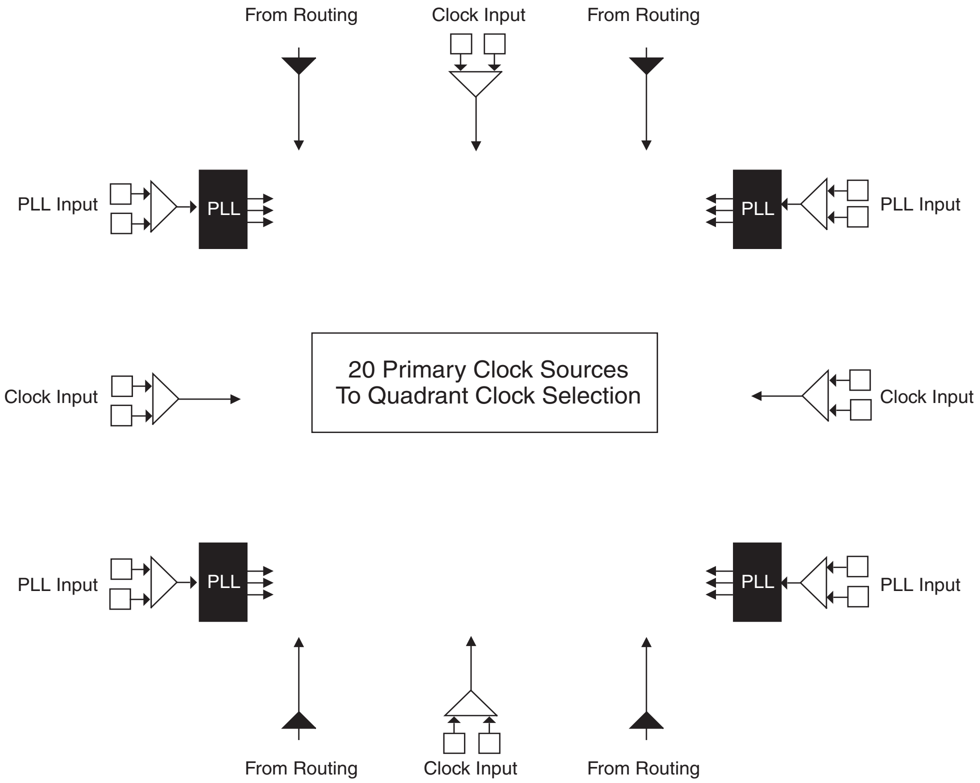
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Primary Clock Sources



Note: Smaller devices have two PLLs.

grammed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-11. PLL Diagram

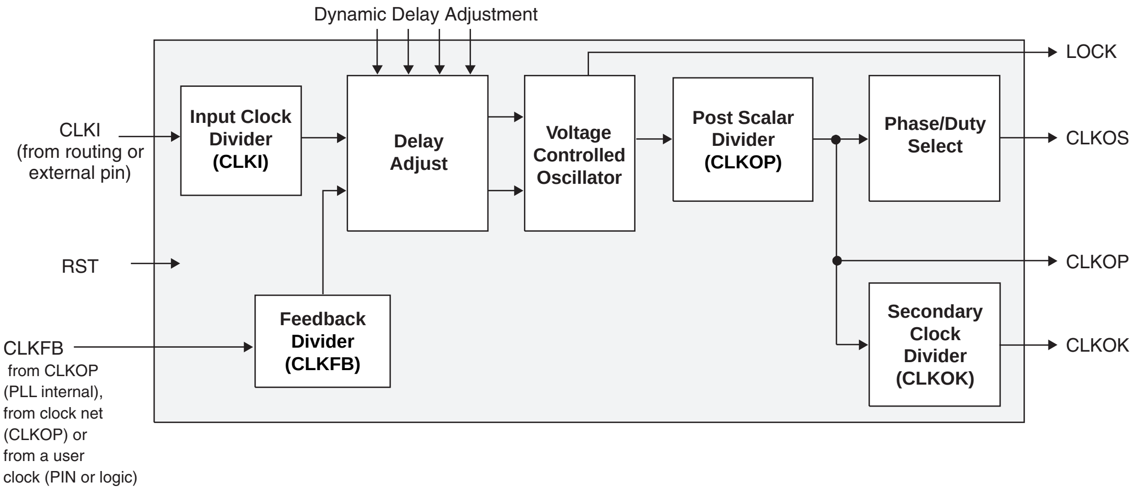


Figure 2-12 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-12. PLL Primitive

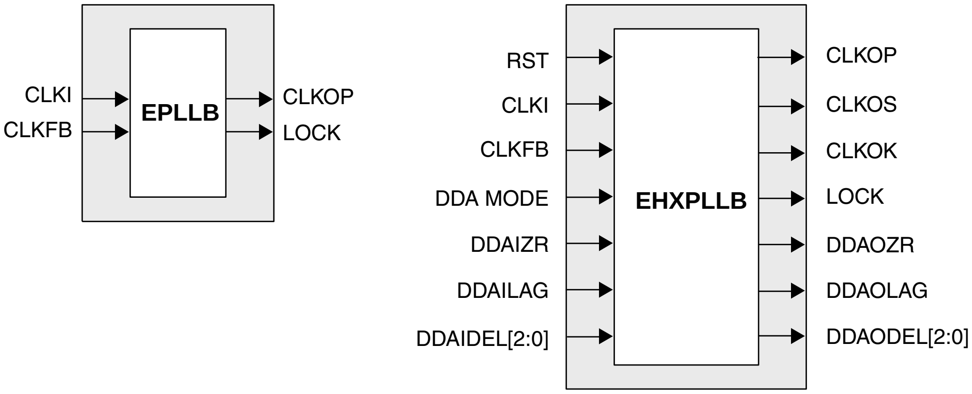


Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information about the PLL, please see the list of technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved regardless of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

Figure 2-13. DCS Block Primitive

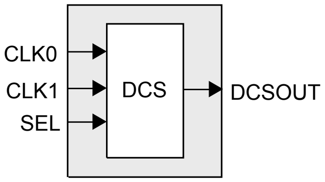


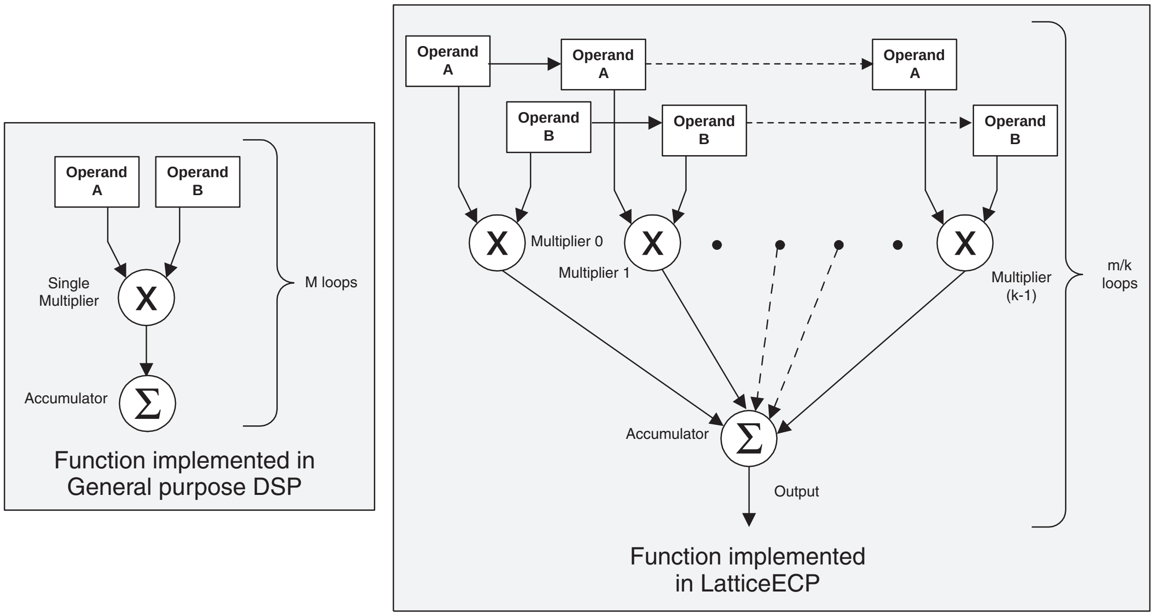
Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-18 compares the serial and the parallel implementations.

Figure 2-18. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

• MULT	(Multiply)
• MAC	(Multiply, Accumulate)
• MULTADD	(Multiply, Addition/Subtraction)
• MULTADDSUM	(Multiply, Addition/Subtraction, Accumulate)

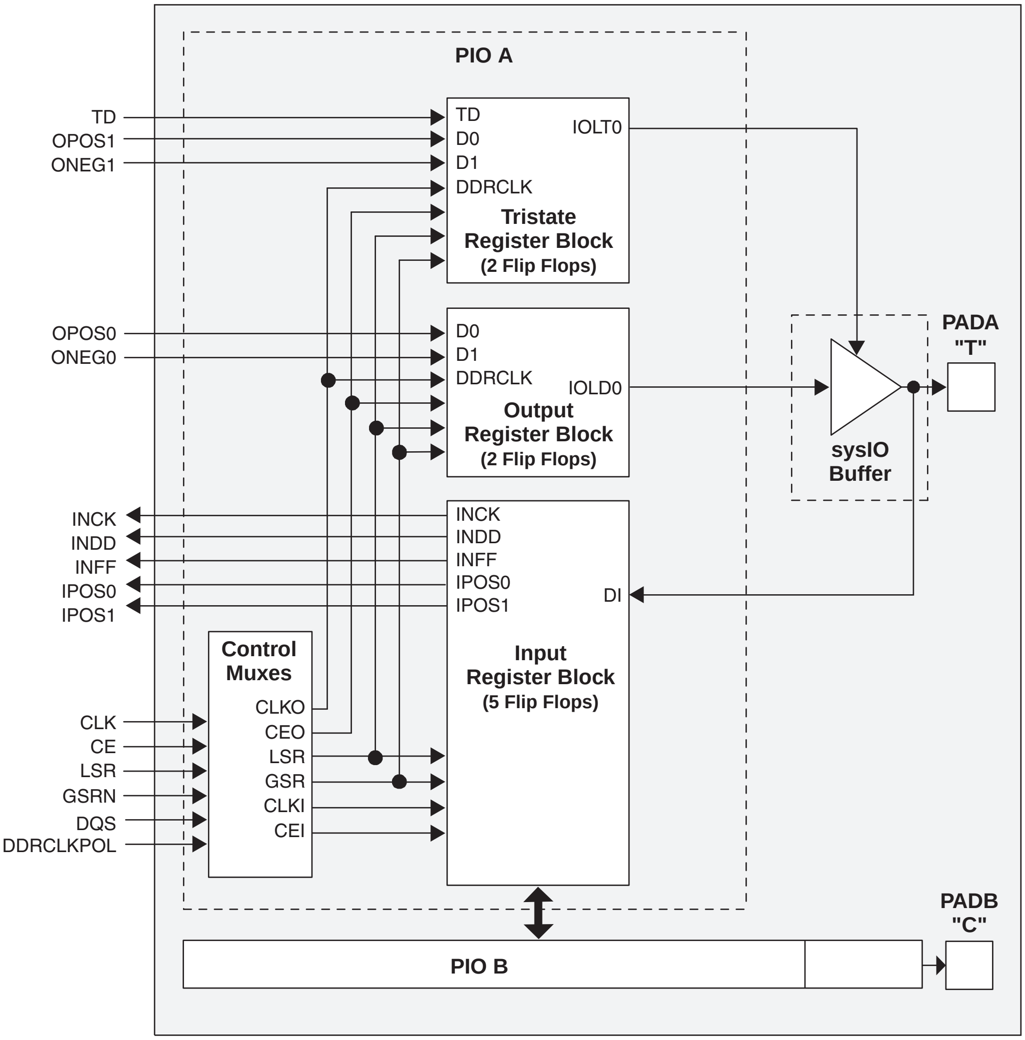
The number of elements available in each block depends on the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

Figure 2-24. PIC Diagram



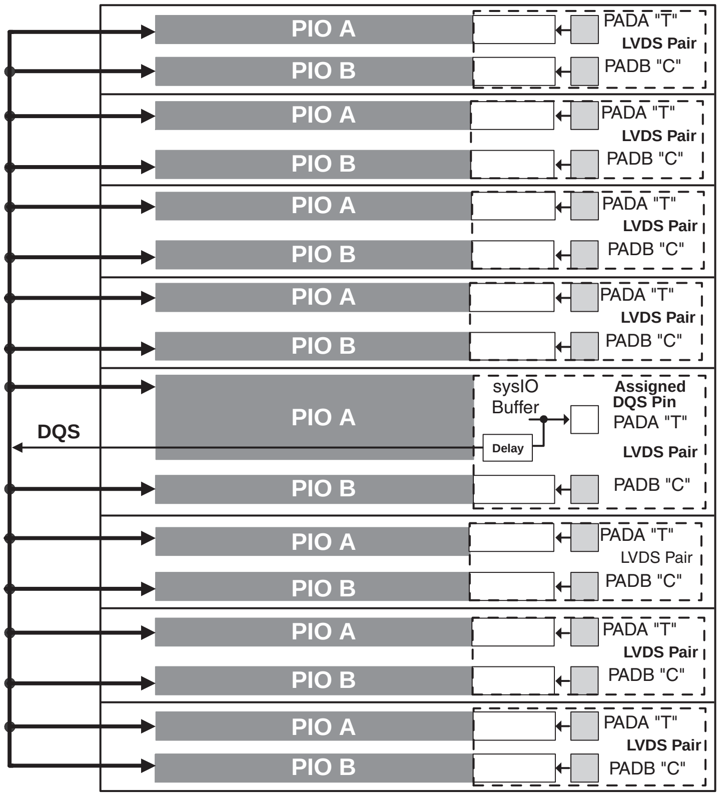
Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}[7]	Clock to Output - PIO Output Register	LFEC1	—	5.09	—	6.11	—	7.13	ns
		LFEC3	—	5.71	—	6.85	—	7.99	ns
		LFEC6	—	5.60	—	6.72	—	7.84	ns
		LFEC10	—	5.47	—	6.57	—	7.66	ns
		LFEC15	—	5.67	—	6.81	—	7.94	ns
		LFEC20	—	5.89	—	7.07	—	8.25	ns
		LFEC33	—	6.19	—	7.42	—	8.66	ns
t_{SU}[7]	Clock to Data Setup - PIO Input Register	LFEC1	-0.08	—	-0.10	—	-0.12	—	ns
		LFEC3	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC6	-0.63	—	-0.76	—	-0.89	—	ns
		LFEC10	-0.43	—	-0.52	—	-0.61	—	ns
		LFEC15	-0.70	—	-0.84	—	-0.98	—	ns
		LFEC20	-0.88	—	-1.06	—	-1.24	—	ns
		LFEC33	-1.12	—	-1.34	—	-1.56	—	ns
t_{H}[7]	Clock to Data Hold - PIO Input Register	LFEC1	2.19	—	2.62	—	3.06	—	ns
		LFEC3	2.80	—	3.36	—	3.92	—	ns
		LFEC6	2.69	—	3.23	—	3.77	—	ns
		LFEC10	2.56	—	3.08	—	3.59	—	ns
		LFEC15	2.76	—	3.32	—	3.87	—	ns
		LFEC20	2.99	—	3.58	—	4.18	—	ns
		LFEC33	3.28	—	3.93	—	4.59	—	ns
t_{SU_DEL}[7]	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC1	3.36	—	4.03	—	4.70	—	ns
		LFEC3	2.74	—	3.29	—	3.84	—	ns
		LFEC6	2.81	—	3.37	—	3.93	—	ns
		LFEC10	3.01	—	3.61	—	4.21	—	ns
		LFEC15	2.74	—	3.29	—	3.83	—	ns
		LFEC20	2.56	—	3.07	—	3.58	—	ns
		LFEC33	2.32	—	2.79	—	3.25	—	ns
tH_DEL[7]	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC1	-1.31	—	-1.57	—	-1.83	—	ns
		LFEC3	-0.70	—	-0.83	—	-0.97	—	ns
		LFEC6	-0.80	—	-0.96	—	-1.12	—	ns
		LFEC10	-0.93	—	-1.12	—	-1.30	—	ns
		LFEC15	-0.73	—	-0.88	—	-1.02	—	ns
		LFEC20	-0.51	—	-0.61	—	-0.71	—	ns
		LFEC33	-0.22	—	-0.26	—	-0.30	—	ns
f_{MAX_IO}[2]	Clock Frequency of I/O and PFU Register	All	—	420	—	378	—	340	Mhz
DDR I/O Pin Parameters[3, 4, 5]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

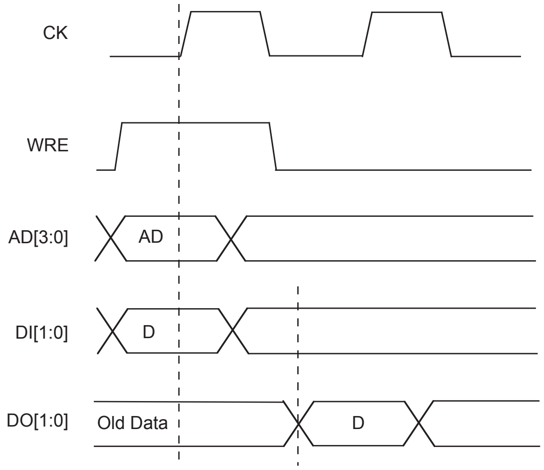
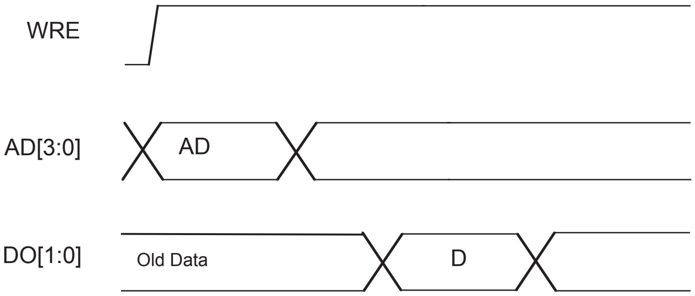


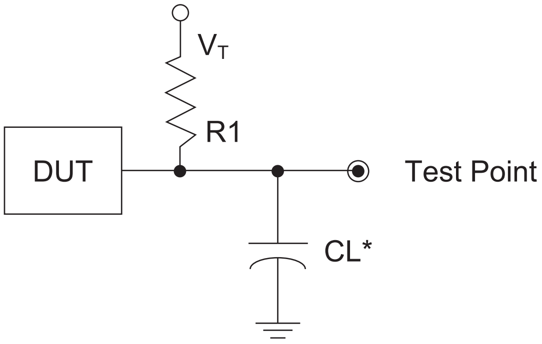
Figure 3-7. Slice Single /Dual Port Read Cycle Timing



Switching Test Conditions

Figure 3-21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-21. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	**R_1**	**C_L**	**Timing Ref.**	**V_T**
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188¾	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary (Cont.)

Pin Type		LFECP/EC15 256-fpBGA	LFECP/EC15 484-fpBGA	LFECP20/EC20 484-fpBGA	LFECP20/EC20 672-fpBGA	LFECP/EC33 484-fpBGA	LFECP/EC33 672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V_{CC}		10	20	20	32	16	28
V_{CCAUX}		2	12	12	20	12	20
V_{CCPLL}		0	0	0	0	4	4
V_{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V_{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

	LFEC1				LFEC3			
Pin Number	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
85	VCCIO4	4			VCCIO4	4		
86	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN
87	PB10B	4	C	CS1N	PB18B	4	C	CS1N
88	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
89	PB11B	4	C	CSN	PB19B	4	C	CSN
90	PB12A	4	T	VREF2_4	PB20A	4	T	VREF2_4
91	PB12B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
92	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
93	GND4	4			GND4	4		
94	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
95	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
96	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
97	PB15A	4	T		PB23A	4	T	
98	PB15B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
99	PB16A	4	T		PB24A	4	T	
100	PB16B	4	C	D5/SPID2	PB24B	4	C	D5/SPID2
101	PB17A	4	T		PB25A	4	T	
102	PB17B	4	C	D6/SPID1	PB25B	4	C	D6/SPID1
103	NC	-			NC	-		
104	VCCIO4	4			VCCIO4	4		
105*	GND3 GND4	-			GND3 GND4	-		
106	VCCIO3	3			VCCIO3	3		
107	PR14B	3	C	VREF2_3	PR18B	3	C	VREF2_3
108	PR14A	3	T	VREF1_3	PR18A	3	T	VREF1_3
109	PR13B	3	C		PR17B	3	C	
110	PR13A	3	T		PR17A	3	T	
111	PR12B	3	C		PR16B	3	C	
112	PR12A	3	T		PR16A	3	T	
113	PR11B	3	C		PR15B	3	C	
114	PR11A	3	T	RDQS11	PR15A	3	T	RDQS15
115	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
116	GND3	3			GND3	3		
117	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
118	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
119	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
120	VCCIO3	3			VCCIO3	3		
121	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
122	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
123	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
124	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
125	CFG2	3			CFG2	3		
126	CFG1	3			CFG1	3		

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

	LFEC1				LFEC3			
Pin Number	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
M4	PL13A	6	T		M4	PL22A	6	T		M4	PL26A	6	T	
M5	PL13B	6	C		M5	PL22B	6	C		M5	PL26B	6	C	
M1	PL14A	6	T		M1	PL23A	6	T		M1	PL27A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
M2	PL14B	6	C		M2	PL23B	6	C		M2	PL27B	6	C	
N3	PL15A	6	T	LDQS15	N3	PL24A	6	T	LDQS24	N3	PL28A	6	T	LDQS28
M3	PL15B	6	C		M3	PL24B	6	C		M3	PL28B	6	C	
N5	PL16A	6	T		N5	PL25A	6	T		N5	PL29A	6	T	
N4	PL16B	6	C		N4	PL25B	6	C		N4	PL29B	6	C	
N1	PL17A	6	T		N1	PL26A	6	T		N1	PL30A	6	T	
N2	PL17B	6	C		N2	PL26B	6	C		N2	PL30B	6	C	
P1	PL18A	6	T		P1	PL27A	6	T		P1	PL31A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
P2	PL18B	6	C		P2	PL27B	6	C		P2	PL31B	6	C	
R6	NC	-			R6	NC	-			R6	PL32A	6	T	
P5	NC	-			P5	NC	-			P5	PL32B	6	C	
P3	NC	-			P3	NC	-			P3	PL33A	6	T	
P4	NC	-			P4	NC	-			P4	PL33B	6	C	
R1	NC	-			R1	NC	-			R1	PL34A	6	T	
R2	NC	-			R2	NC	-			R2	PL34B	6	C	
R5	NC	-			R5	NC	-			R5	PL35A	6	T	
GND	-	-			-	-	-			GND	GND6	6		
R4	NC	-			R4	NC	-			R4	PL35B	6	C	
T1	NC	-			T1	NC	-			T1	NC	-		
T2	NC	-			T2	NC	-			T2	NC	-		
R3	NC	-			R3	NC	-			R3	NC	-		
T3	NC	-			T3	NC	-			T3	NC	-		
T5	TCK	6			T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6			U2	VCCJ	6		
V1	PL20A	6	T	LLM0_PLLT_IN_A	V1	PL29A	6	T	LLM0_PLLT_IN_A	V1	PL37A	6	T	LLM0_PLLT_IN_A
V2	PL20B	6	C	LLM0_PLLC_IN_A	V2	PL29B	6	C	LLM0_PLLC_IN_A	V2	PL37B	6	C	LLM0_PLLC_IN_A
U3	PL21A	6	T	LLM0_PLLT_FB_A	U3	PL30A	6	T	LLM0_PLLT_FB_A	U3	PL38A	6	T	LLM0_PLLT_FB_A
V3	PL21B	6	C	LLM0_PLLC_FB_A	V3	PL30B	6	C	LLM0_PLLC_FB_A	V3	PL38B	6	C	LLM0_PLLC_FB_A
U4	PL22A	6	T		U4	PL31A	6	T		U4	PL39A	6	T	
V5	PL22B	6	C		V5	PL31B	6	C		V5	PL39B	6	C	
W1	PL23A	6	T		W1	PL32A	6	T		W1	PL40A	6	T	
GND	GND6	6			GND	GND6	6			GND	GND6	6		
W2	PL23B	6	C		W2	PL32B	6	C		W2	PL40B	6	C	
Y1	PL24A	6	T	LDQS24	Y1	PL33A	6	T	LDQS33	Y1	PL41A	6	T	LDQS41
Y2	PL24B	6	C		Y2	PL33B	6	C		Y2	PL41B	6	C	
AA1	PL25A	6	T		AA1	PL34A	6	T		AA1	PL42A	6	T	
AA2	PL25B	6	C		AA2	PL34B	6	C		AA2	PL42B	6	C	
W4	PL26A	6	T		W4	PL35A	6	T		W4	PL43A	6	T	
V4	PL26B	6	C		V4	PL35B	6	C		V4	PL43B	6	C	
W3	PL27A	6	T	VREF1_6	W3	PL36A	6	T	VREF1_6	W3	PL44A	6	T	VREF1_6
Y3	PL27B	6	C	VREF2_6	Y3	PL36B	6	C	VREF2_6	Y3	PL44B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6			GND	GND6	6		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	**Ball Function**	**Bank**	**LVDS**	**Dual Function**	**Ball Number**	**Ball Function**	**Bank**	**LVDS**	**Dual Function**
N22	PR30A	3	T		N22	PR42A	3	T	
N19	PR29B	3	C		N19	PR41B	3	C	
N18	PR29A	3	T		N18	PR41A	3	T	
M21	PR28B	3	C		M21	PR40B	3	C	
L20	PR28A	3	T	RDQS28	L20	PR40A	3	T	RDQS40
L21	PR27B	3	C		L21	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M20	PR27A	3	T		M20	PR39A	3	T	
M18	PR26B	3	C		M18	PR38B	3	C	
M19	PR26A	3	T		M19	PR38A	3	T	
M22	PR25B	3	C		M22	PR37B	3	C	
L22	PR25A	3	T		L22	PR37A	3	T	
K22	PR24B	3	C		K22	PR36B	3	C	
K21	PR24A	3	T		K21	PR36A	3	T	
J22	PR22B	2	C	PCLKC2_0	J22	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
J21	PR22A	2	T	PCLKT2_0	J21	PR34A	2	T	PCLKT2_0
H22	PR21B	2	C		H22	PR33B	2	C	
H21	PR21A	2	T		H21	PR33A	2	T	
L19	PR20B	2	C		L19	PR32B	2	C	
L18	PR20A	2	T		L18	PR32A	2	T	
K20	PR19B	2	C		K20	PR31B	2	C	
J20	PR19A	2	T	RDQS19	J20	PR31A	2	T	RDQS31
K19	PR18B	2	C		K19	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
K18	PR18A	2	T		K18	PR30A	2	T	
G22	PR17B	2	C		G22	PR29B	2	C	
F22	PR17A	2	T		F22	PR29A	2	T	
F21	PR16B	2	C		F21	PR28B	2	C	
E22	PR16A	2	T		E22	PR28A	2	T	
E21	PR15B	2	C		E21	PR27B	2	C	
D22	PR15A	2	T		D22	PR27A	2	T	
G21	PR14B	2	C		G21	PR26B	2	C	
G20	PR14A	2	T		G20	PR26A	2	T	
GND	GND2	2			GND	GND2	2		
J18	PR13B	2	C		J18	PR25B	2	C	
H19	PR13A	2	T		H19	PR25A	2	T	
J19	PR12B	2	C		J19	PR24B	2	C	
H20	PR12A	2	T		H20	PR24A	2	T	
H17	PR11B	2	C		H17	PR23B	2	C	
H18	PR11A	2	T		H18	PR23A	2	T	RDQS23
D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
GND	-	-			GND	GND2	2		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A17	PT47A	1	T		A17	PT47A	1	T	
B15	PT46B	1	C		B15	PT46B	1	C	
A16	PT46A	1	T	TDQS46	A16	PT46A	1	T	TDQS46
A15	PT45B	1	C		A15	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
A14	PT45A	1	T		A14	PT45A	1	T	
G14	PT44B	1	C		G14	PT44B	1	C	
E15	PT44A	1	T		E15	PT44A	1	T	
D15	PT43B	1	C		D15	PT43B	1	C	
C15	PT43A	1	T		C15	PT43A	1	T	
C14	PT42B	1	C		C14	PT42B	1	C	
B14	PT42A	1	T		B14	PT42A	1	T	
A13	PT41B	1	C		A13	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
B13	PT41A	1	T		B13	PT41A	1	T	
E14	PT40B	1	C		E14	PT40B	1	C	
C13	PT40A	1	T		C13	PT40A	1	T	
F14	PT39B	1	C		F14	PT39B	1	C	
D14	PT39A	1	T		D14	PT39A	1	T	
E13	PT38B	1	C		E13	PT38B	1	C	
G13	PT38A	1	T	TDQS38	G13	PT38A	1	T	TDQS38
A12	PT37B	1	C		A12	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
B12	PT37A	1	T		B12	PT37A	1	T	
F13	PT36B	1	C		F13	PT36B	1	C	
D13	PT36A	1	T		D13	PT36A	1	T	
F12	PT35B	1	C	VREF2_1	F12	PT35B	1	C	VREF2_1
D12	PT35A	1	T	VREF1_1	D12	PT35A	1	T	VREF1_1
F11	PT34B	1	C		F11	PT34B	1	C	
C12	PT34A	1	T		C12	PT34A	1	T	
A11	PT33B	0	C	PCLKC0_0	A11	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A10	PT33A	0	T	PCLKT0_0	A10	PT33A	0	T	PCLKT0_0
E12	PT32B	0	C	VREF1_0	E12	PT32B	0	C	VREF1_0
E11	PT32A	0	T	VREF2_0	E11	PT32A	0	T	VREF2_0
B11	PT31B	0	C		B11	PT31B	0	C	
C11	PT31A	0	T		C11	PT31A	0	T	
B9	PT30B	0	C		B9	PT30B	0	C	
B10	PT30A	0	T	TDQS30	B10	PT30A	0	T	TDQS30
A9	PT29B	0	C		A9	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
A8	PT29A	0	T		A8	PT29A	0	T	
D11	PT28B	0	C		D11	PT28B	0	C	
C10	PT28A	0	T		C10	PT28A	0	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
L24	PR17A	2	T		L24	PR29A	2	T	
K25	PR16B	2	C		K25	PR28B	2	C	
J25	PR16A	2	T		J25	PR28A	2	T	
J26	PR15B	2	C		J26	PR27B	2	C	
H26	PR15A	2	T		H26	PR27A	2	T	
H25	PR14B	2	C		H25	PR26B	2	C	
GND	GND2	2			GND	GND2	2		
J24	PR14A	2	T		J24	PR26A	2	T	
K21	PR13B	2	C		K21	PR25B	2	C	
K22	PR13A	2	T		K22	PR25A	2	T	
K20	PR12B	2	C		K20	PR24B	2	C	
J20	PR12A	2	T		J20	PR24A	2	T	
K23	PR11B	2	C		K23	PR23B	2	C	
K24	PR11A	2	T		K24	PR23A	2	T	RDQS23
J21	NC	-			J21	PR22B	2	C	
-	-	-			GND	GND2	2		
J22	NC	-			J22	PR22A	2	T	
J23	NC	-			J23	PR21B	2	C	
H22	NC	-			H22	PR21A	2	T	
G26	NC	-			G26	PR20B	2	C	
F26	NC	-			F26	PR20A	2	T	
E26	NC	-			E26	PR19B	2	C	
E25	NC	-			E25	PR19A	2	T	
F25	PR9B	2	C	RUM0_PLLC_FB_A	F25	PR17B	2	C	RUM0_PLLC_FB_A
GND	GND2	2			GND	GND2	2		
G25	PR9A	2	T	RUM0_PLLT_FB_A	G25	PR17A	2	T	RUM0_PLLT_FB_A
H23	PR8B	2	C	RUM0_PLLC_IN_A	H23	PR16B	2	C	RUM0_PLLC_IN_A
H24	PR8A	2	T	RUM0_PLLT_IN_A	H24	PR16A	2	T	RUM0_PLLT_IN_A
H21	PR7B	2	C		H21	PR15B	2	C	
G21	PR7A	2	T		G21	PR15A	2	T	
D26	PR6B	2	C		D26	PR14B	2	C	
D25	PR6A	2	T	RDQS6	D25	PR14A	2	T	RDQS14
F21	PR5B	2	C		F21	PR13B	2	C	
-	-	-			GND	GND2	2		
G22	PR5A	2	T		G22	PR13A	2	T	
G24	PR4B	2	C		G24	PR12B	2	C	
G23	PR4A	2	T		G23	PR12A	2	T	
C26	PR3B	2	C		C26	PR11B	2	C	
C25	PR3A	2	T		C25	PR11A	2	T	
F24	NC	-			F24	PR9B	2	C	
-	-	-			GND	GND2	2		
F23	NC	-			F23	PR9A	2	T	

Date	Version	Section	Change Summary
December 2004	01.4	Architecture	Updated Hot Socketing Recommended Power Up Sequence section.
		Pinout Information	Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Pin Information
			Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Power Supply and NC Connections
			Added LFEC1 and LFEC3 100 TQFP Pinout
			Added LFEC1 and LFEC3 144 TQFP Pinout
			Added LFEC1, LFEC3 and LFECP/EC10 208 PQFP Pinout
			Added LFEC3, LFECP/EC10 and LFECP/EC15 256 fpBGA Pinout
			Added LFECP/EC10 and LFECP/EC15 484 fpBGA Pinout
		Ordering Information	Added Lead-Free Package Designators
			Added Lead-Free Ordering Part Numbers
		Supplemental Information	Updated list of technical notes.
April 2005	01.5	Architecture	EBR memory support section has been updated with clarification.
			Updated sysIO buffer pair section.
		DC & Switching Characteristics	Hot Socketing Specification has been updated.
			DC Electrical Characteristics table (I_{IL}, I_{IH}) has been updated.
			Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			External Switching Characteristics section has been updated.
			Removed t_{RSTW} spec. from PLL Parameter table.
			t_{RST} specifications have been updated.
			sysCONFIG Port Timing Specifications (t_{BSCL}, t_{IODISS}, t_{PRGMRJ}) have been updated.
		Pinout Information	Added LFECP/EC33 Pinout Information
			Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
			484-fpBGA logic connection has been updated (Ball # J6, J17, P6 and P17 for ECP/EC33 are now called VCCPLL).
			672-fpBGA logic connection has been updated (Ball # K19, L8, U19, U8 for ECP/EC33 are now called VCCPLL).
May 2005	01.6	Introduction	ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.
		Architecture	Table 2-10 has been updated (ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.)
			Recommended Power Up Sequence section has been removed.
		DC & Switching Characteristics	Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			Vos test condition has been updated to (VOP+VOM)/2.
			Register-to-Register performance table has been updated (rev. G 0.27).
			External switching characteristics have been updated (rev. G 0.27).
			Internal timing parameters have been updated (rev. G 0.27).
			Timing adders have been updated (rev. G 0.27).
			sysCONFIG port timing specifications have been updated.
		Pinout Information	Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	OPN list has been updated.