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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6100 |
| Total RAM Bits | 94208 |
| Number of I/O | 147 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp6e-3qn208c |

# Introduction

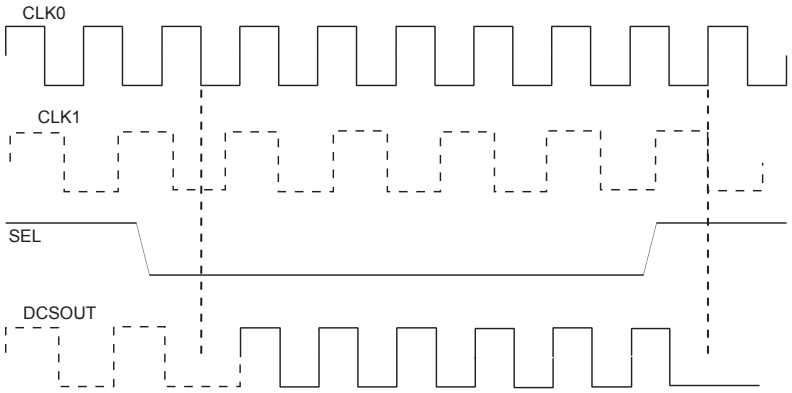
The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (EConomy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (EConomy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (EConomy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

*Figure 2-14. DCS Waveforms*




## sysMEM Memory

The LatticeECP/EC devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

*Table 2-6. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

## Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

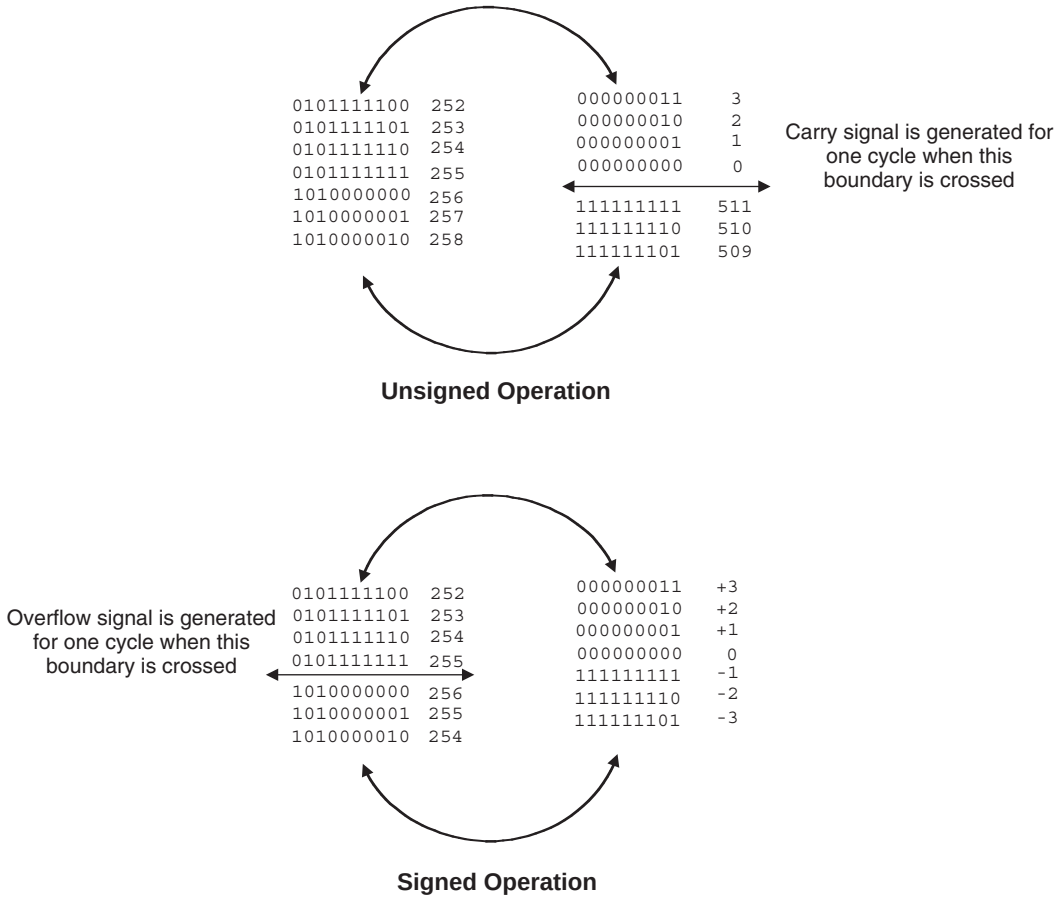
***Table 2-8. An Example of Sign Extension***

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9-Bits | Two's Complement Signed 18-bits |
|---|---|---|---|---|---|---|
| +5 | 0101 | 000000101 | 000000000000000101 | 0101 | 000000101 | 000000000000000101 |
| -6 | 0110 | 000000110 | 000000000000000110 | 1010 | 111111010 | 111111111111111010 |

## OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number then accumulator roll over is said to occur and overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-23.

***Figure 2-23. Accumulator Overflow/Underflow Conditions***



### Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

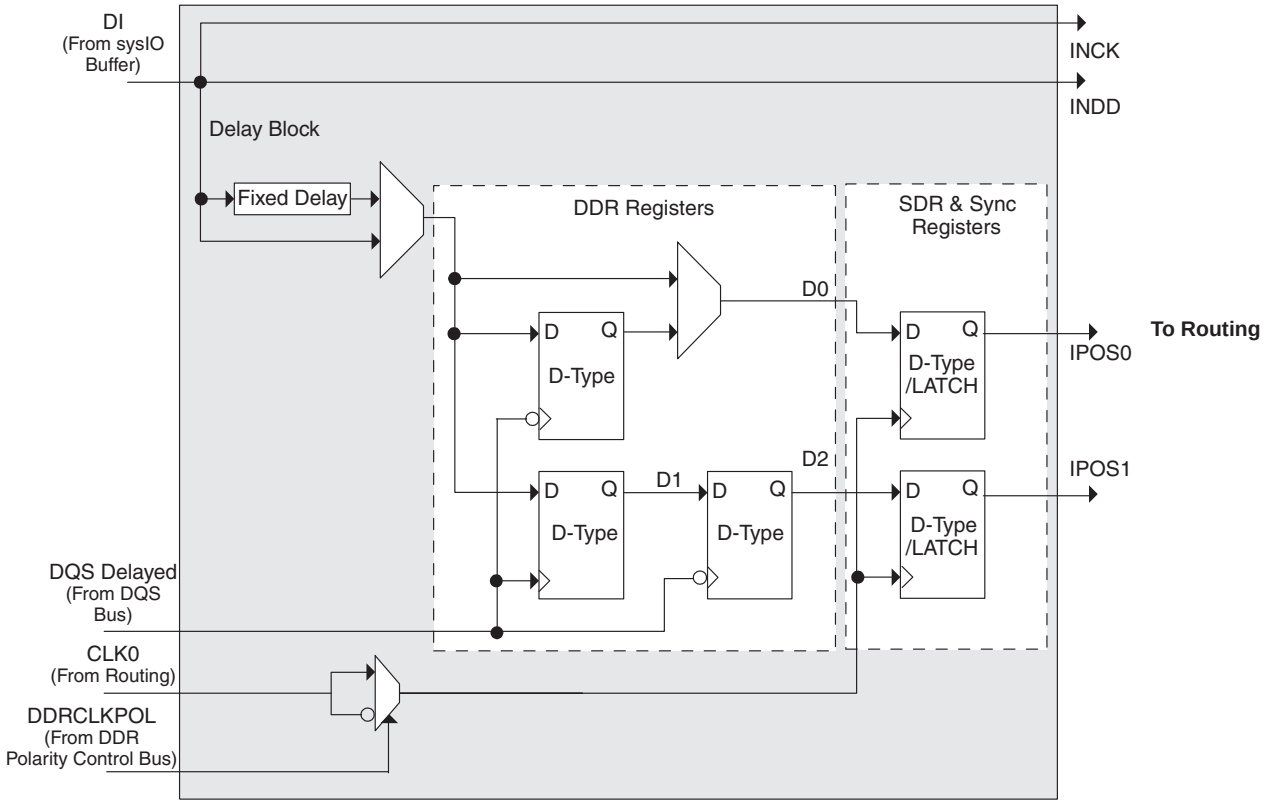
Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-27 shows the input register waveforms for DDR operation and Figure 2-28 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

***Figure 2-26. Input Register Diagram***



## Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master clock for configuration. The oscillator and the master clock run continuously. The default value of the master clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information about the use of this oscillator for configuration, please see the list of technical documentation at the end of this data sheet.

***Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration***

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|---|---|---|
| 2.5* | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |

# Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

# LatticeECP/EC Family Data Sheet DC and Switching Characteristics



## Absolute Maximum Ratings[1, 2, 3]

Supply Voltage $V_{CC}$ . . . . . -0.5 to 1.32V

Supply Voltage $V_{CCAUX}$ . . . . . -0.5 to 3.75V

Supply Voltage $V_{CCJ}$ . . . . . -0.5 to 3.75V

Output Supply Voltage $V_{CCIO}$ . . . . . -0.5 to 3.75V

Dedicated Input Voltage Applied[4] . . . . . -0.5 to 4.25V

I/O Tristate Voltage Applied [4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temp. (Tj) . . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | 1.14 | 1.26 | V |
| $V_{CCAUX}$[3] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCPLL}$ | PLL Supply Voltage for ECP/EC33 | 1.14 | 1.26 | V |
| $V_{CCIO}$[1, 2] | I/O Driver Supply Voltage | 1.140 | 3.465 | V |
| $V_{CCJ}$[1] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.140 | 3.465 | V |
| $t_{JCOM}$ | Junction Commercial Operation | 0 | 85 | °C |
| $t_{JIND}$ | Junction Industrial Operation | -40 | 100 | °C |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 1.2V, they must be connected to the same power supply as $V_{CC}$. If $V_{CCIO}$ or $V_{CCJ}$ is set to 3.3V, they must be connected to the same power supply as $V_{CCAUX}$.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCAUX}$ ramp rate must not exceed 3mV/µs for commercial and 0.6 mV/µs for industrial device operations during power up when transitioning between 0.8V and 1.8V.

## Hot Socketing Specifications[1, 2, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Top and Bottom General Purpose sysI/Os (Banks 0, 1, 4 and 5), JTAG and Dedicated sysCONFIG Pins** | | | | | | |
| $I_{DK\_TB}$ | Input or I/O Leakage Current | 0 ð $V_{IN}$ ð $V_{IH}$ (MAX.) | — | — | +/-1000 | µA |
| **Left and Right General Purpose sysI/Os (Banks 2, 3, 6 and 7)** | | | | | | |
| $I_{DK\_LR}$ | Input or I/O Leakage Current | $V_{IN}$ ð $V_{CCIO}$ | — | — | +/-1000 | µA |
| | | $V_{IN}$ > $V_{CCIO}$ | — | 35 | — | mA |

1. Insensitive to sequence of $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$.
2. 0 ð $V_{CC}$ ð $V_{CC}$ (MAX), 0 ð $V_{CCIO}$ ð $V_{CCIO}$ (MAX) or 0 ð $V_{CCAUX}$ ð $V_{CCAUX}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.

## sysI/O Recommended Operating Conditions

| Standard | $V_{CCIO}$ | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.465 | — | — | — |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18 Class I | 1.71 | 1.8 | 1.89 | 0.833 | 0.90 | 0.969 |
| SSTL2 Class I, II | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL3 Class I, II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL15 Class I | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL15 Class III | 1.425 | 1.5 | 1.575 | — | 0.9 | — |
| HSTL 18 Class I, II | 1.71 | 1.8 | 1.89 | — | 0.9 | — |
| HSTL 18 Class III | 1.71 | 1.8 | 1.89 | — | 1.08 | — |
| LVDS | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL[1] | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |

1. Outputs are implemented with the addition of external resistors. $V_{CCIO}$ applies to outputs only.

# sysI/O Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential input threshold | | +/-100 | — | — | mV |
| $V_{CM}$ | Input common mode voltage | 100mV ð $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.8 | V |
| | | 200mV ð $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.9 | V |
| | | 350mV ð $V_{THD}$ | $V_{THD}$/2 | 1.2 | 2.0 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 6 | mA |

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

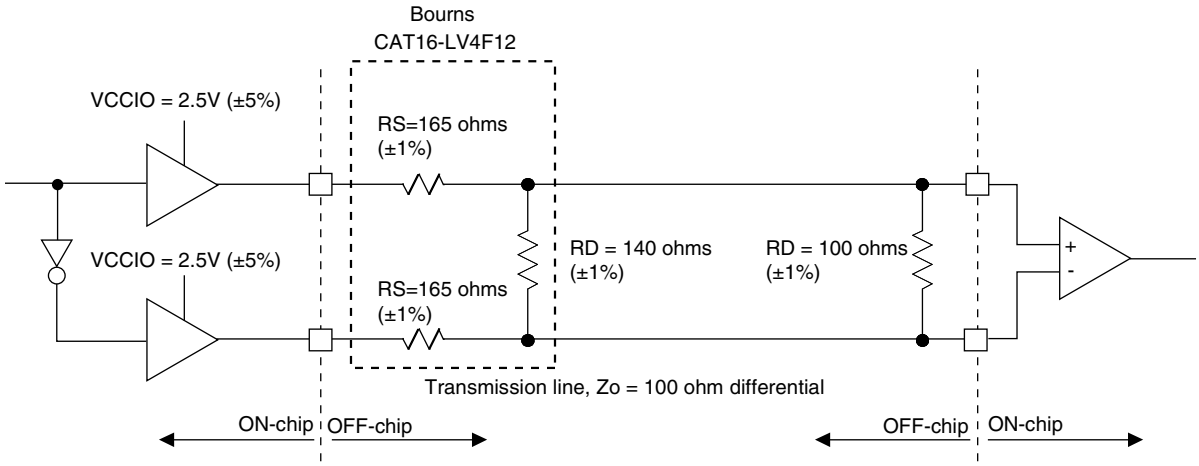



***Table 3-1. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.42 | V |
| $V_{OL}$ | Output low voltage | 1.08 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | ¾ |

## LatticeECP/EC Family Timing Adders[1, 2, 3]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25 | LVDS | 0.41 | 0.50 | 0.58 | ns |
| BLVDS25 | BLVDS | 0.41 | 0.50 | 0.58 | ns |
| LVPECL33 | LVPECL | 0.50 | 0.60 | 0.70 | ns |
| HSTL18_I | HSTL_18 class I | 0.41 | 0.49 | 0.57 | ns |
| HSTL18_II | HSTL_18 class II | 0.41 | 0.49 | 0.57 | ns |
| HSTL18_III | HSTL_18 class III | 0.41 | 0.49 | 0.57 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.37 | 0.44 | 0.52 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.37 | 0.44 | 0.52 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.37 | 0.44 | 0.52 | ns |
| HSTL15_I | HSTL_15 class I | 0.40 | 0.48 | 0.56 | ns |
| HSTL15_III | HSTL_15 class III | 0.40 | 0.48 | 0.56 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.37 | 0.44 | 0.51 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.37 | 0.44 | 0.51 | ns |
| SSTL33_I | SSTL_3 class I | 0.46 | 0.55 | 0.64 | ns |
| SSTL33_II | SSTL_3 class II | 0.46 | 0.55 | 0.64 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.39 | 0.47 | 0.55 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.39 | 0.47 | 0.55 | ns |
| SSTL25_I | SSTL_2 class I | 0.43 | 0.51 | 0.60 | ns |
| SSTL25_II | SSTL_2 class II | 0.43 | 0.51 | 0.60 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.38 | 0.45 | 0.53 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.38 | 0.45 | 0.53 | ns |
| SSTL18_I | SSTL_18 class I | 0.40 | 0.48 | 0.56 | ns |
| SSTL18D_I | Differential SSTL_18 class I | 0.37 | 0.44 | 0.51 | ns |
| LVTTL33 | LVTTL | 0.07 | 0.09 | 0.10 | ns |
| LVCMOS33 | LVCMOS 3.3 | 0.07 | 0.09 | 0.10 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS18 | LVCMOS 1.8 | 0.07 | 0.09 | 0.10 | ns |
| LVCMOS15 | LVCMOS 1.5 | 0.24 | 0.29 | 0.33 | ns |
| LVCMOS12 | LVCMOS 1.2 | 1.27 | 1.52 | 1.77 | ns |
| PCI33 | PCI | 0.07 | 0.09 | 0.10 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 E | 0.12 | 0.14 | 0.17 | ns |
| LVDS25 | LVDS 2.5 | -0.44 | -0.53 | -0.62 | ns |
| BLVDS25 | BLVDS 2.5 | 0.33 | 0.40 | 0.46 | ns |
| LVPECL33 | LVPECL 3.3 | 0.20 | 0.24 | 0.28 | ns |
| HSTL18_I | HSTL_18 class I | -0.10 | -0.12 | -0.14 | ns |
| HSTL18_II | HSTL_18 class II | 0.06 | 0.07 | 0.08 | ns |
| HSTL18_III | HSTL_18 class III | 0.15 | 0.19 | 0.22 | ns |
| HSTL18D_I | Differential HSTL 18 class I | -0.10 | -0.12 | -0.14 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.06 | 0.07 | 0.08 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.15 | 0.19 | 0.22 | ns |
| HSTL15_I | HSTL_15 class I | 0.08 | 0.10 | 0.11 | ns |

## LatticeECP/EC Family Timing Adders[1, 2, 3] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| HSTL15_II | HSTL_15 class II | 0.10 | 0.12 | 0.14 | ns |
| HSTL15_III | HSTL_15 class III | 0.10 | 0.12 | 0.14 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.08 | 0.10 | 0.11 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.10 | 0.12 | 0.14 | ns |
| SSTL33_I | SSTL_3 class I | -0.05 | -0.06 | -0.07 | ns |
| SSTL33_II | SSTL_3 class II | 0.40 | 0.48 | 0.56 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.05 | -0.06 | -0.07 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.40 | 0.48 | 0.56 | ns |
| SSTL25_I | SSTL_2 class I | 0.05 | 0.07 | 0.08 | ns |
| SSTL25_II | SSTL_2 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.05 | 0.07 | 0.08 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL18_I | SSTL_1.8 class I | 0.01 | 0.01 | 0.01 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.01 | 0.01 | 0.01 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.09 | 0.11 | 0.13 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | -0.03 | -0.04 | -0.05 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.36 | 0.43 | 0.51 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | 0.28 | 0.33 | 0.39 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.09 | 0.11 | 0.13 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | -0.03 | -0.04 | -0.05 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.36 | 0.43 | 0.51 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | 0.28 | 0.33 | 0.39 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.18 | 0.21 | 0.25 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.10 | 0.12 | 0.14 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.22 | 0.26 | 0.31 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | 0.14 | 0.16 | 0.19 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.15 | 0.18 | 0.21 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.06 | 0.08 | 0.09 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | 0.01 | 0.01 | 0.01 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.16 | 0.19 | 0.22 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.26 | 0.31 | 0.36 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.04 | 0.04 | 0.05 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.36 | 0.43 | 0.50 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.08 | 0.10 | 0.11 | ns |
| LVCMOS12_4mA | LVCMOS 1.2 4mA drive | 0.36 | 0.43 | 0.50 | ns |
| PCI33 | PCI33 | 1.05 | 1.26 | 1.46 | ns |

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Conditions table of this document.
3. All other standards according to the appropriate specification.

Timing v.G 0.30

## LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 85 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 86 | PB10A | 4 | T | WRITEN | PB18A | 4 | T | WRITEN |
| 87 | PB10B | 4 | C | CS1N | PB18B | 4 | C | CS1N |
| 88 | PB11A | 4 | T | VREF1_4 | PB19A | 4 | T | VREF1_4 |
| 89 | PB11B | 4 | C | CSN | PB19B | 4 | C | CSN |
| 90 | PB12A | 4 | T | VREF2_4 | PB20A | 4 | T | VREF2_4 |
| 91 | PB12B | 4 | C | D0/SPID7 | PB20B | 4 | C | D0/SPID7 |
| 92 | PB13A | 4 | T | D2/SPID5 | PB21A | 4 | T | D2/SPID5 |
| 93 | GND4 | 4 | | | GND4 | 4 | | |
| 94 | PB13B | 4 | C | D1/SPID6 | PB21B | 4 | C | D1/SPID6 |
| 95 | PB14A | 4 | T | BDQS14 | PB22A | 4 | T | BDQS22 |
| 96 | PB14B | 4 | C | D3/SPID4 | PB22B | 4 | C | D3/SPID4 |
| 97 | PB15A | 4 | T | | PB23A | 4 | T | |
| 98 | PB15B | 4 | C | D4/SPID3 | PB23B | 4 | C | D4/SPID3 |
| 99 | PB16A | 4 | T | | PB24A | 4 | T | |
| 100 | PB16B | 4 | C | D5/SPID2 | PB24B | 4 | C | D5/SPID2 |
| 101 | PB17A | 4 | T | | PB25A | 4 | T | |
| 102 | PB17B | 4 | C | D6/SPID1 | PB25B | 4 | C | D6/SPID1 |
| 103 | NC | - | | | NC | - | | |
| 104 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 105* | GND3<br>GND4 | - | | | GND3<br>GND4 | - | | |
| 106 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 107 | PR14B | 3 | C | VREF2_3 | PR18B | 3 | C | VREF2_3 |
| 108 | PR14A | 3 | T | VREF1_3 | PR18A | 3 | T | VREF1_3 |
| 109 | PR13B | 3 | C | | PR17B | 3 | C | |
| 110 | PR13A | 3 | T | | PR17A | 3 | T | |
| 111 | PR12B | 3 | C | | PR16B | 3 | C | |
| 112 | PR12A | 3 | T | | PR16A | 3 | T | |
| 113 | PR11B | 3 | C | | PR15B | 3 | C | |
| 114 | PR11A | 3 | T | RDQS11 | PR15A | 3 | T | RDQS15 |
| 115 | PR10B | 3 | C | RLM0_PLLC_FB_A | PR14B | 3 | C | RLM0_PLLC_FB_A |
| 116 | GND3 | 3 | | | GND3 | 3 | | |
| 117 | PR10A | 3 | T | RLM0_PLLT_FB_A | PR14A | 3 | T | RLM0_PLLT_FB_A |
| 118 | PR9B | 3 | C | RLM0_PLLC_IN_A | PR13B | 3 | C | RLM0_PLLC_IN_A |
| 119 | PR9A | 3 | T | RLM0_PLLT_IN_A | PR13A | 3 | T | RLM0_PLLT_IN_A |
| 120 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 121 | PR8B | 3 | C | DI/CSSPIN | PR12B | 3 | C | DI/CSSPIN |
| 122 | PR8A | 3 | T | DOUT/CSON | PR12A | 3 | T | DOUT/CSON |
| 123 | PR7B | 3 | C | BUSY/SISPI | PR11B | 3 | C | BUSY/SISPI |
| 124 | PR7A | 3 | T | D7/SPID0 | PR11A | 3 | T | D7/SPID0 |
| 125 | CFG2 | 3 | | | CFG2 | 3 | | |
| 126 | CFG1 | 3 | | | CFG1 | 3 | | |

# LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFECP10/LFEC10 | | | | LFECP15/LFEC15 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | LVDS | Dual Function | Ball Function | Bank | LVDS | Dual Function |
| N7 | PB18B | 5 | C | | PB18B | 5 | C | |
| R7 | PB19A | 5 | T | | PB19A | 5 | T | |
| R8 | PB19B | 5 | C | | PB19B | 5 | C | |
| M7 | PB20A | 5 | T | | PB20A | 5 | T | |
| M8 | PB20B | 5 | C | | PB20B | 5 | C | |
| T8 | PB21A | 5 | T | | PB21A | 5 | T | |
| GND | GND5 | 5 | | | GND5 | 5 | | |
| T9 | PB21B | 5 | C | | PB21B | 5 | C | |
| P8 | PB22A | 5 | T | BDQS22 | PB22A | 5 | T | BDQS22 |
| N8 | PB22B | 5 | C | | PB22B | 5 | C | |
| R9 | PB23A | 5 | T | | PB23A | 5 | T | |
| R10 | PB23B | 5 | C | | PB23B | 5 | C | |
| P9 | PB24A | 5 | T | VREF2_5 | PB24A | 5 | T | VREF2_5 |
| N9 | PB24B | 5 | C | VREF1_5 | PB24B | 5 | C | VREF1_5 |
| T10 | PB25A | 5 | T | PCLKT5_0 | PB25A | 5 | T | PCLKT5_0 |
| GND | GND5 | 5 | | | GND5 | 5 | | |
| T11 | PB25B | 5 | C | PCLKC5_0 | PB25B | 5 | C | PCLKC5_0 |
| T12 | PB26A | 4 | T | WRITEN | PB26A | 4 | T | WRITEN |
| T13 | PB26B | 4 | C | CS1N | PB26B | 4 | C | CS1N |
| P10 | PB27A | 4 | T | VREF1_4 | PB27A | 4 | T | VREF1_4 |
| N10 | PB27B | 4 | C | CSN | PB27B | 4 | C | CSN |
| T14 | PB28A | 4 | T | VREF2_4 | PB28A | 4 | T | VREF2_4 |
| T15 | PB28B | 4 | C | D0/SPID7 | PB28B | 4 | C | D0/SPID7 |
| M10 | PB29A | 4 | T | D2/SPID5 | PB29A | 4 | T | D2/SPID5 |
| GND | GND4 | 4 | | | GND4 | 4 | | |
| M11 | PB29B | 4 | C | D1/SPID6 | PB29B | 4 | C | D1/SPID6 |
| R11 | PB30A | 4 | T | BDQS30 | PB30A | 4 | T | BDQS30 |
| P11 | PB30B | 4 | C | D3/SPID4 | PB30B | 4 | C | D3/SPID4 |
| R13 | PB31A | 4 | T | | PB31A | 4 | T | |
| R14 | PB31B | 4 | C | D4/SPID3 | PB31B | 4 | C | D4/SPID3 |
| P12 | PB32A | 4 | T | | PB32A | 4 | T | |
| P13 | PB32B | 4 | C | D5/SPID2 | PB32B | 4 | C | D5/SPID2 |
| N11 | PB33A | 4 | T | | PB33A | 4 | T | |
| GND | GND4 | 4 | | | GND4 | 4 | | |
| N12 | PB33B | 4 | C | D6/SPID1 | PB33B | 4 | C | D6/SPID1 |
| R12 | PB34A | 4 | | | PB34A | 4 | | |
| GND | GND4 | 4 | | | GND4 | 4 | | |
| GND | GND4 | 4 | | | GND4 | 4 | | |
| - | - | - | | | GND4 | 4 | | |
| - | - | - | | | GND4 | 4 | | |
| GND | GND3 | 3 | | | GND3 | 3 | | |
| N13 | PR36B | 3 | C | VREF2_3 | PR44B | 3 | C | VREF2_3 |
| N14 | PR36A | 3 | T | VREF1_3 | PR44A | 3 | T | VREF1_3 |

# LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP6/LFEC6 | | | | | LFECP10/LFEC10 | | | | | LFECP/LFEC15 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| C21 | NC | - | | | C21 | PR5B | 2 | C | | C21 | PR5B | 2 | C | |
| C20 | NC | - | | | C20 | PR5A | 2 | T | | C20 | PR5A | 2 | T | |
| F18 | NC | - | | | F18 | PR4B | 2 | C | | F18 | PR4B | 2 | C | |
| E18 | NC | - | | | E18 | PR4A | 2 | T | | E18 | PR4A | 2 | T | |
| B22 | NC | - | | | B22 | PR3B | 2 | C | | B22 | PR3B | 2 | C | |
| B21 | NC | - | | | B21 | PR3A | 2 | T | | B21 | PR3A | 2 | T | |
| E19 | PR2B | 2 | C | VREF1_2 | E19 | PR2B | 2 | C | VREF1_2 | E19 | PR2B | 2 | C | VREF1_2 |
| D19 | PR2A | 2 | T | VREF2_2 | D19 | PR2A | 2 | T | VREF2_2 | D19 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| G17 | NC | - | | | G17 | NC | - | | | G17 | PT49B | 1 | C | |
| F17 | NC | - | | | F17 | NC | - | | | F17 | PT49A | 1 | T | |
| D18 | NC | - | | | D18 | NC | - | | | D18 | PT48B | 1 | C | |
| C18 | NC | - | | | C18 | NC | - | | | C18 | PT48A | 1 | T | |
| C19 | NC | - | | | C19 | NC | - | | | C19 | PT47B | 1 | C | |
| B20 | NC | - | | | B20 | NC | - | | | B20 | PT47A | 1 | T | |
| D17 | NC | - | | | D17 | NC | - | | | D17 | PT46B | 1 | C | |
| C16 | NC | - | | | C16 | NC | - | | | C16 | PT46A | 1 | T | TDQS46 |
| B19 | NC | - | | | B19 | NC | - | | | B19 | PT45B | 1 | C | |
| GND | - | - | | | GND | - | - | | | GND | GND1 | 1 | | |
| A20 | NC | - | | | A20 | NC | - | | | A20 | PT45A | 1 | T | |
| E17 | NC | - | | | E17 | NC | - | | | E17 | PT44B | 1 | C | |
| C17 | NC | - | | | C17 | NC | - | | | C17 | PT44A | 1 | T | |
| F16 | NC | - | | | F16 | NC | - | | | F16 | PT43B | 1 | C | |
| E16 | NC | - | | | E16 | NC | - | | | E16 | PT43A | 1 | T | |
| F15 | NC | - | | | F15 | NC | - | | | F15 | PT42B | 1 | C | |
| D16 | NC | - | | | D16 | NC | - | | | D16 | PT42A | 1 | T | |
| B18 | PT33B | 1 | C | | B18 | PT41B | 1 | C | | B18 | PT41B | 1 | C | |
| GND | - | - | | | GND | - | - | | | GND | GND1 | 1 | | |
| A19 | PT33A | 1 | T | | A19 | PT41A | 1 | T | | A19 | PT41A | 1 | T | |
| B17 | PT32B | 1 | C | | B17 | PT40B | 1 | C | | B17 | PT40B | 1 | C | |
| A18 | PT32A | 1 | T | | A18 | PT40A | 1 | T | | A18 | PT40A | 1 | T | |
| B16 | PT31B | 1 | C | | B16 | PT39B | 1 | C | | B16 | PT39B | 1 | C | |
| A17 | PT31A | 1 | T | | A17 | PT39A | 1 | T | | A17 | PT39A | 1 | T | |
| B15 | PT30B | 1 | C | | B15 | PT38B | 1 | C | | B15 | PT38B | 1 | C | |
| A16 | PT30A | 1 | T | TDQS30 | A16 | PT38A | 1 | T | TDQS38 | A16 | PT38A | 1 | T | TDQS38 |
| A15 | PT29B | 1 | C | | A15 | PT37B | 1 | C | | A15 | PT37B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A14 | PT29A | 1 | T | | A14 | PT37A | 1 | T | | A14 | PT37A | 1 | T | |
| G14 | PT28B | 1 | C | | G14 | PT36B | 1 | C | | G14 | PT36B | 1 | C | |
| E15 | PT28A | 1 | T | | E15 | PT36A | 1 | T | | E15 | PT36A | 1 | T | |
| D15 | PT27B | 1 | C | | D15 | PT35B | 1 | C | | D15 | PT35B | 1 | C | |
| C15 | PT27A | 1 | T | | C15 | PT35A | 1 | T | | C15 | PT35A | 1 | T | |
| C14 | PT26B | 1 | C | | C14 | PT34B | 1 | C | | C14 | PT34B | 1 | C | |
| B14 | PT26A | 1 | T | | B14 | PT34A | 1 | T | | B14 | PT34A | 1 | T | |
| A13 | PT25B | 1 | C | | A13 | PT33B | 1 | C | | A13 | PT33B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B13 | PT25A | 1 | T | | B13 | PT33A | 1 | T | | B13 | PT33A | 1 | T | |
| E14 | PT24B | 1 | C | | E14 | PT32B | 1 | C | | E14 | PT32B | 1 | C | |
| C13 | PT24A | 1 | T | | C13 | PT32A | 1 | T | | C13 | PT32A | 1 | T | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| D4 | PL2A | 7 | T | VREF2_7 | D4 | PL2A | 7 | T | VREF2_7 |
| E4 | PL2B | 7 | C | VREF1_7 | E4 | PL2B | 7 | C | VREF1_7 |
| GND | - | - | | | GND | GND7 | 7 | | |
| C3 | PL3A | 7 | T | | C3 | PL10A | 7 | T | |
| B2 | PL3B | 7 | C | | B2 | PL10B | 7 | C | |
| E5 | PL4A | 7 | T | | E5 | PL11A | 7 | T | |
| F5 | PL4B | 7 | C | | F5 | PL11B | 7 | C | |
| D3 | PL5A | 7 | T | | D3 | PL12A | 7 | T | |
| C2 | PL5B | 7 | C | | C2 | PL12B | 7 | C | |
| GND | - | - | | | GND | GND7 | 7 | | |
| F4 | PL6A | 7 | T | LDQS6 | F4 | PL14A | 7 | T | LDQS14 |
| G4 | PL6B | 7 | C | | G4 | PL14B | 7 | C | |
| E3 | PL7A | 7 | T | | E3 | PL15A | 7 | T | |
| D2 | PL7B | 7 | C | | D2 | PL15B | 7 | C | |
| B1 | PL8A | 7 | T | LUM0_PLLT_IN_A | B1 | PL16A | 7 | T | LUM0_PLLT_IN_A |
| C1 | PL8B | 7 | C | LUM0_PLLC_IN_A | C1 | PL16B | 7 | C | LUM0_PLLC_IN_A |
| F3 | PL9A | 7 | T | LUM0_PLLT_FB_A | F3 | PL17A | 7 | T | LUM0_PLLT_FB_A |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| E2 | PL9B | 7 | C | LUM0_PLLC_FB_A | E2 | PL17B | 7 | C | LUM0_PLLC_FB_A |
| GND | - | - | | | GND | GND7 | 7 | | |
| G5 | PL11A | 7 | T | | G5 | PL23A | 7 | T | LDQS23 |
| H6 | PL11B | 7 | C | | H6 | PL23B | 7 | C | |
| G3 | PL12A | 7 | T | | G3 | PL24A | 7 | T | |
| H4 | PL12B | 7 | C | | H4 | PL24B | 7 | C | |
| J5 | PL13A | 7 | T | | J5 | PL25A | 7 | T | |
| H5 | PL13B | 7 | C | | H5 | PL25B | 7 | C | |
| F2 | PL14A | 7 | T | | F2 | PL26A | 7 | T | |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| F1 | PL14B | 7 | C | | F1 | PL26B | 7 | C | |
| E1 | PL15A | 7 | T | | E1 | PL27A | 7 | T | |
| D1 | PL15B | 7 | C | | D1 | PL27B | 7 | C | |
| H3 | PL16A | 7 | T | | H3 | PL28A | 7 | T | |
| G2 | PL16B | 7 | C | | G2 | PL28B | 7 | C | |
| H2 | PL17A | 7 | T | | H2 | PL29A | 7 | T | |
| G1 | PL17B | 7 | C | | G1 | PL29B | 7 | C | |
| J4 | PL18A | 7 | T | | J4 | PL30A | 7 | T | |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| J3 | PL18B | 7 | C | | J3 | PL30B | 7 | C | |
| J2 | PL19A | 7 | T | LDQS19 | J2 | PL31A | 7 | T | LDQS31 |
| H1 | PL19B | 7 | C | | H1 | PL31B | 7 | C | |
| K4 | PL20A | 7 | T | | K4 | PL32A | 7 | T | |
| K5 | PL20B | 7 | C | | K5 | PL32B | 7 | C | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| N22 | PR30A | 3 | T | | N22 | PR42A | 3 | T | |
| N19 | PR29B | 3 | C | | N19 | PR41B | 3 | C | |
| N18 | PR29A | 3 | T | | N18 | PR41A | 3 | T | |
| M21 | PR28B | 3 | C | | M21 | PR40B | 3 | C | |
| L20 | PR28A | 3 | T | RDQS28 | L20 | PR40A | 3 | T | RDQS40 |
| L21 | PR27B | 3 | C | | L21 | PR39B | 3 | C | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| M20 | PR27A | 3 | T | | M20 | PR39A | 3 | T | |
| M18 | PR26B | 3 | C | | M18 | PR38B | 3 | C | |
| M19 | PR26A | 3 | T | | M19 | PR38A | 3 | T | |
| M22 | PR25B | 3 | C | | M22 | PR37B | 3 | C | |
| L22 | PR25A | 3 | T | | L22 | PR37A | 3 | T | |
| K22 | PR24B | 3 | C | | K22 | PR36B | 3 | C | |
| K21 | PR24A | 3 | T | | K21 | PR36A | 3 | T | |
| J22 | PR22B | 2 | C | PCLKC2_0 | J22 | PR34B | 2 | C | PCLKC2_0 |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| J21 | PR22A | 2 | T | PCLKT2_0 | J21 | PR34A | 2 | T | PCLKT2_0 |
| H22 | PR21B | 2 | C | | H22 | PR33B | 2 | C | |
| H21 | PR21A | 2 | T | | H21 | PR33A | 2 | T | |
| L19 | PR20B | 2 | C | | L19 | PR32B | 2 | C | |
| L18 | PR20A | 2 | T | | L18 | PR32A | 2 | T | |
| K20 | PR19B | 2 | C | | K20 | PR31B | 2 | C | |
| J20 | PR19A | 2 | T | RDQS19 | J20 | PR31A | 2 | T | RDQS31 |
| K19 | PR18B | 2 | C | | K19 | PR30B | 2 | C | |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| K18 | PR18A | 2 | T | | K18 | PR30A | 2 | T | |
| G22 | PR17B | 2 | C | | G22 | PR29B | 2 | C | |
| F22 | PR17A | 2 | T | | F22 | PR29A | 2 | T | |
| F21 | PR16B | 2 | C | | F21 | PR28B | 2 | C | |
| E22 | PR16A | 2 | T | | E22 | PR28A | 2 | T | |
| E21 | PR15B | 2 | C | | E21 | PR27B | 2 | C | |
| D22 | PR15A | 2 | T | | D22 | PR27A | 2 | T | |
| G21 | PR14B | 2 | C | | G21 | PR26B | 2 | C | |
| G20 | PR14A | 2 | T | | G20 | PR26A | 2 | T | |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| J18 | PR13B | 2 | C | | J18 | PR25B | 2 | C | |
| H19 | PR13A | 2 | T | | H19 | PR25A | 2 | T | |
| J19 | PR12B | 2 | C | | J19 | PR24B | 2 | C | |
| H20 | PR12A | 2 | T | | H20 | PR24A | 2 | T | |
| H17 | PR11B | 2 | C | | H17 | PR23B | 2 | C | |
| H18 | PR11A | 2 | T | | H18 | PR23A | 2 | T | RDQS23 |
| D21 | PR9B | 2 | C | RUM0_PLLC_FB_A | D21 | PR17B | 2 | C | RUM0_PLLC_FB_A |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| GND | - | - | | | GND | GND2 | 2 | | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| AF22 | PB51A | 4 | T | | AF22 | PB51A | 4 | T | |
| AB17 | PB51B | 4 | C | | AB17 | PB51B | 4 | C | |
| AE22 | PB52A | 4 | T | | AE22 | PB52A | 4 | T | |
| AA18 | PB52B | 4 | C | | AA18 | PB52B | 4 | C | |
| AE19 | PB53A | 4 | T | | AE19 | PB53A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AE20 | PB53B | 4 | C | | AE20 | PB53B | 4 | C | |
| AA19 | PB54A | 4 | T | BDQS54 | AA19 | PB54A | 4 | T | BDQS54 |
| Y18 | PB54B | 4 | C | | Y18 | PB54B | 4 | C | |
| AF23 | PB55A | 4 | T | | AF23 | PB55A | 4 | T | |
| AA20 | PB55B | 4 | C | | AA20 | PB55B | 4 | C | |
| AC18 | PB56A | 4 | T | | AC18 | PB56A | 4 | T | |
| AB18 | PB56B | 4 | C | | AB18 | PB56B | 4 | C | |
| AF24 | PB57A | 4 | T | | AF24 | PB57A | 4 | T | |
| - | - | - | | | GND | GND4 | 4 | | |
| AE23 | PB57B | 4 | C | | AE23 | PB57B | 4 | C | |
| AD19 | NC | - | | | AD19 | PB58A | 4 | T | |
| AD20 | NC | - | | | AD20 | PB58B | 4 | C | |
| AC19 | NC | - | | | AC19 | PB59A | 4 | T | |
| AB19 | NC | - | | | AB19 | PB59B | 4 | C | |
| AD21 | NC | - | | | AD21 | PB60A | 4 | T | |
| AC20 | NC | - | | | AC20 | PB60B | 4 | C | |
| AF25 | NC | - | | | AF25 | PB61A | 4 | T | |
| - | - | - | | | GND | GND4 | 4 | | |
| AE25 | NC | - | | | AE25 | PB61B | 4 | C | |
| AB21 | NC | - | | | AB21 | PB62A | 4 | T | BDQS62 |
| AB20 | NC | - | | | AB20 | PB62B | 4 | C | |
| AE24 | NC | - | | | AE24 | PB63A | 4 | T | |
| AD23 | NC | - | | | AD23 | PB63B | 4 | C | |
| AD22 | NC | - | | | AD22 | PB64A | 4 | T | |
| AC21 | NC | - | | | AC21 | PB64B | 4 | C | |
| AC22 | NC | - | | | AC22 | PB65A | 4 | T | |
| AB22 | NC | - | | | AB22 | PB65B | 4 | C | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| AC23 | PR48B | 3 | C | VREF2_3 | AC23 | PR68B | 3 | C | VREF2_3 |
| AC24 | PR48A | 3 | T | VREF1_3 | AC24 | PR68A | 3 | T | VREF1_3 |
| AD24 | NC | - | | | AD24 | PR67B | 3 | C | |
| AD25 | NC | - | | | AD25 | PR67A | 3 | T | |
| AE26 | NC | - | | | AE26 | PR66B | 3 | C | |
| AD26 | NC | - | | | AD26 | PR66A | 3 | T | |
| Y20 | NC | - | | | Y20 | PR65B | 3 | C | |

# LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| Y19 | NC | - | | | Y19 | PR65A | 3 | T | RDQS65 |
| AA23 | NC | - | | | AA23 | PR64B | 3 | C | |
| - | - | - | | | GND | GND3 | 3 | | |
| AA22 | NC | - | | | AA22 | PR64A | 3 | T | |
| AB23 | NC | - | | | AB23 | PR63B | 3 | C | |
| AB24 | NC | - | | | AB24 | PR63A | 3 | T | |
| Y21 | NC | - | | | Y21 | PR62B | 3 | C | |
| AA21 | NC | - | | | AA21 | PR62A | 3 | T | |
| Y23 | NC | - | | | Y23 | PR61B | 3 | C | |
| Y22 | NC | - | | | Y22 | PR61A | 3 | T | |
| AA24 | NC | - | | | AA24 | PR60B | 3 | C | |
| - | - | - | | | GND | GND3 | 3 | | |
| Y24 | NC | - | | | Y24 | PR60A | 3 | T | |
| AC25 | PR47B | 3 | C | | AC25 | PR59B | 3 | C | |
| AC26 | PR47A | 3 | T | | AC26 | PR59A | 3 | T | |
| AB25 | PR46B | 3 | C | | AB25 | PR58B | 3 | C | |
| AA25 | PR46A | 3 | T | | AA25 | PR58A | 3 | T | |
| AB26 | PR45B | 3 | C | | AB26 | PR57B | 3 | C | |
| AA26 | PR45A | 3 | T | RDQS45 | AA26 | PR57A | 3 | T | RDQS57 |
| W23 | PR44B | 3 | C | RLM0_PLLC_IN_A | W23 | PR56B | 3 | C | RLM0_PLLC_IN_A |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| W24 | PR44A | 3 | T | RLM0_PLLT_IN_A | W24 | PR56A | 3 | T | RLM0_PLLT_IN_A |
| W22 | PR43B | 3 | C | RLM0_PLLC_FB_A | W22 | PR55B | 3 | C | RLM0_PLLC_FB_A |
| W21 | PR43A | 3 | T | RLM0_PLLT_FB_A | W21 | PR55A | 3 | T | RLM0_PLLT_FB_A |
| Y25 | PR42B | 3 | C | DI/CSSPIN | Y25 | PR54B | 3 | C | DI/CSSPIN |
| Y26 | PR42A | 3 | T | DOUT/CSON | Y26 | PR54A | 3 | T | DOUT/CSON |
| W25 | PR41B | 3 | C | BUSY/SISPI | W25 | PR53B | 3 | C | BUSY/SISPI |
| W26 | PR41A | 3 | T | D7/SPID0 | W26 | PR53A | 3 | T | D7/SPID0 |
| V24 | CFG2 | 3 | | | V24 | CFG2 | 3 | | |
| V21 | CFG1 | 3 | | | V21 | CFG1 | 3 | | |
| V23 | CFG0 | 3 | | | V23 | CFG0 | 3 | | |
| V22 | PROGRAMN | 3 | | | V22 | PROGRAMN | 3 | | |
| V20 | CCLK | 3 | | | V20 | CCLK | 3 | | |
| V25 | INITN | 3 | | | V25 | INITN | 3 | | |
| U20 | DONE | 3 | | | U20 | DONE | 3 | | |
| V26 | PR39B | 3 | C | | V26 | PR51B | 3 | C | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| U26 | PR39A | 3 | T | | U26 | PR51A | 3 | T | |
| U24 | PR38B | 3 | C | | U24 | PR50B | 3 | C | |
| U25 | PR38A | 3 | T | | U25 | PR50A | 3 | T | |
| U23 | PR37B | 3 | C | | U23 | PR49B | 3 | C | |
| U22 | PR37A | 3 | T | | U22 | PR49A | 3 | T | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| M10 | GND | - | | | M10 | GND | - | | |
| M11 | GND | - | | | M11 | GND | - | | |
| M12 | GND | - | | | M12 | GND | - | | |
| M13 | GND | - | | | M13 | GND | - | | |
| M14 | GND | - | | | M14 | GND | - | | |
| M15 | GND | - | | | M15 | GND | - | | |
| M16 | GND | - | | | M16 | GND | - | | |
| M17 | GND | - | | | M17 | GND | - | | |
| N10 | GND | - | | | N10 | GND | - | | |
| N11 | GND | - | | | N11 | GND | - | | |
| N12 | GND | - | | | N12 | GND | - | | |
| N13 | GND | - | | | N13 | GND | - | | |
| N14 | GND | - | | | N14 | GND | - | | |
| N15 | GND | - | | | N15 | GND | - | | |
| N16 | GND | - | | | N16 | GND | - | | |
| N17 | GND | - | | | N17 | GND | - | | |
| P10 | GND | - | | | P10 | GND | - | | |
| P11 | GND | - | | | P11 | GND | - | | |
| P12 | GND | - | | | P12 | GND | - | | |
| P13 | GND | - | | | P13 | GND | - | | |
| P14 | GND | - | | | P14 | GND | - | | |
| P15 | GND | - | | | P15 | GND | - | | |
| P16 | GND | - | | | P16 | GND | - | | |
| P17 | GND | - | | | P17 | GND | - | | |
| R10 | GND | - | | | R10 | GND | - | | |
| R11 | GND | - | | | R11 | GND | - | | |
| R12 | GND | - | | | R12 | GND | - | | |
| R13 | GND | - | | | R13 | GND | - | | |
| R14 | GND | - | | | R14 | GND | - | | |
| R15 | GND | - | | | R15 | GND | - | | |
| R16 | GND | - | | | R16 | GND | - | | |
| R17 | GND | - | | | R17 | GND | - | | |
| T10 | GND | - | | | T10 | GND | - | | |
| T11 | GND | - | | | T11 | GND | - | | |
| T12 | GND | - | | | T12 | GND | - | | |
| T13 | GND | - | | | T13 | GND | - | | |
| T14 | GND | - | | | T14 | GND | - | | |
| T15 | GND | - | | | T15 | GND | - | | |
| T16 | GND | - | | | T16 | GND | - | | |
| T17 | GND | - | | | T17 | GND | - | | |
| U10 | GND | - | | | U10 | GND | - | | |
| U11 | GND | - | | | U11 | GND | - | | |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| September 2005 | 02.0 | Architecture | sysIO section has been updated. |
| | | DC & Switching Characteristics | Recommended Operating Conditions has been updated with $V_{CCPLL}$. |
| | | | DC Electrical Characteristics table has been updated |
| | | | Removed 5V Tolerant Input Buffer section. |
| | | | Register-to-Register performance table has been updated (rev. G 0.28). |
| | | | LatticeECP/EC External Switching Characteristics table has been updated (rev. G 0.28). |
| | | | LatticeECP/EC Internal Switching Characteristics table has been updated (rev. G 0.28). |
| | | | LatticeECP/EC Family Timing Adders have been updated (rev. G 0.28). |
| | | | sysCLOCK PLL timing table has been updated (rev. G 0.28) |
| | | | LatticeECP/EC sysCONFIG Port Timing specification table has been updated (rev. G 0.28). |
| | | | Master Clock table has been updated (rev. G 0.28). |
| | | | JTAG Port Timing specification table has been updated (rev. G 0.28). |
| | | Pinout Information | Signal Description table has been updated with $V_{CCPLL}$. |
| November 2005 | 02.1 | DC & Switching Characteristics | Pin-to-Pin Performance table has been updated (G 0.30)<br>- 4:1MUX, 8:1MUX, 16:1MUX, 32:1MUX<br>Register-to-Register Performance (G 0.30) - No timing number changes. |
| | | | External Switching Characteristics (G 0.30) - No timing number changes. |
| | | | Internal Switching Characteristics (G 0.30)<br>-$t_{SUP\_DSP}$, $t_{HP\_DSP}$, $t_{SUO\_DSP}$, $t_{HO\_DSP}$, $t_{COI\_DSP}$, $t_{COD\_DSP}$ numbers have been updated. |
| | | | Family Timing Adders (G 0.30) - No timing number changes. |
| | | | sysCLOCK PLL Timing (G 0.30) - No timing number changes. |
| | | | sysCONFIG Port Timing Specifications (G 0.30) - No timing number changes. |
| | | | Master Clock (G 0.30) - No timing number changes. |
| | | | JTAG Port Timing Specification (G 0.30) - No timing number changes. |
| | | Ordering Information | Added 208-PQFP lead-free part numbers. |
| March 2006 | 02.2 | DC & Switching Characteristics | Added footnote 3. to $V_{CCAUX}$ in the Recommended Operating Conditions table. |
| January 2007 | 02.3 | Architecture | EBR Asynchronous Reset section added. |
| February 2007 | 02.4 | Architecture | Updated EBR Asynchronous Reset section. |
| | | | Updated Maximum Number of Elements in a Block table - MAC value for x9 changed to 2. |
| May 2007 | 02.5 | Architecture | Updated text in Ripple Mode section. |
| November 2007 | 02.6 | DC & Switching Characteristics | Added JTAG Port Waveforms diagram. |
| | | | Updated $t_{RST}$ timing information in the sysCLOCK PLL Timing table. |
| | | Pinout Information | Added Thermal Management text section. |
| | | Supplemental Information | Updated title list. |
| February 2008 | 02.7 | DC & Switching Characteristics | Read/Write Mode (Normal) and Read/Write Mode with Input and Output Registers waveforms in the EBR Memory Timing Diagrams section have been updated. |
| September 2012 | 02.8 | All | Updated document with new corporate logo. |