# Lattice Semiconductor Corporation - LFECP6E-4FN256C Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6100 |
| Total RAM Bits | 94208 |
| Number of I/O | 195 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp6e-4fn256c |

*Figure 2-4. Slice Diagram*

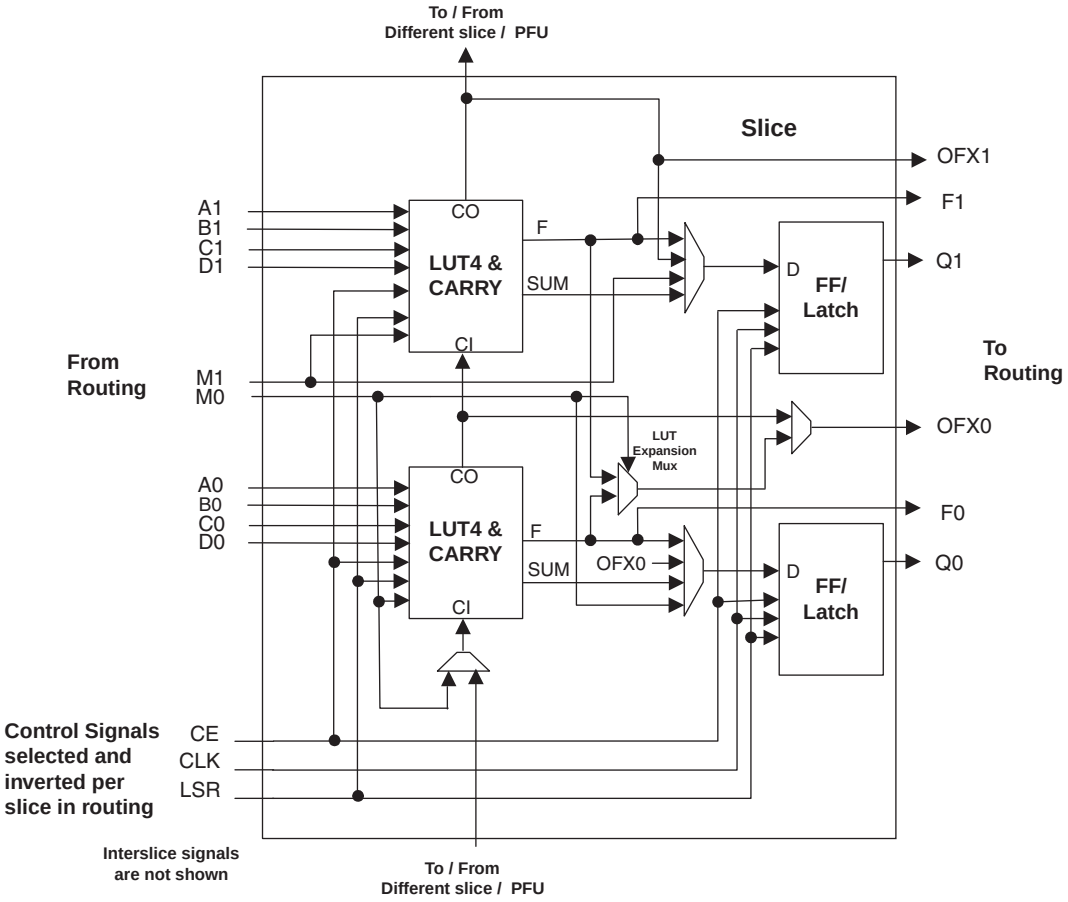



*Table 2-1. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

## Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, the routing of both short and long connections between PFUs.

The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

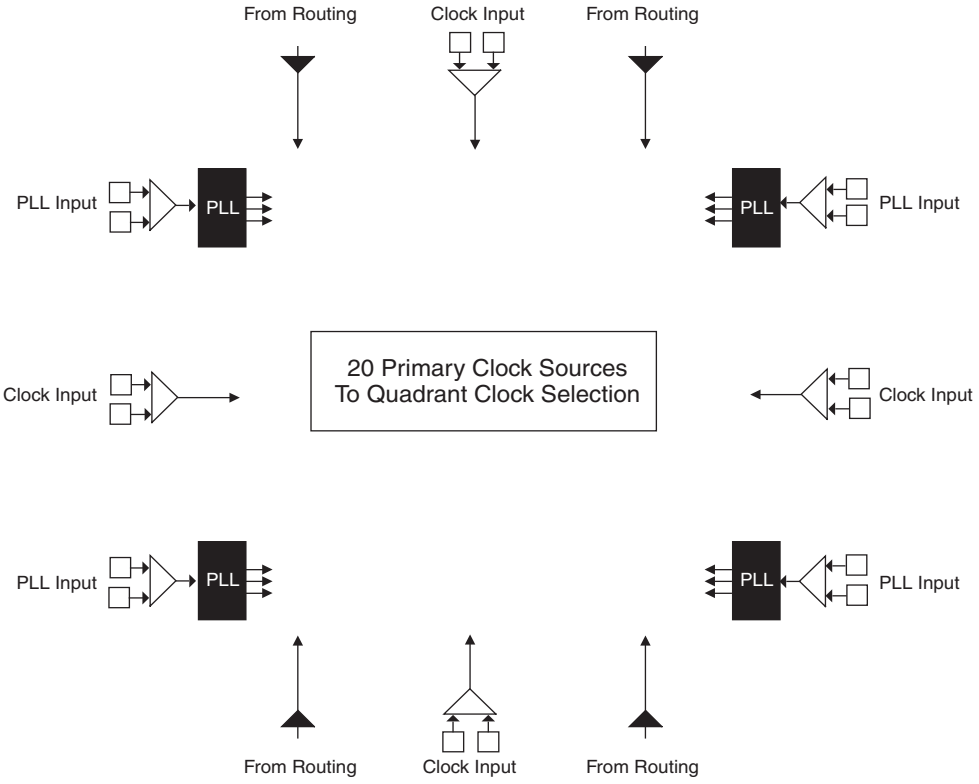
## Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

### Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

***Figure 2-6. Primary Clock Sources***




Note: Smaller devices have two PLLs.

*Table 2-7. Maximum Number of Elements in a Block*

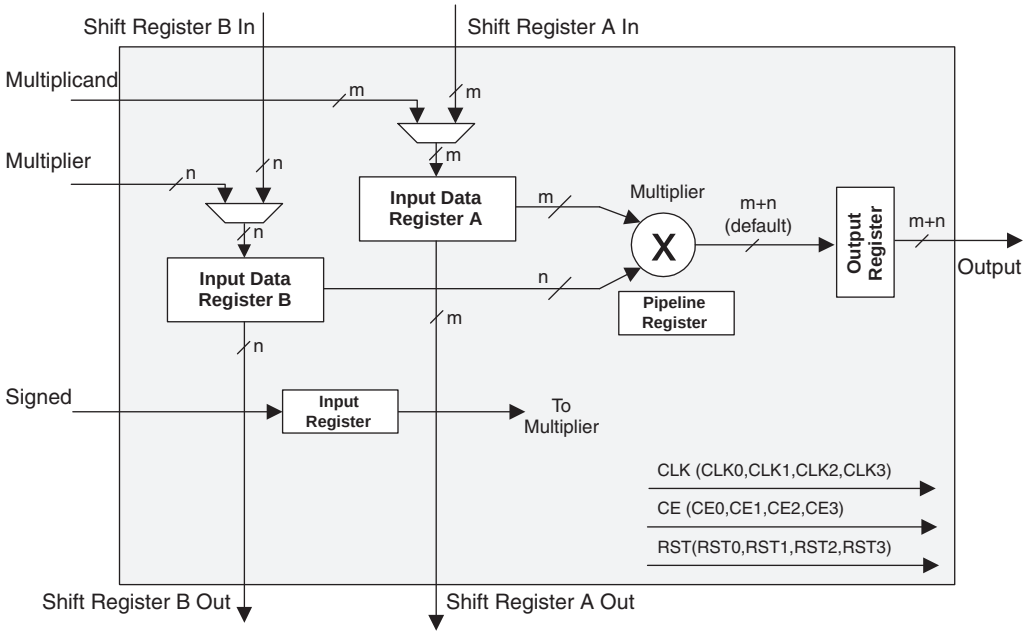
| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADD | 4 | 2 | — |
| MULTADDSUM | 2 | 1 | — |

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift registers from previous operand registers. In addition by selecting “dynamic operation” in the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle. Similarly by selecting ‘Dynamic operation’ in the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.

## MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-19 shows the MULT sysDSP element.

*Figure 2-19. MULT sysDSP Element*



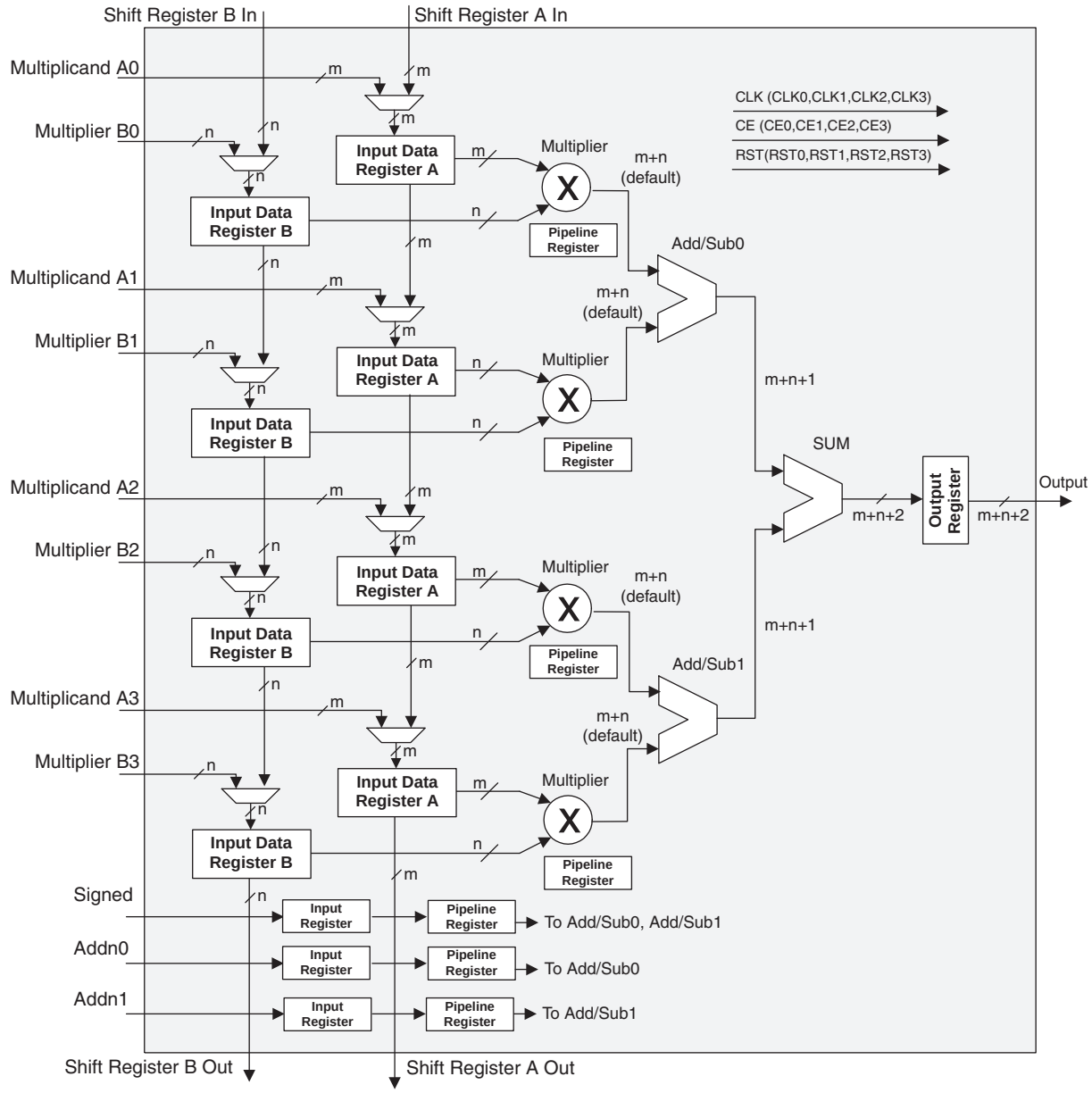

## MAC sysDSP Element

In this case the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-20 shows the MAC sysDSP element.

## MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUM sysDSP element.

***Figure 2-22. MULTADDSUM***




## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

## Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

***Table 2-8. An Example of Sign Extension***

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9-Bits | Two's Complement Signed 18-bits |
|---|---|---|---|---|---|---|
| +5 | 0101 | 000000101 | 000000000000000101 | 0101 | 000000101 | 000000000000000101 |
| -6 | 0110 | 000000110 | 000000000000000110 | 1010 | 111111010 | 111111111111111010 |

## OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number then accumulator roll over is said to occur and overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-23.

***Figure 2-23. Accumulator Overflow/Underflow Conditions***

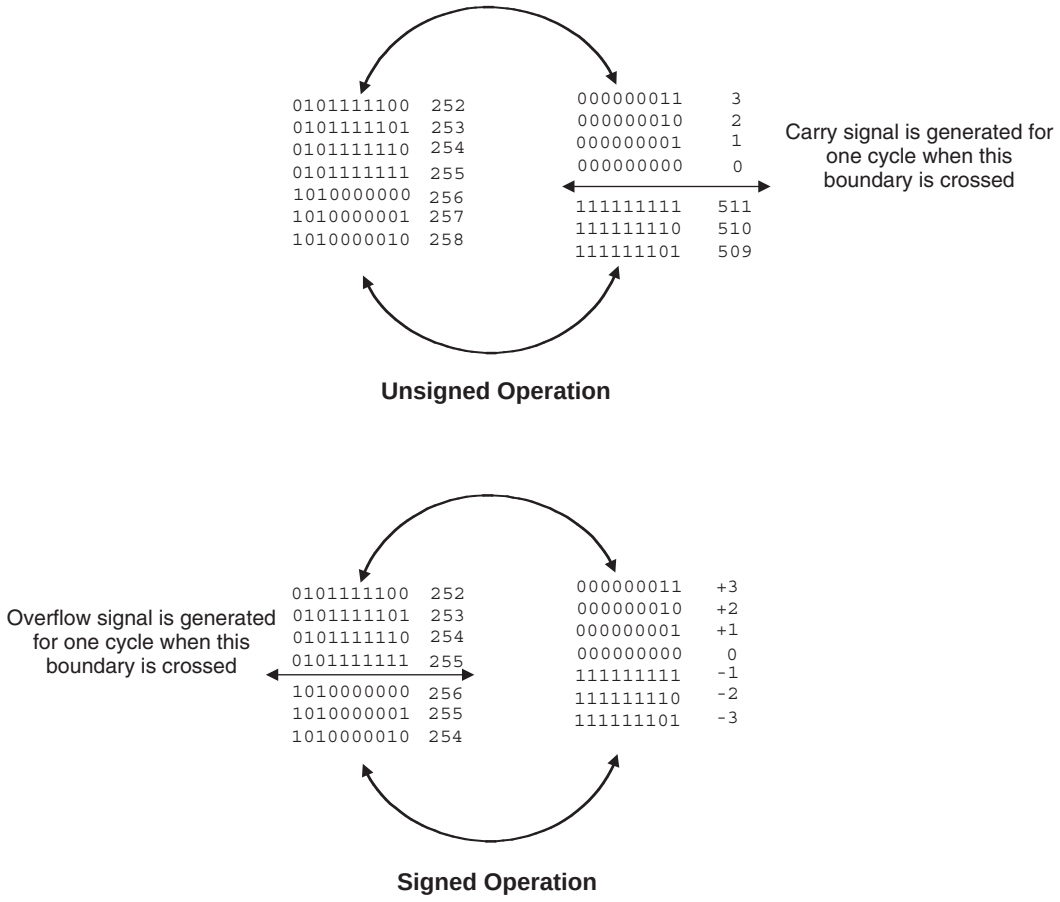
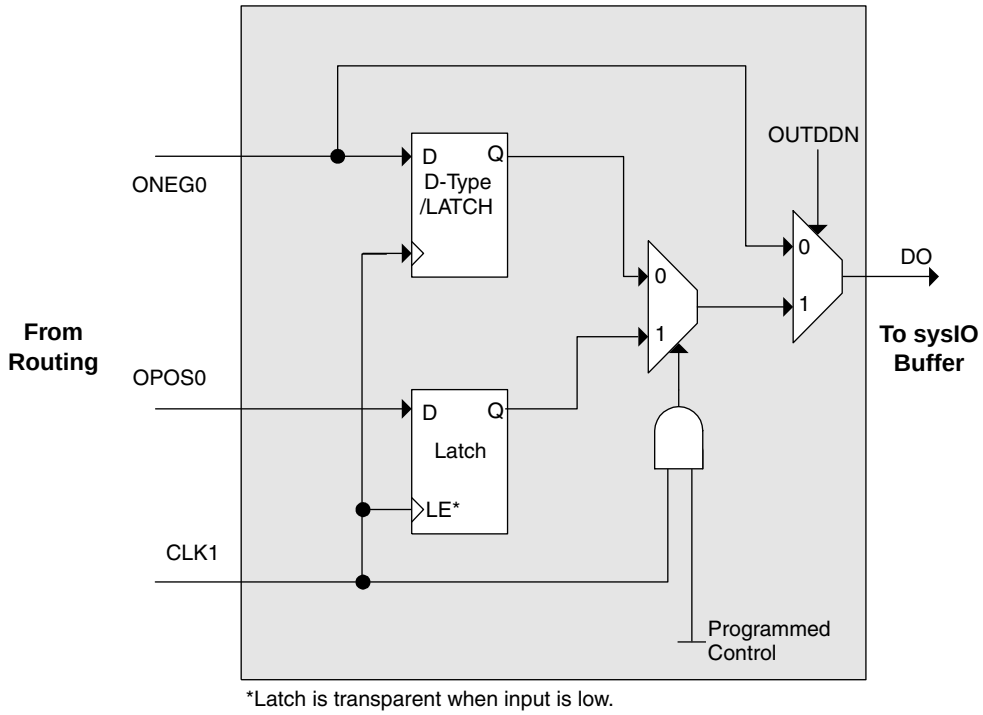
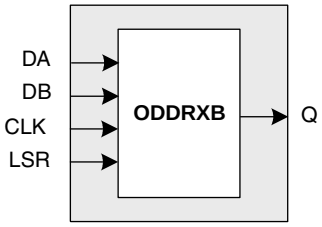


*Figure 2-29. Output Register Block*




*Latch is transparent when input is low.

*Figure 2-30. ODDRXB Primitive*




**Tristate Register Block**

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## LVDS25E

The top and bottom side of LatticeECP/EC devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in

Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

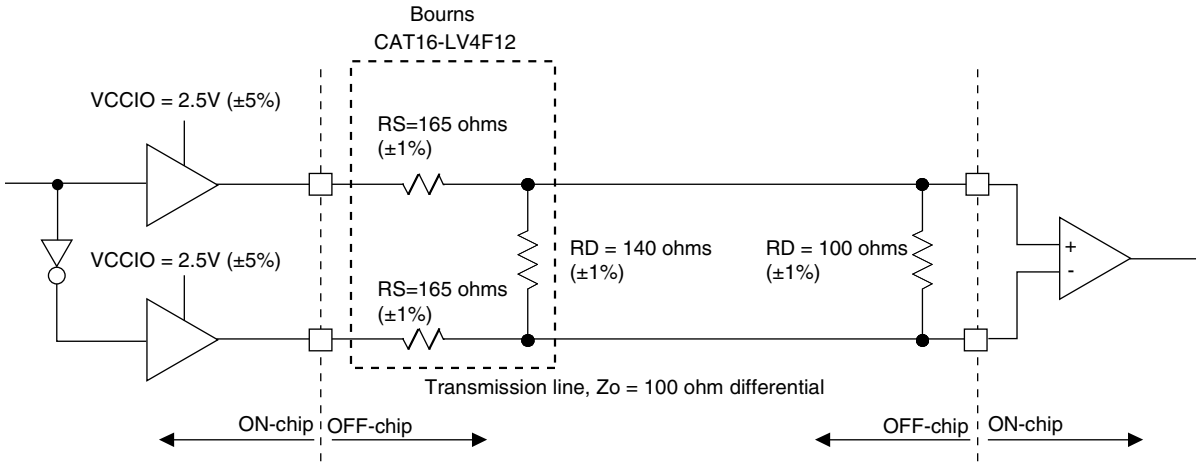



***Table 3-1. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.42 | V |
| $V_{OL}$ | Output low voltage | 1.08 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | ¾ |

## LVPECL

The LatticeECP/EC devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

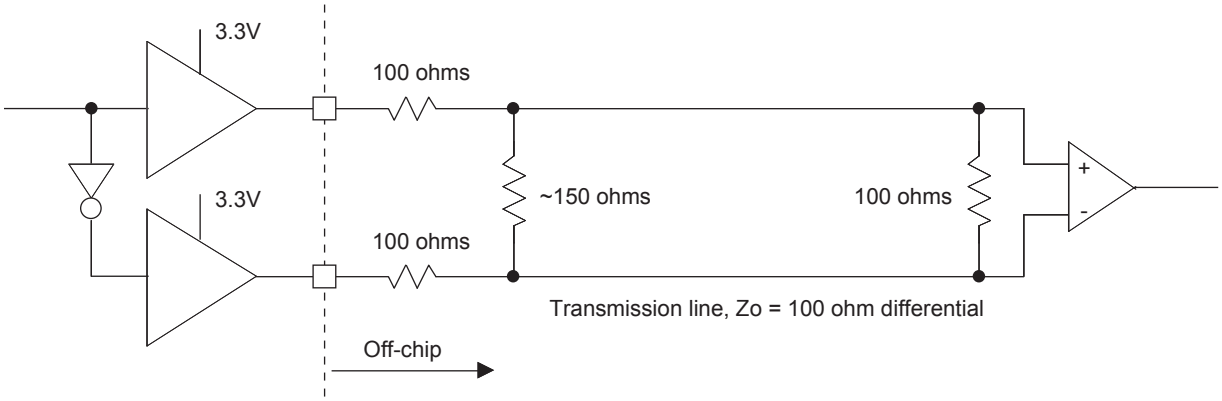



***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

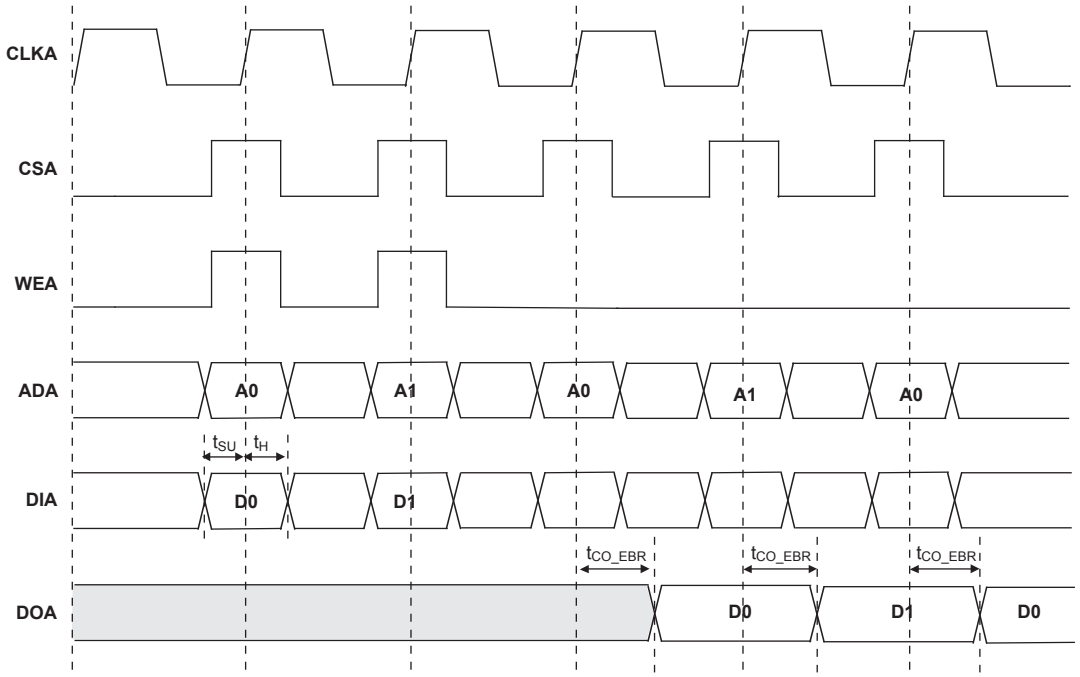
| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | ohm |
| $R_P$ | Driver parallel resistor | 150 | ohm |
| $R_T$ | Receiver termination | 100 | ohm |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | ohm |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

For further information about LVPECL, BLVDS and other differential interfaces please see the list of technical information at the end of this data sheet.

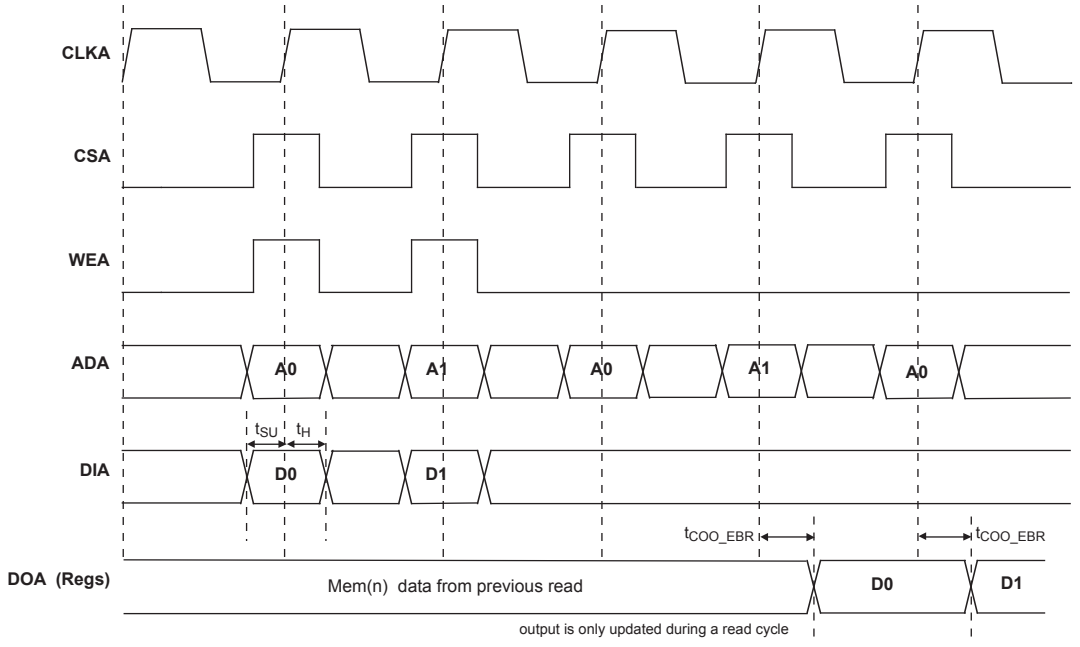
## EBR Memory Timing Diagrams

***Figure 3-8. Read/Write Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-9. Read/Write Mode with Input and Output Registers***



## LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 41 | PB11A | 4 | T | VREF1_4 | PB19A | 4 | T | VREF1_4 |
| 42 | PB11B | 4 | C | CSN | PB19B | 4 | C | CSN |
| 43 | PB12B | 4 | | D0/SPID7 | PB20B | 4 | | D0/SPID7 |
| 44 | PB13A | 4 | T | D2/SPID5 | PB21A | 4 | T | D2/SPID5 |
| 45 | PB13B | 4 | C | D1/SPID6 | PB21B | 4 | C | D1/SPID6 |
| 46 | PB14A | 4 | T | BDQS14 | PB22A | 4 | T | BDQS22 |
| 47 | PB14B | 4 | C | D3/SPID4 | PB22B | 4 | C | D3/SPID4 |
| 48 | PB15B | 4 | | D4/SPID3 | PB23B | 4 | | D4/SPID3 |
| 49 | PB16B | 4 | | D5/SPID2 | PB24B | 4 | | D5/SPID2 |
| 50 | PB17B | 4 | | D6/SPID1 | PB25B | 4 | | D6/SPID1 |
| 51* | GND3 GND4 | - | | | GND3 GND4 | - | | |
| 52 | PR10B | 3 | C | RLM0_PLLC_FB_A | PR14B | 3 | C | RLM0_PLLC_FB_A |
| 53 | PR10A | 3 | T | RLM0_PLLT_FB_A | PR14A | 3 | T | RLM0_PLLT_FB_A |
| 54 | PR9B | 3 | C | RLM0_PLLC_IN_A | PR13B | 3 | C | RLM0_PLLC_IN_A |
| 55 | PR9A | 3 | T | RLM0_PLLT_IN_A | PR13A | 3 | T | RLM0_PLLT_IN_A |
| 56 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 57 | PR8B | 3 | C | DI/CSSPIN | PR12B | 3 | C | DI/CSSPIN |
| 58 | PR8A | 3 | T | DOUT/CSON | PR12A | 3 | T | DOUT/CSON |
| 59 | PR7B | 3 | C | BUSY/SISPI | PR11B | 3 | C | BUSY/SISPI |
| 60 | PR7A | 3 | T | D7/SPID0 | PR11A | 3 | T | D7/SPID0 |
| 61 | CFG2 | 3 | | | CFG2 | 3 | | |
| 62 | CFG1 | 3 | | | CFG1 | 3 | | |
| 63 | CFG0 | 3 | | | CFG0 | 3 | | |
| 64 | VCC | - | | | VCC | - | | |
| 65 | PROGRAMN | 3 | | | PROGRAMN | 3 | | |
| 66 | CCLK | 3 | | | CCLK | 3 | | |
| 67 | INITN | 3 | | | INITN | 3 | | |
| 68 | GND | - | | | GND | - | | |
| 69 | DONE | 3 | | | DONE | 3 | | |
| 70 | PR5B | 2 | C | PCLKC2_0 | PR9B | 2 | C | PCLKC2_0 |
| 71 | PR5A | 2 | T | PCLKT2_0 | PR9A | 2 | T | PCLKT2_0 |
| 72 | PR2B | 2 | | VREF1_2 | PR2B | 2 | | VREF1_2 |
| 73 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 74 | GND2 | 2 | | | GND2 | 2 | | |
| 75 | PT17B | 1 | C | | PT25B | 1 | C | |
| 76 | PT17A | 1 | T | | PT25A | 1 | T | |
| 77 | PT14B | 1 | C | | PT22B | 1 | C | |
| 78 | PT14A | 1 | T | TDQS14 | PT22A | 1 | T | TDQS22 |
| 79 | PT13A | 1 | | | PT21A | 1 | | |
| 80 | PT12B | 1 | C | | PT20B | 1 | C | |
| 81 | PT12A | 1 | T | | PT20A | 1 | T | |

# LFEC1, LFEC3, LFECP/EC6 Logic Signal Connections: 144 TQFP

| Pin Number | LFEC1 | | | | LFEC3 | | | | LFECP6/EC6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 1 | VCCIO7 | 7 | | | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 2 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 |
| 3 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 |
| 4 | PL3A | 7 | T | | PL7A | 7 | T | | PL7A | 7 | T | |
| 5 | PL3B | 7 | C | | PL7B | 7 | C | | PL7B | 7 | C | |
| 6 | PL4A | 7 | T | | PL8A | 7 | T | | PL8A | 7 | T | |
| 7 | PL4B | 7 | C | | PL8B | 7 | C | | PL8B | 7 | C | |
| 8 | PL5A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 | PL9A | 7 | T | PCLKT7_0 |
| 9 | PL5B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 | PL9B | 7 | C | PCLKC7_0 |
| 10 | XRES | 6 | | | XRES | 6 | | | XRES | 6 | | |
| 11 | NC | - | | | NC | - | | | VCC | - | | |
| 12 | NC | - | | | NC | - | | | GND | - | | |
| 13 | VCC | - | | | VCC | - | | | VCC | - | | |
| 14 | TCK | 6 | | | TCK | 6 | | | TCK | 6 | | |
| 15 | GND | - | | | GND | - | | | GND | - | | |
| 16 | TDI | 6 | | | TDI | 6 | | | TDI | 6 | | |
| 17 | TMS | 6 | | | TMS | 6 | | | TMS | 6 | | |
| 18 | TDO | 6 | | | TDO | 6 | | | TDO | 6 | | |
| 19 | VCCJ | 6 | | | VCCJ | 6 | | | VCCJ | 6 | | |
| 20 | PL7A | 6 | T | LLM0_PLLT_IN_A | PL11A | 6 | T | LLM0_PLLT_IN_A | PL20A | 6 | T | LLM0_PLLT_IN_A |
| 21 | PL7B | 6 | C | LLM0_PLLC_IN_A | PL11B | 6 | C | LLM0_PLLC_IN_A | PL20B | 6 | C | LLM0_PLLC_IN_A |
| 22 | PL8A | 6 | T | LLM0_PLLT_FB_A | PL12A | 6 | T | LLM0_PLLT_FB_A | PL21A | 6 | T | LLM0_PLLT_FB_A |
| 23 | PL8B | 6 | C | LLM0_PLLC_FB_A | PL12B | 6 | C | LLM0_PLLC_FB_A | PL21B | 6 | C | LLM0_PLLC_FB_A |
| 24 | VCCIO6 | 6 | | | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 25 | PL9A | 6 | T | | PL13A | 6 | T | | PL22A | 6 | T | |
| 26 | PL9B | 6 | C | | PL13B | 6 | C | | PL22B | 6 | C | |
| 27 | PL10A | 6 | T | | PL14A | 6 | T | | PL23A | 6 | T | |
| 28 | GND6 | 6 | | | GND6 | 6 | | | GND6 | 6 | | |
| 29 | PL10B | 6 | C | | PL14B | 6 | C | | PL23B | 6 | C | |
| 30 | PL11A | 6 | T | LDQS11 | PL15A | 6 | T | LDQS15 | PL24A | 6 | T | LDQS24 |
| 31 | PL11B | 6 | C | | PL15B | 6 | C | | PL24B | 6 | C | |
| 32 | PL12A | 6 | T | | PL16A | 6 | T | | PL25A | 6 | T | |
| 33 | PL12B | 6 | C | | PL16B | 6 | C | | PL25B | 6 | C | |
| 34 | PL14A | 6 | T | VREF1_6 | PL18A | 6 | T | VREF1_6 | PL27A | 6 | T | VREF1_6 |
| 35 | PL14B | 6 | C | VREF2_6 | PL18B | 6 | C | VREF2_6 | PL27B | 6 | C | VREF2_6 |
| 36 | VCCIO6 | 6 | | | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 37* | GND5 GND6 | - | | | GND5 GND6 | - | | | GND5 GND6 | - | | |
| 38 | VCCIO5 | 5 | | | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 39 | PB2A | 5 | T | | PB10A | 5 | T | | PB10A | 5 | T | |
| 40 | PB2B | 5 | C | | PB10B | 5 | C | | PB10B | 5 | C | |
| 41 | PB3A | 5 | T | | PB11A | 5 | T | | PB11A | 5 | T | |
| 42 | PB3B | 5 | C | | PB11B | 5 | C | | PB11B | 5 | C | |
| 43 | PB5B | 5 | | | PB13B | 5 | | | PB13B | 5 | | |
| 44 | VCCIO5 | 5 | | | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 45 | PB6A | 5 | T | BDQS6 | PB14A | 5 | T | BDQS14 | PB14A | 5 | T | BDQS14 |
| 46 | PB6B | 5 | C | | PB14B | 5 | C | | PB14B | 5 | C | |
| 47 | PB7A | 5 | T | | PB15A | 5 | T | | PB15A | 5 | T | |
| 48 | PB7B | 5 | C | | PB15B | 5 | C | | PB15B | 5 | C | |
| 49 | PB8A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 |

## LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFEC1 | | | | LFEC3 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | LVDS | Dual Function | Pin Function | Bank | LVDS | Dual Function |
| 43 | PL11A | 6 | T | LDQS11 | PL15A | 6 | T | LDQS15 |
| 44 | PL11B | 6 | C | | PL15B | 6 | C | |
| 45 | PL12A | 6 | T | | PL16A | 6 | T | |
| 46 | PL12B | 6 | C | | PL16B | 6 | C | |
| 47 | PL13A | 6 | T | | PL17A | 6 | T | |
| 48 | PL13B | 6 | C | | PL17B | 6 | C | |
| 49 | PL14A | 6 | T | VREF1_6 | PL18A | 6 | T | VREF1_6 |
| 50 | PL14B | 6 | C | VREF2_6 | PL18B | 6 | C | VREF2_6 |
| 51 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 52* | GND5<br>GND6 | - | | | GND5<br>GND6 | - | | |
| 53 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 54 | NC | - | | | PB2A | 5 | T | |
| 55 | NC | - | | | PB2B | 5 | C | |
| 56 | NC | - | | | PB3A | 5 | T | |
| 57 | NC | - | | | PB3B | 5 | C | |
| 58 | NC | - | | | PB4A | 5 | T | |
| 59 | NC | - | | | PB4B | 5 | C | |
| 60 | NC | - | | | PB5A | 5 | T | |
| 61 | NC | - | | | PB5B | 5 | C | |
| 62 | NC | - | | | PB6A | 5 | T | BDQS6 |
| 63 | NC | - | | | PB6B | 5 | C | |
| 64 | NC | - | | | VCCIO5 | 5 | | |
| 65 | PB2A | 5 | T | | PB10A | 5 | T | |
| 66 | PB2B | 5 | C | | PB10B | 5 | C | |
| 67 | PB3A | 5 | T | | PB11A | 5 | T | |
| 68 | PB3B | 5 | C | | PB11B | 5 | C | |
| 69 | PB4A | 5 | T | | PB12A | 5 | T | |
| 70 | PB4B | 5 | C | | PB12B | 5 | C | |
| 71 | PB5A | 5 | T | | PB13A | 5 | T | |
| 72 | NC | - | | | GND5 | 5 | | |
| 73 | PB5B | 5 | C | | PB13B | 5 | C | |
| 74 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 75 | PB6A | 5 | T | BDQS6 | PB14A | 5 | T | BDQS14 |
| 76 | PB6B | 5 | C | | PB14B | 5 | C | |
| 77 | PB7A | 5 | T | | PB15A | 5 | T | |
| 78 | PB7B | 5 | C | | PB15B | 5 | C | |
| 79 | PB8A | 5 | T | VREF2_5 | PB16A | 5 | T | VREF2_5 |
| 80 | PB8B | 5 | C | VREF1_5 | PB16B | 5 | C | VREF1_5 |
| 81 | PB9A | 5 | T | PCLKT5_0 | PB17A | 5 | T | PCLKT5_0 |
| 82 | GND5 | 5 | | | GND5 | 5 | | |
| 83 | PB9B | 5 | C | PCLKC5_0 | PB17B | 5 | C | PCLKC5_0 |
| 84 | VCCAUX | - | | | VCCAUX | - | | |

## LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFEC3 | | | | LFECP6/LFEC6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | LVDS | Dual Function | Ball Function | Bank | LVDS | Dual Function |
| C16 | PR4B | 2 | C | | PR4B | 2 | C | |
| B16 | PR4A | 2 | T | | PR4A | 2 | T | |
| C15 | PR3B | 2 | C | | PR3B | 2 | C | |
| C14 | PR3A | 2 | T | | PR3A | 2 | T | |
| D14 | PR2B | 2 | C | VREF1_2 | PR2B | 2 | C | VREF1_2 |
| D13 | PR2A | 2 | T | VREF2_2 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | | GND2 | 2 | | |
| GND | GND1 | 1 | | | GND1 | 1 | | |
| - | - | - | | | GND1 | 1 | | |
| B13 | NC | - | | | PT26B | 1 | C | |
| C13 | NC | - | | | PT26A | 1 | T | |
| C12 | PT25B | 1 | C | | PT25B | 1 | C | |
| - | - | - | | | GND1 | 1 | | |
| D12 | PT25A | 1 | T | | PT25A | 1 | T | |
| A15 | PT24B | 1 | C | | PT24B | 1 | C | |
| B14 | PT24A | 1 | T | | PT24A | 1 | T | |
| D11 | PT23B | 1 | C | | PT23B | 1 | C | |
| C11 | PT23A | 1 | T | | PT23A | 1 | T | |
| E10 | PT22B | 1 | C | | PT22B | 1 | C | |
| E11 | PT22A | 1 | T | TDQS22 | PT22A | 1 | T | TDQS22 |
| A14 | PT21B | 1 | C | | PT21B | 1 | C | |
| GND | GND1 | 1 | | | GND1 | 1 | | |
| A13 | PT21A | 1 | T | | PT21A | 1 | T | |
| D10 | PT20B | 1 | C | | PT20B | 1 | C | |
| C10 | PT20A | 1 | T | | PT20A | 1 | T | |
| A12 | PT19B | 1 | C | VREF2_1 | PT19B | 1 | C | VREF2_1 |
| B12 | PT19A | 1 | T | VREF1_1 | PT19A | 1 | T | VREF1_1 |
| A11 | PT18B | 1 | C | | PT18B | 1 | C | |
| B11 | PT18A | 1 | T | | PT18A | 1 | T | |
| A10 | PT17B | 0 | C | PCLKC0_0 | PT17B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND0 | 0 | | |
| B10 | PT17A | 0 | T | PCLKT0_0 | PT17A | 0 | T | PCLKT0_0 |
| C9 | PT16B | 0 | C | VREF1_0 | PT16B | 0 | C | VREF1_0 |
| B9 | PT16A | 0 | T | VREF2_0 | PT16A | 0 | T | VREF2_0 |
| E9 | PT15B | 0 | C | | PT15B | 0 | C | |
| D9 | PT15A | 0 | T | | PT15A | 0 | T | |
| D8 | PT14B | 0 | C | | PT14B | 0 | C | |
| C8 | PT14A | 0 | T | TDQS14 | PT14A | 0 | T | TDQS14 |
| A9 | PT13B | 0 | C | | PT13B | 0 | C | |
| GND | GND0 | 0 | | | GND0 | 0 | | |
| A8 | PT13A | 0 | T | | PT13A | 0 | T | |
| B8 | PT12B | 0 | C | | PT12B | 0 | C | |
| B7 | PT12A | 0 | T | | PT12A | 0 | T | |

## LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA

| Ball Number | LFECP10/LFEC10 | | | | LFECP15/LFEC15 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | LVDS | Dual Function | Ball Function | Bank | LVDS | Dual Function |
| GND | GND7 | 7 | | | GND7 | 7 | | |
| D4 | PL2A | 7 | T | VREF2_7 | PL2A | 7 | T | VREF2_7 |
| D3 | PL2B | 7 | C | VREF1_7 | PL2B | 7 | C | VREF1_7 |
| GND | GND7 | 7 | | | GND7 | 7 | | |
| C3 | PL12A | 7 | T | | PL16A | 7 | T | |
| C2 | PL12B | 7 | C | | PL16B | 7 | C | |
| B1 | PL13A | 7 | T | | PL17A | 7 | T | |
| C1 | PL13B | 7 | C | | PL17B | 7 | C | |
| E3 | PL14A | 7 | T | | PL18A | 7 | T | |
| GND | GND7 | 7 | | | GND7 | 7 | | |
| - | - | - | | | GND7 | 7 | | |
| E4 | PL14B | 7 | C | | PL18B | 7 | C | |
| F4 | PL15A | 7 | T | LDQS15 | PL19A | 7 | T | LDQS19 |
| F5 | PL15B | 7 | C | | PL19B | 7 | C | |
| G4 | PL16A | 7 | T | | PL20A | 7 | T | |
| G3 | PL16B | 7 | C | | PL20B | 7 | C | |
| D2 | PL17A | 7 | T | | PL21A | 7 | T | |
| D1 | PL17B | 7 | C | | PL21B | 7 | C | |
| E1 | PL18A | 7 | T | PCLKT7_0 | PL22A | 7 | T | PCLKT7_0 |
| GND | GND7 | 7 | | | GND7 | 7 | | |
| E2 | PL18B | 7 | C | PCLKC7_0 | PL22B | 7 | C | PCLKC7_0 |
| F3 | XRES | 6 | | | XRES | 6 | | |
| G5 | PL20A | 6 | T | | PL24A | 6 | T | |
| H5 | PL20B | 6 | C | | PL24B | 6 | C | |
| F2 | PL21A | 6 | T | | PL25A | 6 | T | |
| F1 | PL21B | 6 | C | | PL25B | 6 | C | |
| H4 | PL22A | 6 | T | | PL26A | 6 | T | |
| H3 | PL22B | 6 | C | | PL26B | 6 | C | |
| G2 | PL23A | 6 | T | | PL27A | 6 | T | |
| GND | GND6 | 6 | | | GND6 | 6 | | |
| G1 | PL23B | 6 | C | | PL27B | 6 | C | |
| J4 | PL24A | 6 | T | LDQS24 | PL28A | 6 | T | LDQS28 |
| J3 | PL24B | 6 | C | | PL28B | 6 | C | |
| J5 | PL25A | 6 | T | | PL29A | 6 | T | |
| K5 | PL25B | 6 | C | | PL29B | 6 | C | |
| H2 | PL26A | 6 | T | | PL30A | 6 | T | |
| H1 | PL26B | 6 | C | | PL30B | 6 | C | |
| J2 | PL27A | 6 | T | | PL31A | 6 | T | |
| GND | GND6 | 6 | | | GND6 | 6 | | |
| J1 | PL27B | 6 | C | | PL31B | 6 | C | |
| K4 | TCK | 6 | | | TCK | 6 | | |
| K3 | TDI | 6 | | | TDI | 6 | | |

# LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

| LFECP20/LFEC20 | | | | | LFECP/LFEC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| C22 | PR9A | 2 | T | RUM0_PLLT_FB_A | C22 | PR17A | 2 | T | RUM0_PLLT_FB_A |
| G19 | PR8B | 2 | C | RUM0_PLLC_IN_A | G19 | PR16B | 2 | C | RUM0_PLLC_IN_A |
| G18 | PR8A | 2 | T | RUM0_PLLT_IN_A | G18 | PR16A | 2 | T | RUM0_PLLT_IN_A |
| F20 | PR7B | 2 | C | | F20 | PR15B | 2 | C | |
| F19 | PR7A | 2 | T | | F19 | PR15A | 2 | T | |
| E20 | PR6B | 2 | C | | E20 | PR14B | 2 | C | |
| D20 | PR6A | 2 | T | RDQS6 | D20 | PR14A | 2 | T | RDQS14 |
| C21 | PR5B | 2 | C | | C21 | PR13B | 2 | C | |
| GND | - | - | | | GND | GND2 | 2 | | |
| C20 | PR5A | 2 | T | | C20 | PR13A | 2 | T | |
| F18 | PR4B | 2 | C | | F18 | PR12B | 2 | C | |
| E18 | PR4A | 2 | T | | E18 | PR12A | 2 | T | |
| B22 | PR3B | 2 | C | | B22 | PR11B | 2 | C | |
| B21 | PR3A | 2 | T | | B21 | PR11A | 2 | T | |
| GND | - | - | | | GND | GND2 | 2 | | |
| E19 | PR2B | 2 | C | VREF1_2 | E19 | PR2B | 2 | C | VREF1_2 |
| D19 | PR2A | 2 | T | VREF2_2 | D19 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| GND | - | - | | | GND | GND1 | 1 | | |
| G17 | PT57B | 1 | C | | G17 | PT57B | 1 | C | |
| GND | - | - | | | GND | GND1 | 1 | | |
| F17 | PT57A | 1 | T | | F17 | PT57A | 1 | T | |
| D18 | PT56B | 1 | C | | D18 | PT56B | 1 | C | |
| C18 | PT56A | 1 | T | | C18 | PT56A | 1 | T | |
| C19 | PT55B | 1 | C | | C19 | PT55B | 1 | C | |
| B20 | PT55A | 1 | T | | B20 | PT55A | 1 | T | |
| D17 | PT54B | 1 | C | | D17 | PT54B | 1 | C | |
| C16 | PT54A | 1 | T | TDQS54 | C16 | PT54A | 1 | T | TDQS54 |
| B19 | PT53B | 1 | C | | B19 | PT53B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A20 | PT53A | 1 | T | | A20 | PT53A | 1 | T | |
| E17 | PT52B | 1 | C | | E17 | PT52B | 1 | C | |
| C17 | PT52A | 1 | T | | C17 | PT52A | 1 | T | |
| F16 | PT51B | 1 | C | | F16 | PT51B | 1 | C | |
| E16 | PT51A | 1 | T | | E16 | PT51A | 1 | T | |
| F15 | PT50B | 1 | C | | F15 | PT50B | 1 | C | |
| D16 | PT50A | 1 | T | | D16 | PT50A | 1 | T | |
| B18 | PT49B | 1 | C | | B18 | PT49B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A19 | PT49A | 1 | T | | A19 | PT49A | 1 | T | |
| B17 | PT48B | 1 | C | | B17 | PT48B | 1 | C | |
| A18 | PT48A | 1 | T | | A18 | PT48A | 1 | T | |
| B16 | PT47B | 1 | C | | B16 | PT47B | 1 | C | |

## LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

| LFEC20/LFECP20 | | | | | LFECP/EC33 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| Y6 | NC | - | | | Y6 | PL62A | 6 | T | |
| W7 | NC | - | | | W7 | PL62B | 6 | C | |
| AA4 | NC | - | | | AA4 | PL63A | 6 | T | |
| AB3 | NC | - | | | AB3 | PL63B | 6 | C | |
| AC2 | NC | - | | | AC2 | PL64A | 6 | T | |
| - | - | - | | | GND | GND6 | 6 | | |
| AC3 | NC | - | | | AC3 | PL64B | 6 | C | |
| AA5 | NC | - | | | AA5 | PL65A | 6 | T | LDQS65 |
| AB5 | NC | - | | | AB5 | PL65B | 6 | C | |
| AD3 | NC | - | | | AD3 | PL66A | 6 | T | |
| AD2 | NC | - | | | AD2 | PL66B | 6 | C | |
| AE1 | NC | - | | | AE1 | PL67A | 6 | T | |
| AD1 | NC | - | | | AD1 | PL67B | 6 | C | |
| AB4 | PL48A | 6 | T | VREF1_6 | AB4 | PL68A | 6 | T | VREF1_6 |
| AC4 | PL48B | 6 | C | VREF2_6 | AC4 | PL68B | 6 | C | VREF2_6 |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB6 | PB2A | 5 | T | | AB6 | PB2A | 5 | T | |
| AA6 | PB2B | 5 | C | | AA6 | PB2B | 5 | C | |
| AC7 | PB3A | 5 | T | | AC7 | PB3A | 5 | T | |
| Y8 | PB3B | 5 | C | | Y8 | PB3B | 5 | C | |
| AB7 | PB4A | 5 | T | | AB7 | PB4A | 5 | T | |
| AA7 | PB4B | 5 | C | | AA7 | PB4B | 5 | C | |
| AC6 | PB5A | 5 | T | | AC6 | PB5A | 5 | T | |
| AC5 | PB5B | 5 | C | | AC5 | PB5B | 5 | C | |
| AB8 | PB6A | 5 | T | BDQS6 | AB8 | PB6A | 5 | T | BDQS6 |
| AC8 | PB6B | 5 | C | | AC8 | PB6B | 5 | C | |
| AE2 | PB7A | 5 | T | | AE2 | PB7A | 5 | T | |
| AA8 | PB7B | 5 | C | | AA8 | PB7B | 5 | C | |
| AF2 | PB8A | 5 | T | | AF2 | PB8A | 5 | T | |
| Y9 | PB8B | 5 | C | | Y9 | PB8B | 5 | C | |
| AD5 | PB9A | 5 | T | | AD5 | PB9A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AD4 | PB9B | 5 | C | | AD4 | PB9B | 5 | C | |
| AD8 | PB10A | 5 | T | | AD8 | PB10A | 5 | T | |
| AC9 | PB10B | 5 | C | | AC9 | PB10B | 5 | C | |
| AE3 | PB11A | 5 | T | | AE3 | PB11A | 5 | T | |
| AB9 | PB11B | 5 | C | | AB9 | PB11B | 5 | C | |
| AF3 | PB12A | 5 | T | | AF3 | PB12A | 5 | T | |
| AD9 | PB12B | 5 | C | | AD9 | PB12B | 5 | C | |
| AE4 | PB13A | 5 | T | | AE4 | PB13A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

**LatticeECP Industrial (Continued)**

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP20E-3F672I | 400 | -3 | fpBGA | 672 | IND | 19.7K |
| LFECP20E-4F672I | 400 | -4 | fpBGA | 672 | IND | 19.7K |
| LFECP20E-3F484I | 360 | -3 | fpBGA | 484 | IND | 19.7K |
| LFECP20E-4F484I | 360 | -4 | fpBGA | 484 | IND | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3F672I | 496 | -3 | fpBGA | 672 | IND | 32.8K |
| LFECP33E-4F672I | 496 | -4 | fpBGA | 672 | IND | 32.8K |
| LFECP33E-3F484I | 360 | -3 | fpBGA | 484 | IND | 32.8K |
| LFECP33E-4F484I | 360 | -4 | fpBGA | 484 | IND | 32.8K |

**LatticeEC Commercial (Continued)**

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC10E-4FN256C | 195 | -4 | Lead-Free fpBGA | 256 | COM | 10.2K |
| LFEC10E-5FN256C | 195 | -5 | Lead-Free fpBGA | 256 | COM | 10.2K |
| LFEC10E-3QN208C | 147 | -3 | Lead-Free PQFP | 208 | COM | 10.2K |
| LFEC10E-4QN208C | 147 | -4 | Lead-Free PQFP | 208 | COM | 10.2K |
| LFEC10E-5QN208C | 147 | -5 | Lead-Free PQFP | 208 | COM | 10.2K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC15E-3FN484C | 352 | -3 | Lead-Free fpBGA | 484 | COM | 15.3K |
| LFEC15E-4FN484C | 352 | -4 | Lead-Free fpBGA | 484 | COM | 15.3K |
| LFEC15E-5FN484C | 352 | -5 | Lead-Free fpBGA | 484 | COM | 15.3K |
| LFEC15E-3FN256C | 195 | -3 | Lead-Free fpBGA | 256 | COM | 15.3K |
| LFEC15E-4FN256C | 195 | -4 | Lead-Free fpBGA | 256 | COM | 15.3K |
| LFEC15E-5FN256C | 195 | -5 | Lead-Free fpBGA | 256 | COM | 15.3K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC20E-3FN672C | 400 | -3 | Lead-Free fpBGA | 672 | COM | 19.7K |
| LFEC20E-4FN672C | 400 | -4 | Lead-Free fpBGA | 672 | COM | 19.7K |
| LFEC20E-5FN672C | 400 | -5 | Lead-Free fpBGA | 672 | COM | 19.7K |
| LFEC20E-3FN484C | 360 | -3 | Lead-Free fpBGA | 484 | COM | 19.7K |
| LFEC20E-4FN484C | 360 | -4 | Lead-Free fpBGA | 484 | COM | 19.7K |
| LFEC20E-5FN484C | 360 | -5 | Lead-Free fpBGA | 484 | COM | 19.7K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC33E-3FN672C | 496 | -3 | Lead-Free fpBGA | 672 | COM | 32.8K |
| LFEC33E-4FN672C | 496 | -4 | Lead-Free fpBGA | 672 | COM | 32.8K |
| LFEC33E-5FN672C | 496 | -5 | Lead-Free fpBGA | 672 | COM | 32.8K |
| LFEC33E-3FN484C | 360 | -3 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFEC33E-4FN484C | 360 | -4 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFEC33E-5FN484C | 360 | -5 | Lead-Free fpBGA | 484 | COM | 32.8K |

### LatticeECP Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFECP33E-3FN484C | 360 | -3 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFECP33E-4FN484C | 360 | -4 | Lead-Free fpBGA | 484 | COM | 32.8K |
| LFECP33E-5FN484C | 360 | -5 | Lead-Free fpBGA | 484 | COM | 32.8K |

### LatticeEC Industrial

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC1E-3QN208I | 112 | -3 | Lead-Free PQFP | 208 | IND | 1.5K |
| LFEC1E-4QN208I | 112 | -4 | Lead-Free PQFP | 208 | IND | 1.5K |
| LFEC1E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 1.5K |
| LFEC1E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 1.5K |
| LFEC1E-3TN100I | 67 | -3 | Lead-Free TQFP | 100 | IND | 1.5K |
| LFEC1E-4TN100I | 67 | -4 | Lead-Free TQFP | 100 | IND | 1.5K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC3E-3FN256I | 160 | -3 | Lead-Free fpBGA | 256 | IND | 3.1K |
| LFEC3E-4FN256I | 160 | -4 | Lead-Free fpBGA | 256 | IND | 3.1K |
| LFEC3E-3QN208I | 145 | -3 | Lead-Free PQFP | 208 | IND | 3.1K |
| LFEC3E-4QN208I | 145 | -4 | Lead-Free PQFP | 208 | IND | 3.1K |
| LFEC3E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 3.1K |
| LFEC3E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 3.1K |
| LFEC3E-3TN100I | 67 | -3 | Lead-Free TQFP | 100 | IND | 3.1K |
| LFEC3E-4TN100I | 67 | -4 | Lead-Free TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC6E-3FN484I | 224 | -3 | Lead-Free fpBGA | 484 | IND | 6.1K |
| LFEC6E-4FN484I | 224 | -4 | Lead-Free fpBGA | 484 | IND | 6.1K |
| LFEC6E-3FN256I | 195 | -3 | Lead-Free fpBGA | 256 | IND | 6.1K |
| LFEC6E-4FN256I | 195 | -4 | Lead-Free fpBGA | 256 | IND | 6.1K |
| LFEC6E-3QN208I | 147 | -3 | Lead-Free PQFP | 208 | IND | 6.1K |
| LFEC6E-4QN208I | 147 | -4 | Lead-Free PQFP | 208 | IND | 6.1K |
| LFEC6E-3TN144I | 97 | -3 | Lead-Free TQFP | 144 | IND | 6.1K |
| LFEC6E-4TN144I | 97 | -4 | Lead-Free TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins/Balls | Temp. | LUTs |
|---|---|---|---|---|---|---|
| LFEC10E-3FN484I | 288 | -3 | Lead-Free fpBGA | 484 | IND | 10.2K |
| LFEC10E-4FN484I | 288 | -4 | Lead-Free fpBGA | 484 | IND | 10.2K |
| LFEC10E-3FN256I | 195 | -3 | Lead-Free fpBGA | 256 | IND | 10.2K |
| LFEC10E-4FN256I | 195 | -4 | Lead-Free fpBGA | 256 | IND | 10.2K |
| LFEC10E-3QN208I | 147 | -3 | Lead-Free PQFP | 208 | IND | 10.2K |
| LFEC10E-4QN208I | 147 | -4 | Lead-Free PQFP | 208 | IND | 10.2K |