Lattice Semiconductor Corporation - LFECP6E-5FN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

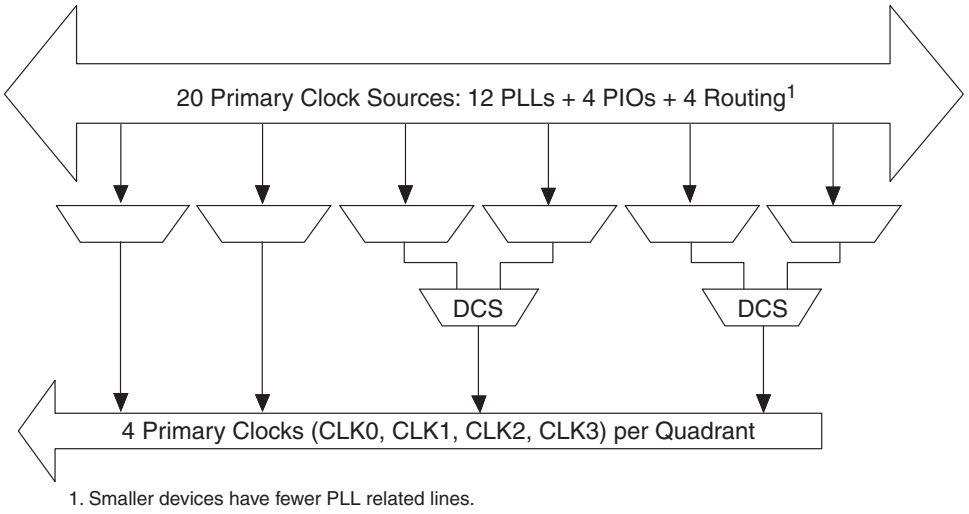
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6100
Total RAM Bits	94208
Number of I/O	224
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfecp6e-5fn484c

Figure 2-8. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-9. Per Quadrant Secondary Clock Selection

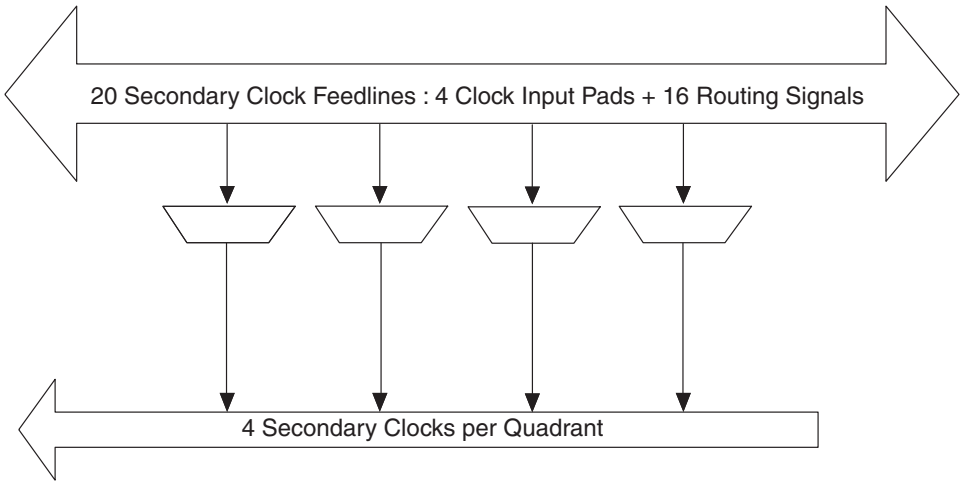
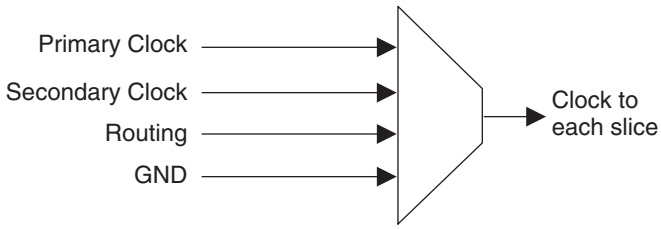


Figure 2-10. Slice Clock Selection

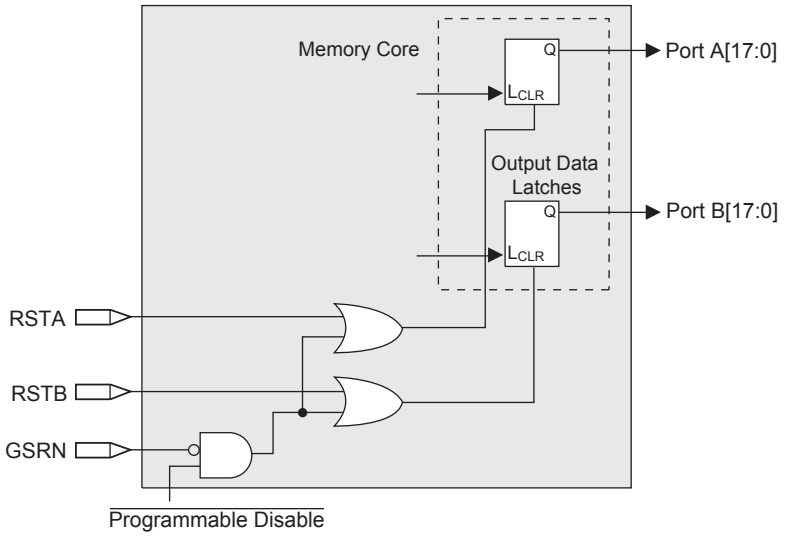


sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

Figure 2-16. Memory Core Reset

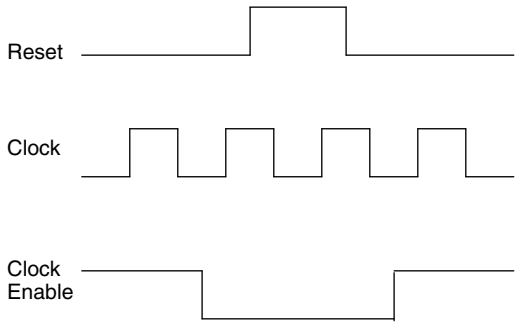


For further information about sysMEM EBR block, please see the the list of technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-17. The GSR input to the EBR is always asynchronous.

Figure 2-17. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP Block

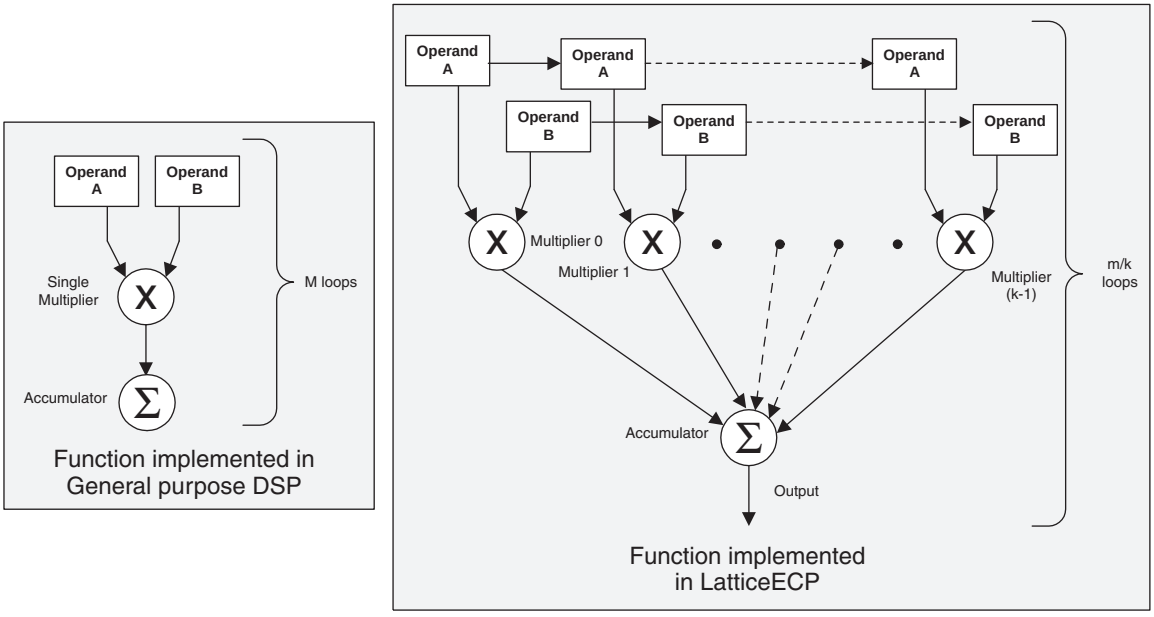
The LatticeECP-DSP family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and

decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-18 compares the serial and the parallel implementations.

Figure 2-18. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

IPexpress™

The user can access the sysDSP block via the IPexpress configuration tool, included with the ispLEVER design tool suite. IPexpress has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
LFECP6	4	32	16	4
LFECP10	5	40	20	5
LFECP15	6	48	24	6
LFECP20	7	56	28	7
LFECP33	8	64	32	8

Table 2-10. Embedded SRAM in LatticeECP Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LFECP6	10	92
LFECP10	30	276
LFECP15	38	350
LFECP20	46	424
LFECP33	54	498

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

Table 2-11. DSP Block Performance of LatticeECP Family

Device	DSP Block	DSP Performance MMAC
LFECP6	4	3680
LFECP10	5	4600
LFECP15	6	5520
LFECP20	7	6440
LFECP33	8	7360

Figure 2-27. Input Register DDR Waveforms

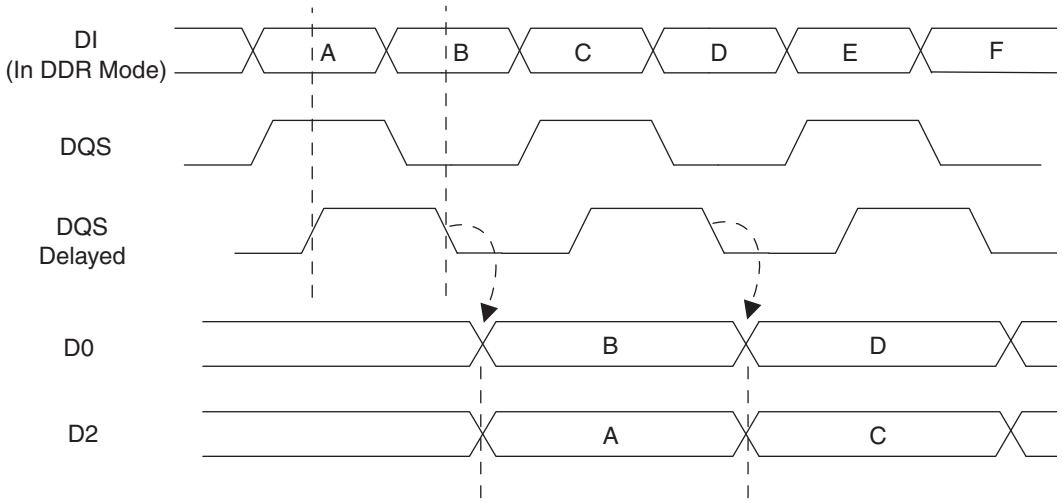
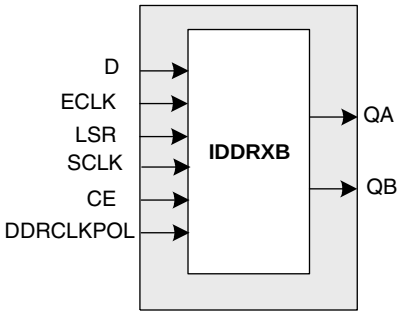


Figure 2-28. INDDRXB Primitive



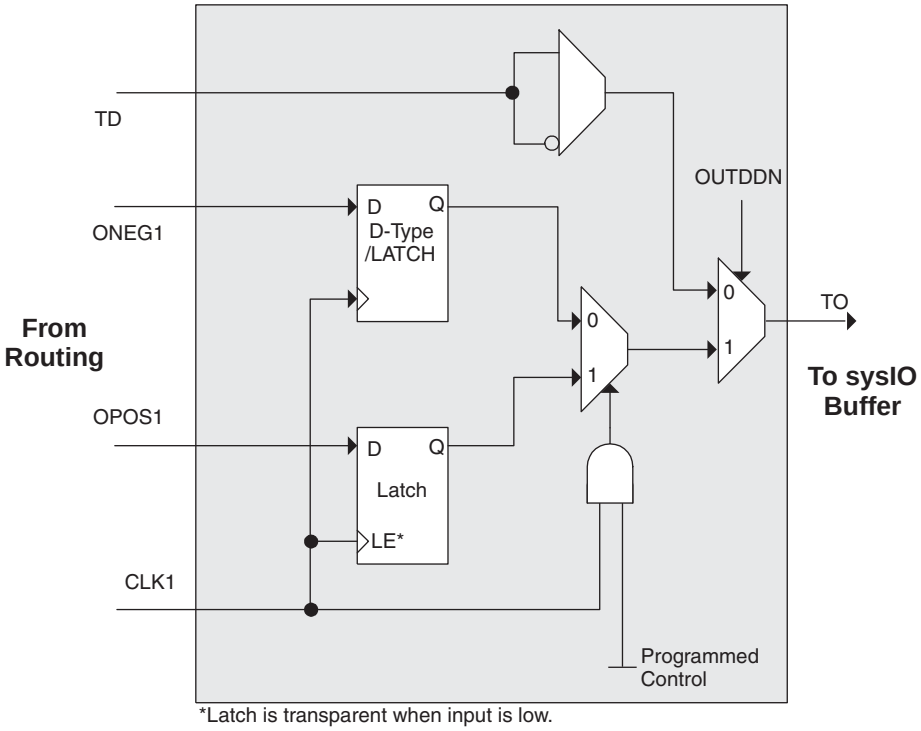
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-31. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP/EC devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeECP/EC sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL, BLVDS, RSDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

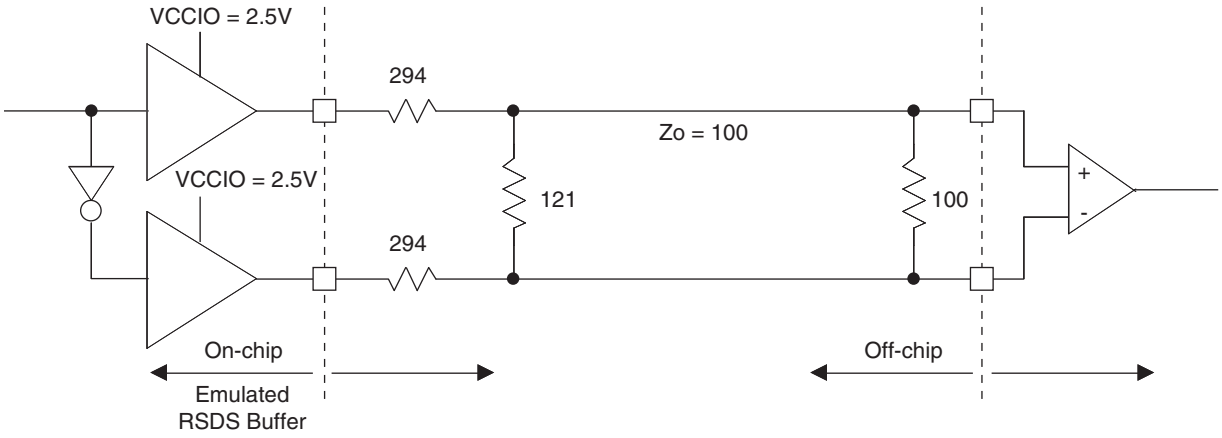


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohm
R_S	Driver series resistor	294	ohm
R_P	Driver parallel resistor	121	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohm
I_{DC}	DC output current	3.66	mA

LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

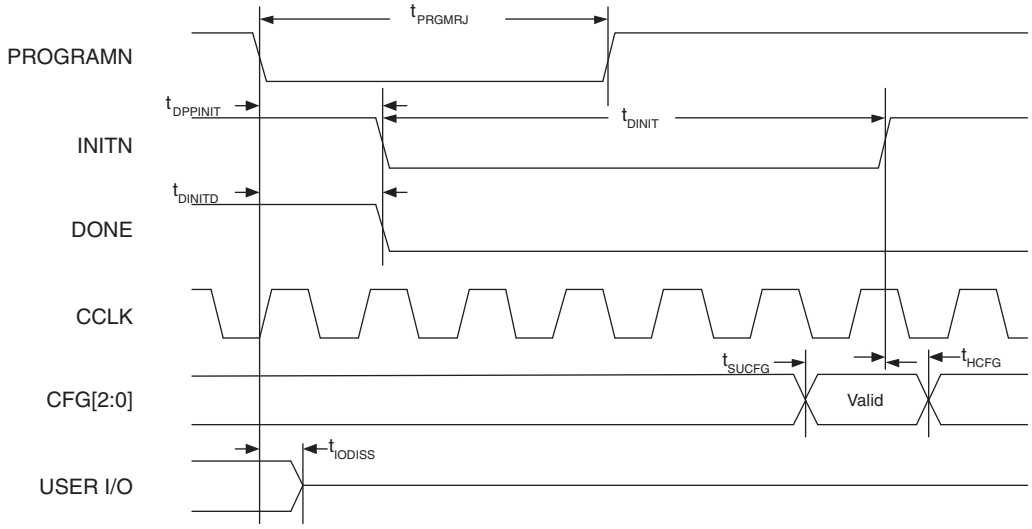
Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

Figure 3-17. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-18. Wake-Up Timing

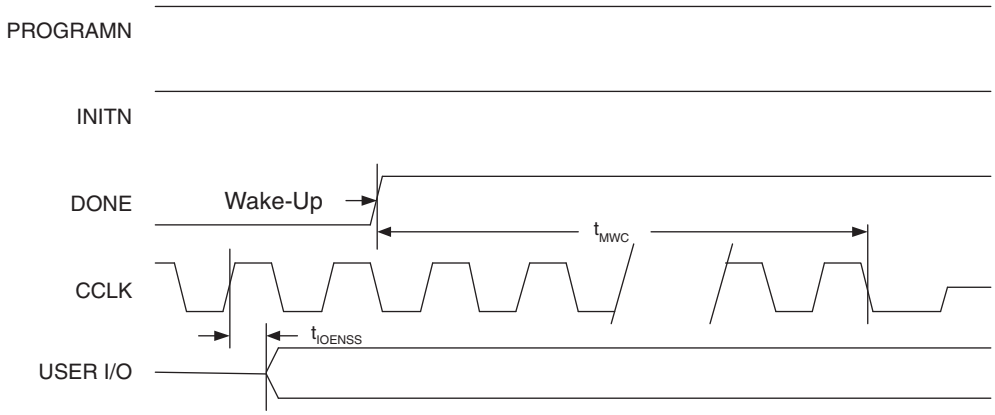
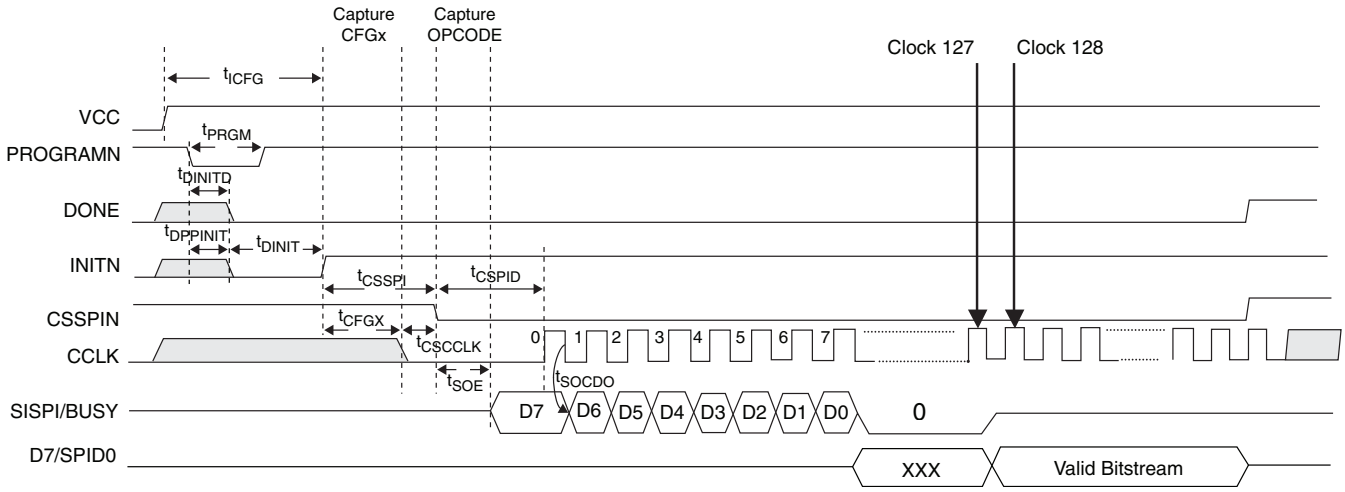


Figure 3-19. sysCONFIG SPI Port Sequence



LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
41	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4
42	PB11B	4	C	CSN	PB19B	4	C	CSN
43	PB12B	4		D0/SPID7	PB20B	4		D0/SPID7
44	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
45	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
46	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22
47	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
48	PB15B	4		D4/SPID3	PB23B	4		D4/SPID3
49	PB16B	4		D5/SPID2	PB24B	4		D5/SPID2
50	PB17B	4		D6/SPID1	PB25B	4		D6/SPID1
51*	GND3 GND4	-			GND3 GND4	-		
52	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A
53	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A
54	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A
55	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A
56	VCCIO3	3			VCCIO3	3		
57	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN
58	PR8A	3	T	DOUT/CSON	PR12A	3	T	DOUT/CSON
59	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI
60	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0
61	CFG2	3			CFG2	3		
62	CFG1	3			CFG1	3		
63	CFG0	3			CFG0	3		
64	VCC	-			VCC	-		
65	PROGRAMN	3			PROGRAMN	3		
66	CCLK	3			CCLK	3		
67	INITN	3			INITN	3		
68	GND	-			GND	-		
69	DONE	3			DONE	3		
70	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
71	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
72	PR2B	2		VREF1_2	PR2B	2		VREF1_2
73	VCCIO2	2			VCCIO2	2		
74	GND2	2			GND2	2		
75	PT17B	1	C		PT25B	1	C	
76	PT17A	1	T		PT25A	1	T	
77	PT14B	1	C		PT22B	1	C	
78	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
79	PT13A	1			PT21A	1		
80	PT12B	1	C		PT20B	1	C	
81	PT12A	1	T		PT20A	1	T	

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
82	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
83	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
84	PT10B	1	C		PT18B	1	C	
85	PT10A	1	T		PT18A	1	T	
86	VCCIO1	1			VCCIO1	1		
87	VCCAUX	-			VCCAUX	-		
88	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
89	GND0	0			GND0	0		
90	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
91	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
92	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
93	PT7B	0			PT15B	0		
94	PT6B	0	C		PT14B	0	C	
95	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
96	PT4B	0	C		PT12B	0	C	
97	PT4A	0	T		PT12A	0	T	
98	PT2B	0	C		PT10B	0	C	
99	PT2A	0	T		PT10A	0	T	
100	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
G12	PR18A	2	T	PCLKT2_0	PR22A	2	T	PCLKT2_0
G13	PR17B	2	C		PR21B	2	C	
F13	PR17A	2	T		PR21A	2	T	
F12	PR16B	2	C		PR20B	2	C	
E13	PR16A	2	T		PR20A	2	T	
D16	PR15B	2	C		PR19B	2	C	
D15	PR15A	2	T		PR19A	2	T	RDQS19
F14	PR14B	2	C		PR18B	2	C	
GND	GND2	2			GND2	2		
E14	PR14A	2	T		PR18A	2	T	
C16	PR13B	2	C		PR17B	2	C	
B16	PR13A	2	T		PR17A	2	T	
C15	PR12B	2	C		PR16B	2	C	
C14	PR12A	2	T		PR16A	2	T	
GND	GND2	2			GND2	2		
-	-	-			GND2	2		
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
-	-	-			GND1	1		
B13	PT34B	1	C		PT34B	1	C	
C13	PT34A	1	T		PT34A	1	T	
C12	PT33B	1	C		PT33B	1	C	
GND	GND1	1			GND1	1		
D12	PT33A	1	T		PT33A	1	T	
A15	PT32B	1	C		PT32B	1	C	
B14	PT32A	1	T		PT32A	1	T	
D11	PT31B	1	C		PT31B	1	C	
C11	PT31A	1	T		PT31A	1	T	
E10	PT30B	1	C		PT30B	1	C	
E11	PT30A	1	T	TDQS30	PT30A	1	T	TDQS30
A14	PT29B	1	C		PT29B	1	C	
GND	GND1	1			GND1	1		
A13	PT29A	1	T		PT29A	1	T	
D10	PT28B	1	C		PT28B	1	C	
C10	PT28A	1	T		PT28A	1	T	
A12	PT27B	1	C	VREF2_1	PT27B	1	C	VREF2_1
B12	PT27A	1	T	VREF1_1	PT27A	1	T	VREF1_1
A11	PT26B	1	C		PT26B	1	C	
B11	PT26A	1	T		PT26A	1	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR17A	2	T	RUM0_PLLT_FB_A
G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR16B	2	C	RUM0_PLLC_IN_A
G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR16A	2	T	RUM0_PLLT_IN_A
F20	PR7B	2	C		F20	PR15B	2	C	
F19	PR7A	2	T		F19	PR15A	2	T	
E20	PR6B	2	C		E20	PR14B	2	C	
D20	PR6A	2	T	RDQS6	D20	PR14A	2	T	RDQS14
C21	PR5B	2	C		C21	PR13B	2	C	
GND	-	-			GND	GND2	2		
C20	PR5A	2	T		C20	PR13A	2	T	
F18	PR4B	2	C		F18	PR12B	2	C	
E18	PR4A	2	T		E18	PR12A	2	T	
B22	PR3B	2	C		B22	PR11B	2	C	
B21	PR3A	2	T		B21	PR11A	2	T	
GND	-	-			GND	GND2	2		
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
GND	-	-			GND	GND1	1		
G17	PT57B	1	C		G17	PT57B	1	C	
GND	-	-			GND	GND1	1		
F17	PT57A	1	T		F17	PT57A	1	T	
D18	PT56B	1	C		D18	PT56B	1	C	
C18	PT56A	1	T		C18	PT56A	1	T	
C19	PT55B	1	C		C19	PT55B	1	C	
B20	PT55A	1	T		B20	PT55A	1	T	
D17	PT54B	1	C		D17	PT54B	1	C	
C16	PT54A	1	T	TDQS54	C16	PT54A	1	T	TDQS54
B19	PT53B	1	C		B19	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
A20	PT53A	1	T		A20	PT53A	1	T	
E17	PT52B	1	C		E17	PT52B	1	C	
C17	PT52A	1	T		C17	PT52A	1	T	
F16	PT51B	1	C		F16	PT51B	1	C	
E16	PT51A	1	T		E16	PT51A	1	T	
F15	PT50B	1	C		F15	PT50B	1	C	
D16	PT50A	1	T		D16	PT50A	1	T	
B18	PT49B	1	C		B18	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
A19	PT49A	1	T		A19	PT49A	1	T	
B17	PT48B	1	C		B17	PT48B	1	C	
A18	PT48A	1	T		A18	PT48A	1	T	
B16	PT47B	1	C		B16	PT47B	1	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A21	PT51A	1	T		A21	PT51A	1	T	
E17	PT50B	1	C		E17	PT50B	1	C	
B17	PT50A	1	T		B17	PT50A	1	T	
C17	PT49B	1	C		C17	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
D17	PT49A	1	T		D17	PT49A	1	T	
F17	PT48B	1	C		F17	PT48B	1	C	
E20	PT48A	1	T		E20	PT48A	1	T	
G17	PT47B	1	C		G17	PT47B	1	C	
B20	PT47A	1	T		B20	PT47A	1	T	
E16	PT46B	1	C		E16	PT46B	1	C	
A20	PT46A	1	T	TDQS46	A20	PT46A	1	T	TDQS46
A19	PT45B	1	C		A19	PT45B	1	C	
GND	GND1	1			GND	GND1	1		
B19	PT45A	1	T		B19	PT45A	1	T	
D16	PT44B	1	C		D16	PT44B	1	C	
C16	PT44A	1	T		C16	PT44A	1	T	
F16	PT43B	1	C		F16	PT43B	1	C	
A18	PT43A	1	T		A18	PT43A	1	T	
G16	PT42B	1	C		G16	PT42B	1	C	
B18	PT42A	1	T		B18	PT42A	1	T	
A17	PT41B	1	C		A17	PT41B	1	C	
GND	GND1	1			GND	GND1	1		
A16	PT41A	1	T		A16	PT41A	1	T	
D15	PT40B	1	C		D15	PT40B	1	C	
B16	PT40A	1	T		B16	PT40A	1	T	
E15	PT39B	1	C		E15	PT39B	1	C	
C15	PT39A	1	T		C15	PT39A	1	T	
F15	PT38B	1	C		F15	PT38B	1	C	
G15	PT38A	1	T	TDQS38	G15	PT38A	1	T	TDQS38
B15	PT37B	1	C		B15	PT37B	1	C	
GND	GND1	1			GND	GND1	1		
A15	PT37A	1	T		A15	PT37A	1	T	
E14	PT36B	1	C		E14	PT36B	1	C	
G14	PT36A	1	T		G14	PT36A	1	T	
D14	PT35B	1	C	VREF2_1	D14	PT35B	1	C	VREF2_1
E13	PT35A	1	T	VREF1_1	E13	PT35A	1	T	VREF1_1
F14	PT34B	1	C		F14	PT34B	1	C	
C14	PT34A	1	T		C14	PT34A	1	T	
B14	PT33B	0	C	PCLKC0_0	B14	PT33B	0	C	PCLKC0_0
GND	GND0	0			GND	GND0	0		
A14	PT33A	0	T	PCLKT0_0	A14	PT33A	0	T	PCLKT0_0

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

LatticeECP/EC Family Data Sheet Ordering Information

Part Number Description

LFXXX XX X – X XXXX X

Device Family
- Lattice EC (FPGA)
- Lattice ECP (EC FPGA + DSP Blocks)

Logic Capacity
- 1* = 1.5K LUTs
- 3* = 3K LUTs
- 6 = 6K LUTs
- 10 = 10K LUTs
- 15 = 15K LUTs
- 20 = 20K LUTs
- 33 = 33K LUTs

Supply Voltage
- E = 1.2V

Grade
- C = Commercial
- I = Industrial

Package
- T100 = 100-pin TQFP*
- T144 = 144-pin TQFP
- Q208 = 208-pin PQFP
- F256 = 256-ball fpBGA
- F484 = 484-ball fpBGA
- F672 = 672-ball fpBGA
- TN100 = 100-pin Lead-free TQFP*
- TN144 = 144-pin Lead-free TQFP
- QN208 = 208-pin Lead-free PQFP
- FN256 = 256-ball Lead-free fpBGA
- FN484 = 484-ball Lead-free fpBGA
- FN672 = 672-ball Lead-free fpBGA

Speed
- 3 = Slowest
- 4
- 5 = Fastest

*Not available in the LatticeECP Family.

Ordering Information

Note:þLatticeECP/EC devices are dual marked. For example, the commercial speed grade LFEC20E-4F484C is also marked with industrial grade -3I (LFEC20E-3F484I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC1E-3QN208I	112	-3	Lead-Free PQFP	208	IND	1.5K
LFEC1E-4QN208I	112	-4	Lead-Free PQFP	208	IND	1.5K
LFEC1E-3TN144I	97	-3	Lead-Free TQFP	144	IND	1.5K
LFEC1E-4TN144I	97	-4	Lead-Free TQFP	144	IND	1.5K
LFEC1E-3TN100I	67	-3	Lead-Free TQFP	100	IND	1.5K
LFEC1E-4TN100I	67	-4	Lead-Free TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC3E-3FN256I	160	-3	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-4FN256I	160	-4	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-3QN208I	145	-3	Lead-Free PQFP	208	IND	3.1K
LFEC3E-4QN208I	145	-4	Lead-Free PQFP	208	IND	3.1K
LFEC3E-3TN144I	97	-3	Lead-Free TQFP	144	IND	3.1K
LFEC3E-4TN144I	97	-4	Lead-Free TQFP	144	IND	3.1K
LFEC3E-3TN100I	67	-3	Lead-Free TQFP	100	IND	3.1K
LFEC3E-4TN100I	67	-4	Lead-Free TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K