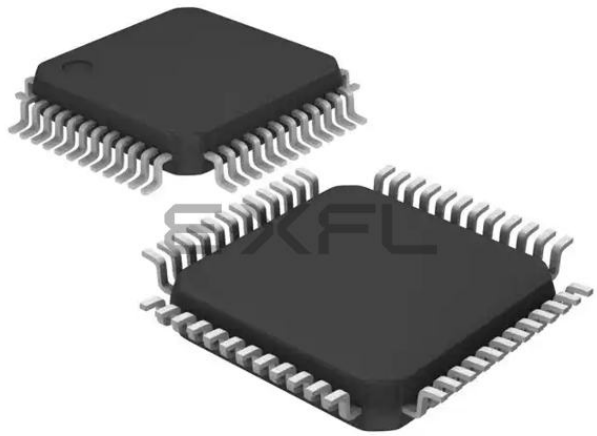

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8246mlfr

1 MC56F825x/MC56F824x Family Configuration

Table 1 compares the MC56F825x/MC56F824x devices.

Table 1. MC56F825x/MC56F824x Device Comparison

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Operation Frequency (MHz)		60					
High Speed Peripheral Clock (MHz)		120					
Flash memory size (KB) with 1024 words per page		48	48	48	64	64	64
RAM size (KB)		6	6	8	8	8	8
Enhanced Flex PWM (eFlexPWM)	High resolution NanoEdge PWM (520 ps res.)	6	6	6	6	6	6
	Enhanced Flex PWM with Input Capture	0	0	3	0	0	3
	PWM Fault Inputs (from Crossbar Input)	4	4	4	4	4	4
12-bit ADC with x1, 2x, 4x Programmable Gain		2 x 4Ch	2 x 5Ch	2 x 8Ch	2 x 4Ch	2 x 5 Ch	2 x 8 Ch
Analog comparators (ACMP) each with integrated 5-bit DAC		3					
12-bit DAC		1					
Cyclic Redundancy Check (CRC)		Yes					
Inter-Integrated Circuit (I^2C) / SMBus		2					
Queued Serial peripheral Interface (QSPI)		1					
High speed Queued Serial Communications Interface (QSCI)[1]		2					
Controller Area Network (MSCAN)		0			1		
High Speed 16-bit multi-purpose timers (TMR)[2]		8					
Computer operating properly (COP) watchdog timer		Yes					
Integrated Power-On Reset and low voltage detection		Yes					
Phase-locked loop (PLL)		Yes					
8 MHz (400 kHz at standby mode) on-chip ROSC		Yes					
Crystal/resonator oscillator		Yes					
Crossbar	Input pins	6	6	6	6	6	6
	Output pins	2	2	6	2	2	6
General purpose I/O (GPIO)[3]		35	39	54	35	39	54
IEEE 1149.1 Joint Test Action Group (JTAG) interface		Yes					
Enhanced on-chip emulator (EOnCE)		Yes					
Operating temperature range	V temperature devices	–40 °C to 105 °C					
	M temperature devices	–40 °C to 125 °C					
Package		44LQFP	48LQFP	64LQFP	44LQFP	48LQFP	64LQFP

1 Can be clocked by high speed peripheral clock up to 120 MHz

2 Can be clocked by high speed peripheral clock up to 120 MHz

3 Shared with other function pins

2 Overview

2.1 MC56F825x/MC56F824x Features

2.1.1 Core

- Efficient 56800E digital signal processor (DSP) engine with modified Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.1.2 Operation Range

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range
  - V temperature devices: –40 °C to +105 °C
  - M temperature devices: –40 °C to +125 °C

2.1.3 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K x 16) to 64 KB (32K x 16) on-chip flash memory with 2048 bytes (1024 x 16) page size
- 6 KB (3K x 16) to 8 KB (4K x 16) on-chip RAM with byte addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

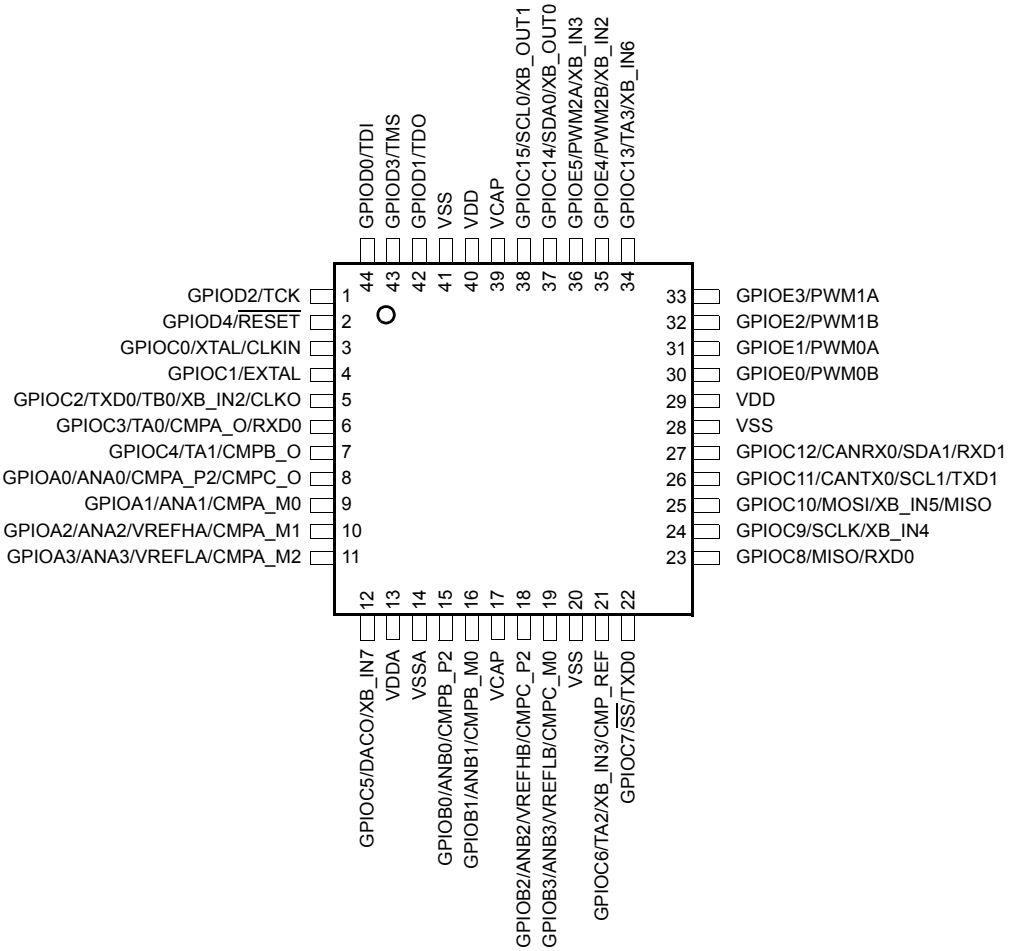


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

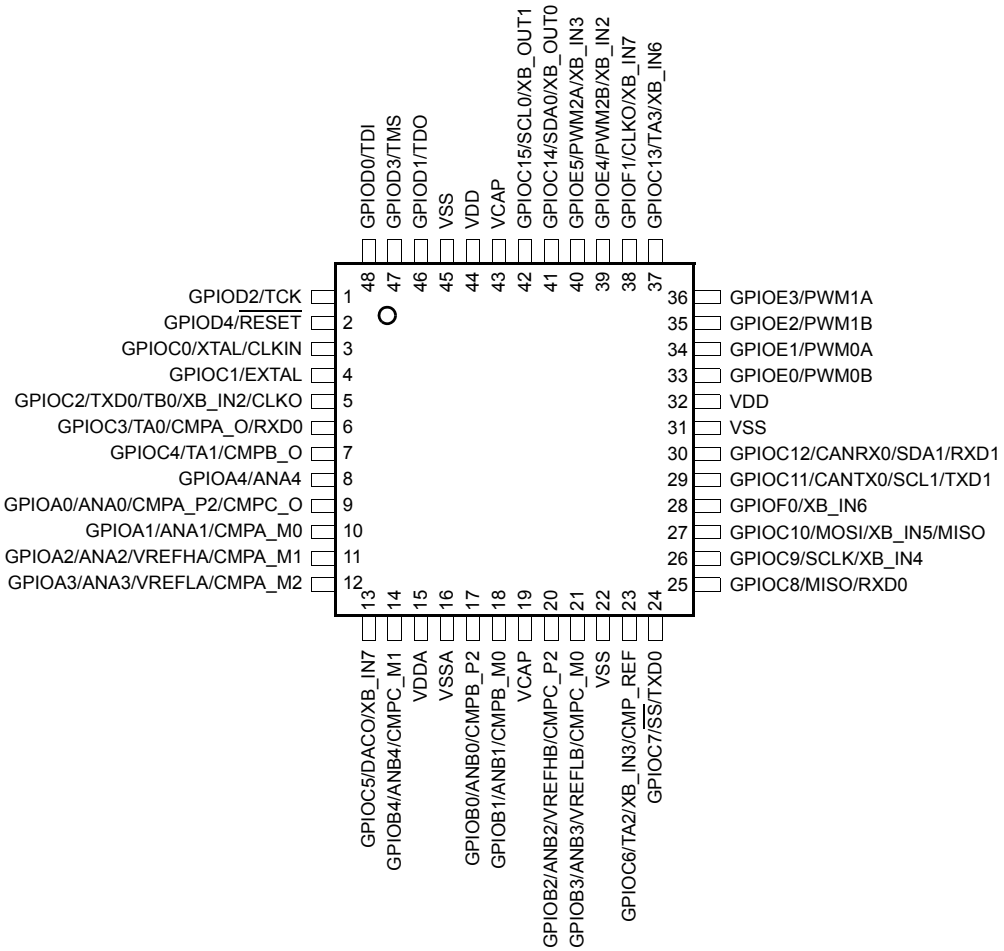


Figure 4. Top View: 56F8246 and 56F8256 48-Pin LQFP Package

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC10	25	27	35	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)				Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(XB_IN5)				Input		XB_IN5 — Crossbar module input 5
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOC10.
GPIOC11	26	29	37	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANTX)				Open-drain Output		CANTX — CAN transmit data output (not available on 56F8245/46/47)
(SCL1)				Input/ Open-drain Output		SCL1 — I^2C1 serial clock
(TXD1)				Output		TXD1 — SCI1 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC11.
GPIOC12	27	30	38	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANRX)				Input		CANRX — CAN receive data input (not available on 56F8245/46/47)
(SDA1)				Input/ Open-drain Output		SDA1 — I^2C1 serial data line
(RXD1)				Input		RXD1 — SCI1 receive data input After reset, the default state is GPIOC12.
GPIOC13	34	37	49	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA3)				Input/ Output		TA3 — Quad timer module A channel 3input/output.
(XB_IN6)				Input		XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOC13.

[2] This RAM is shared with program space starting at P: 0x00 8000. See Figure 6 and Figure 7.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This mapping eases online reprogramming of on-chip flash.

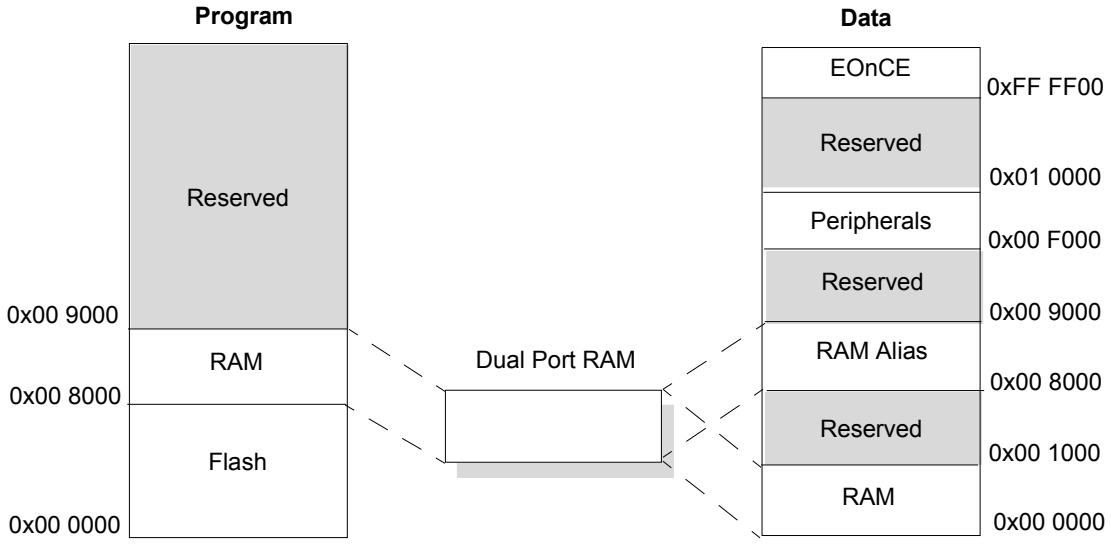


Figure 6. 56F8255/56/57 Dual Port RAM Map

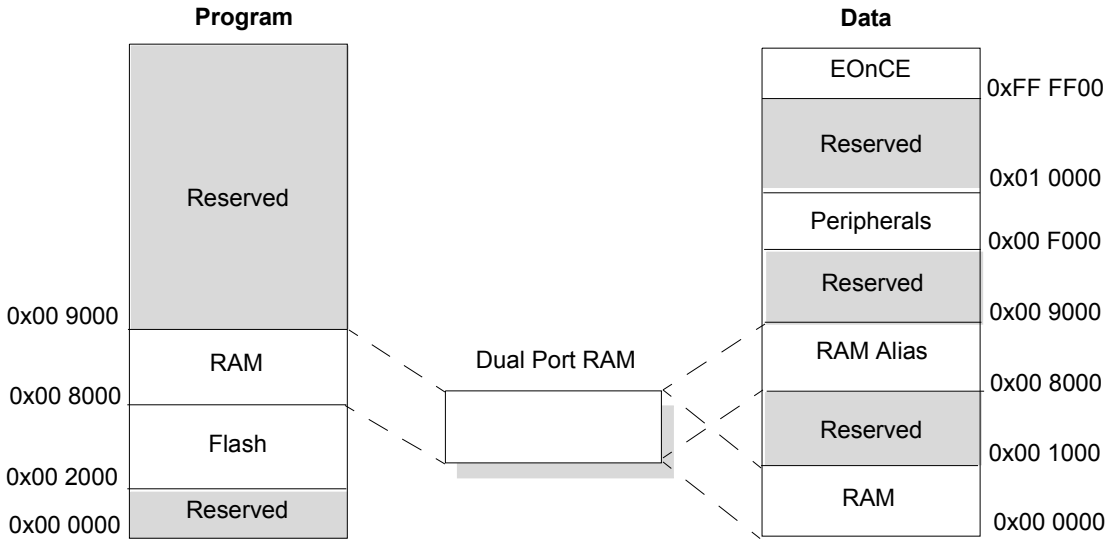


Figure 7. 56F8247 Dual Port RAM Map

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

Table 15. Crossbar Input Signal Assignments

XBAR_INn	Input from	Function
XBAR_IN0	Logic Zero	V_{SS}
XBAR_IN1	Logic One	V_{DD}
XBAR_IN2	XB_IN2	Package pin
XBAR_IN3	XB_IN3	Package pin
XBAR_IN4	XB_IN4	Package pin
XBAR_IN5	XB_IN5	Package pin
XBAR_IN6	XB_IN6	Package pin
XBAR_IN7	XB_IN7	Package pin
XBAR_IN8	Unused	
XBAR_IN9	CMPA_OUT	Comparator A Output
XBAR_IN10	CMPB_OUT	Comparator B Output
XBAR_IN11	CMPC_OUT	Comparator C Output
XBAR_IN12	TB0	Quad Timer B0 Output
XBAR_IN13	TB1	Quad Timer B1 Output
XBAR_IN14	TB2	Quad Timer B2 Output
XBAR_IN15	TB3	Quad Timer B3 Output
XBAR_IN16	PWM0_TRIG_COMB	eFlexPWM submodule 0: PWM0_OUT_TRIG0 or PWM0_OUT_TRIG1
XBAR_IN17	PWM1_TRIG_COMB	eFlexPWM submodule 1: PWM1_OUT_TRIG0 or PWM1_OUT_TRIG1
XBAR_IN18	PWM2_TRIG_COMB	eFlexPWM submodule 2: PWM2_OUT_TRIG0 or PWM2_OUT_TRIG1
XBAR_IN19	PWM[012]_TRIG_COMB	eFlexPWM submodule 0, 1, or 2; PWM0_TRIG_COMB or PWM1_TRIG_COMB or PWM2_TRIG_COMB
XBAR_IN20	PWM3_TRIG0	eFlexPWM submodule 3: PWM3_OUT_TRIG0
XBAR_IN21	PWM3_TRIG1	eFlexPWM submodule 3: PWM3_OUT_TRIG1

5.7.2.2 Crossbar Switch Outputs

Table 16 lists the signal assignments of Crossbar Switch outputs.

Table 16. Crossbar Output Signal Assignments

XBAR_OUTn	Output to	Function
XBAR_OUT0	XB_OUT0	Package pin
XBAR_OUT1	XB_OUT1	Package pin
XBAR_OUT2	XB_OUT2	Package pin
XBAR_OUT3	XB_OUT3	Package pin
XBAR_OUT4	XB_OUT4	Package pin
XBAR_OUT5	XB_OUT5	Package pin
XBAR_OUT6	ADCA	ADCA Trigger

Table 16. Crossbar Output Signal Assignments (continued)

XBAR_OUTn	Output to	Function
XBAR_OUT7	ADCB	ADCB Trigger
XBAR_OUT8	DAC	12-bit DAC SYNC_IN
XBAR_OUT9	CMPA	Comparator A Window/Sample
XBAR_OUT10	CMPB	Comparator B Window/Sample
XBAR_OUT11	CMPC	Comparator C Window/Sample
XBAR_OUT12	PWM0 EXTA	eFlexPWM submodule 0 Alternate Control signal
XBAR_OUT13	PWM1 EXTA	eFlexPWM submodule 1 Alternate Control signal
XBAR_OUT14	PWM2 EXTA	eFlexPWM submodule 2 Alternate Control signal
XBAR_OUT15	PWM3 EXTA	eFlexPWM submodule 3 Alternate Control signal
XBAR_OUT16	PWM0 EXT_SYNC	eFlexPWM submodule 0 External Synchronization signal
XBAR_OUT17	PWM1 EXT_SYNC	eFlexPWM submodule 1 External Synchronization signal
XBAR_OUT18	PWM2 EXT_SYNC	eFlexPWM submodule 2 External Synchronization signal
XBAR_OUT19	PWM3 EXT_SYNC	eFlexPWM submodule 3 External Synchronization signal
XBAR_OUT20	PWM EXT_CLK	eFlexPWM External Clock signal
XBAR_OUT21	PWM FAULT0	eFlexPWM Module FAULT0
XBAR_OUT22	PWM FAULT1	eFlexPWM Module FAULT1
XBAR_OUT23	PWM FAULT2	eFlexPWM Module FAULT2
XBAR_OUT24	PWM FAULT3	eFlexPWM Module FAULT3
XBAR_OUT25	PWM FORCE	eFlexPWM External Output Force signal
XBAR_OUT26	TB0	Quad Timer B0 Input when SIM_GPS3[12] is set
XBAR_OUT27	TB1	Quad Timer B1 Input when SIM_GPS3[13] is set
XBAR_OUT28	TB2	Quad Timer B2 Input when SIM_GPS3[14] is set
XBAR_OUT29	TB3	Quad Timer B3 Input when SIM_GPS3[15] is set

5.7.3 Interconnection of PWM Module and ADC Module

In addition to how PWM0_EXTA, PWM1_EXTA, PWM2_EXTA, and PWM3_EXTA connect to crossbar outputs, the ADC conversion high/low limit compare results of sample0, sample1, and sample2 are used to drive PWM0_EXTB, PWM1_EXTB, and PWM2_EXTB, respectively. PWM3_EXTB is permanently tied to GND.

State of PWM0_EXTB:

- If the ADC conversion result in SAMPLE0 is greater than the value programmed into the high limit register 0, PWM0_EXTB is driven low.
- If the ADC conversion result in SAMPLE0 is less than the value programmed into the low limit register 0, PWM0_EXTB is driven high.

State of PWM1_EXTB:

- If the ADC conversion result in SAMPLE1 is greater than the value programmed into the high limit register 1, PWM1_EXTB is driven low.

word ensures that the device remains secure after the next reset (caused, for example, by the device powering down). Refer to the flash memory section of the device's reference manual for details.

When flash security mode is enabled, the MC56F825x/MC56F824x disables the core's EOnCE debug capabilities. Normal program execution is otherwise unaffected.

6.2 Flash Access Lock and Unlock Mechanisms

Several methods effectively lock or unlock the on-chip flash.

6.2.1 Disabling EOnCE Access

You can read on-chip flash by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TCK, TMS, TDO, and TDI pins compose a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG port is active and provides the chip's boundary scan capability and access to the ID register. However, proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

6.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field. The erasure disables security by clearing the protection register. This approach does not compromise security. The entire contents of your secured code stored in flash are erased before the next reset or power-up sequence, when security becomes disabled.

To start the lockout recovery sequence via JTAG, first shift the JTAG public instruction (LOCKOUT_RECOVERY) into the chip-level TAP controller's instruction register. Then shift the clock divider value into the corresponding 7-bit data register. Finally, the TAP controller must enter the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the device's reference manual for details, or contact Freescale.

NOTE

After completion of the lockout recovery sequence, you must reset the JTAG TAP controller and the device to return to normal unsecured operation. A power-on reset resets both.

6.2.3 Flash Lockout Recovery Using CodeWarrior

You can use CodeWarrior to unlock a device by selecting the following items in the indicated sequence:

1. Debug menu
2. DSP56800E
3. Unlock Flash

You can accomplish the same task with another CodeWarrior mechanism that uses the device's memory configuration file: the command "Unlock_Flash_on_Connect 1" in the .cfg file.

This lockout recovery mechanism completely erases the internal flash contents, including the configuration field, thereby disabling security (the protection register is cleared).

7.17 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 33. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration [3]	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 19
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

3 This minimum number guarantees that a reliable reset occurs.

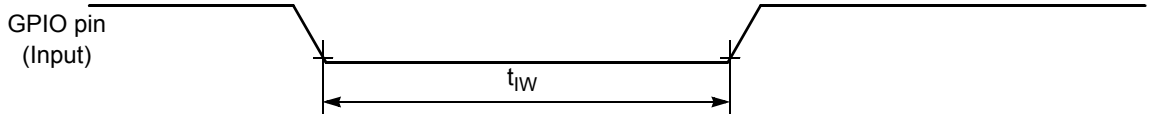


Figure 19. GPIO Interrupt Timing (Negative Edge-Sensitive)

7.18 Queued Serial Peripheral Interface (SPI) Timing

Table 34. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	Refer to
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 23
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 23
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 23

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

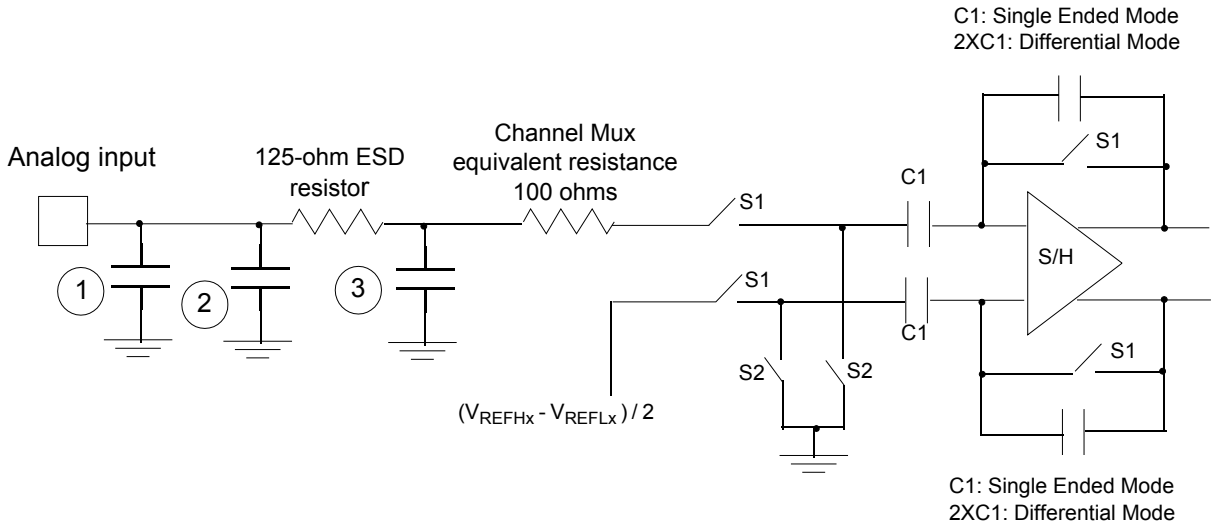
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.



1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case. Refer to Equation 5.

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^{O}C)

Ψ_{JT} = Thermal characterization parameter (^{O}C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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	CASE NUMBER: 840F–02	11 AUG 2006
	STANDARD: JEDEC MS–026 BCD	

Figure 34. 56F8247 and 56F8257 64-Pin LQFP Mechanical Information

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CAN	25	0–2	P:0x32	CAN Error Interrupt
CAN	26	0–2	P:0x34	CAN Wake-Up Interrupt
QSCI1	27	0–2	P:0x36	QSCI1 Receiver Overrun/Errors
QSCI1	28	0–2	P:0x38	QSCI1 Receiver Full
QSCI1	29	0–2	P:0x3A	QSCI1 Transmitter Idle
QSCI1	30	0–2	P:0x3C	QSCI1 Transmitter Empty
QSCI0	31	0–2	P:0x3E	QSCI0 Receiver Overrun/Errors
QSCI0	32	0–2	P:0x40	QSCI0 Receiver Full
QSCI0	33	0–2	P:0x42	QSCI0 Transmitter Idle
QSCI0	34	0–2	P:0x44	QSCI0 Transmitter Empty
QSPI	35	0–2	P:0x46	SPI Transmitter Empty
QSPI	36	0–2	P:0x48	SPI Receiver Full
I^2C1	37	0–2	P:0x4A	I^2C1 Interrupt
I^2C0	38	0 -2	P:0x4C	I^2C0 Interrupt
TMRA3	39	0 -2	P:0x4E	Quad Timer A, Channel 3 Interrupt
TMRA2	40	0 -2	P:0x50	Quad Timer A, Channel 2 Interrupt
TMRA1	41	0 -2	P:0x52	Quad Timer A, Channel 1 Interrupt
TMRA0	42	0 -2	P:0x54	Quad Timer A, Channel 0 Interrupt
eFlexPWM	43	0 -2	P:0x56	PWM Fault
eFlexPWM	44	0 -2	P:0x58	PWM Reload Error
eFlexPWM	45	0 -2	P:0x5A	PWM Sub-Module 3 Reload
eFlexPWM	46	0 -2	P:0x5C	PWM Sub-Module 3 input capture
eFlexPWM	47	0 -2	P:0x5E	PWM Sub-Module 3 Compare
eFlexPWM	48	0 -2	P:0x60	PWM Sub-Module 2 Reload
eFlexPWM	49	0 -2	P:0x62	PWM Sub-Module 2 Compare
eFlexPWM	50	0 -2	P:0x64	PWM Sub-Module 1 Reload
eFlexPWM	51	0 -2	P:0x66	PWM Sub-Module 1 Compare
eFlexPWM	52	0 -2	P:0x68	PWM Sub-Module 0 Reload
eFlexPWM	53	0 -2	P:0x6A	PWM Sub-Module 0Compare
FM	54	0 -2	P:0x6C	Flash Memory Access Error
FM	55	0 -2	P:0x6E	Flash Memory Programming Command Complete
FM	56	0 -2	P:0x70	Flash Memory Buffer Empty Request
CMPC	57	0–2	P:0x72	Comparator C Rising/Falling Flag
CMPB	58	0–2	P:0x74	Comparator B Rising/Falling Flag

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CMPA	59	0–2	P:0x76	Comparator A Rising/Falling Flag
GPIOF	60	0–2	P:0x78	GPIOF Interrupt
GPIOE	61	0–2	P:0x7A	GPIOE Interrupt
GPIOD	62	0–2	P:0x7C	GPIOD Interrupt
GPIOC	63	0–2	P:0x7E	GPIOC Interrupt
GPIOB	64	0–2	P:0x80	GPIOB Interrupt
GPIOA	65	0–2	P:0x82	GPIOA Interrupt
SWILP	66	-1	P:0x84	SW Interrupt Low Priority

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

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