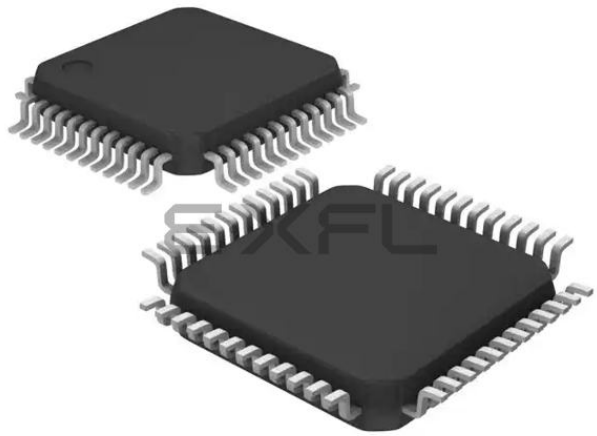

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8246vlf

Table of Contents

2 Overview

2.1 MC56F825x/MC56F824x Features

2.1.1 Core

- Efficient 56800E digital signal processor (DSP) engine with modified Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.1.2 Operation Range

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range
  - V temperature devices: –40 °C to +105 °C
  - M temperature devices: –40 °C to +125 °C

2.1.3 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K x 16) to 64 KB (32K x 16) on-chip flash memory with 2048 bytes (1024 x 16) page size
- 6 KB (3K x 16) to 8 KB (4K x 16) on-chip RAM with byte addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

  - Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8 channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency: up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First 8 samples have Offset, Limit and Zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger
- Inter-module Crossbar Switch (XBAR)
  - Programmable internal module connections among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, Timer input/output, ADC triggers, and Comparator outputs
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator
- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power down mode
  - Output can be routed to internal comparator, or off chip
- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - Support LIN slave operation

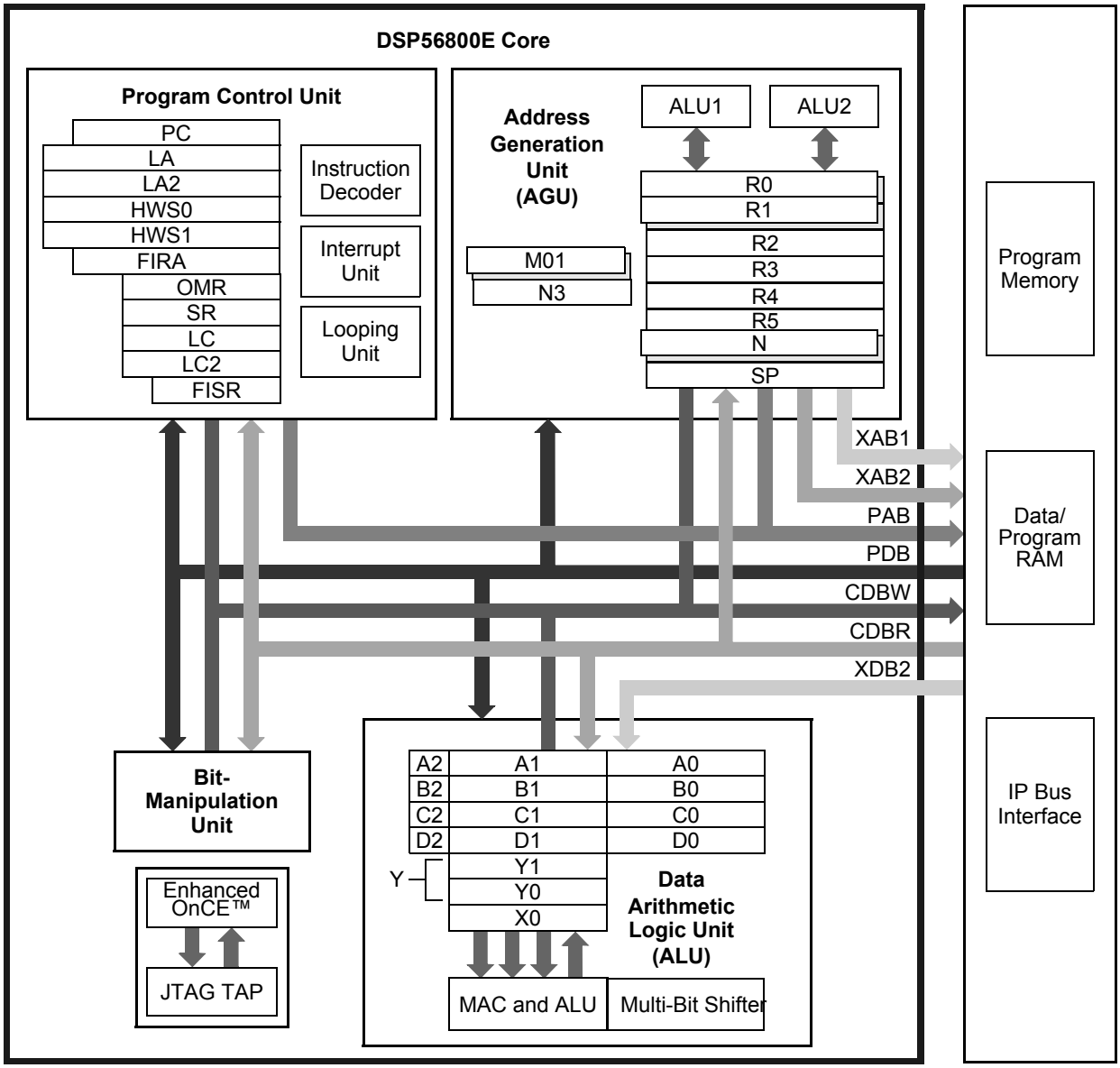


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

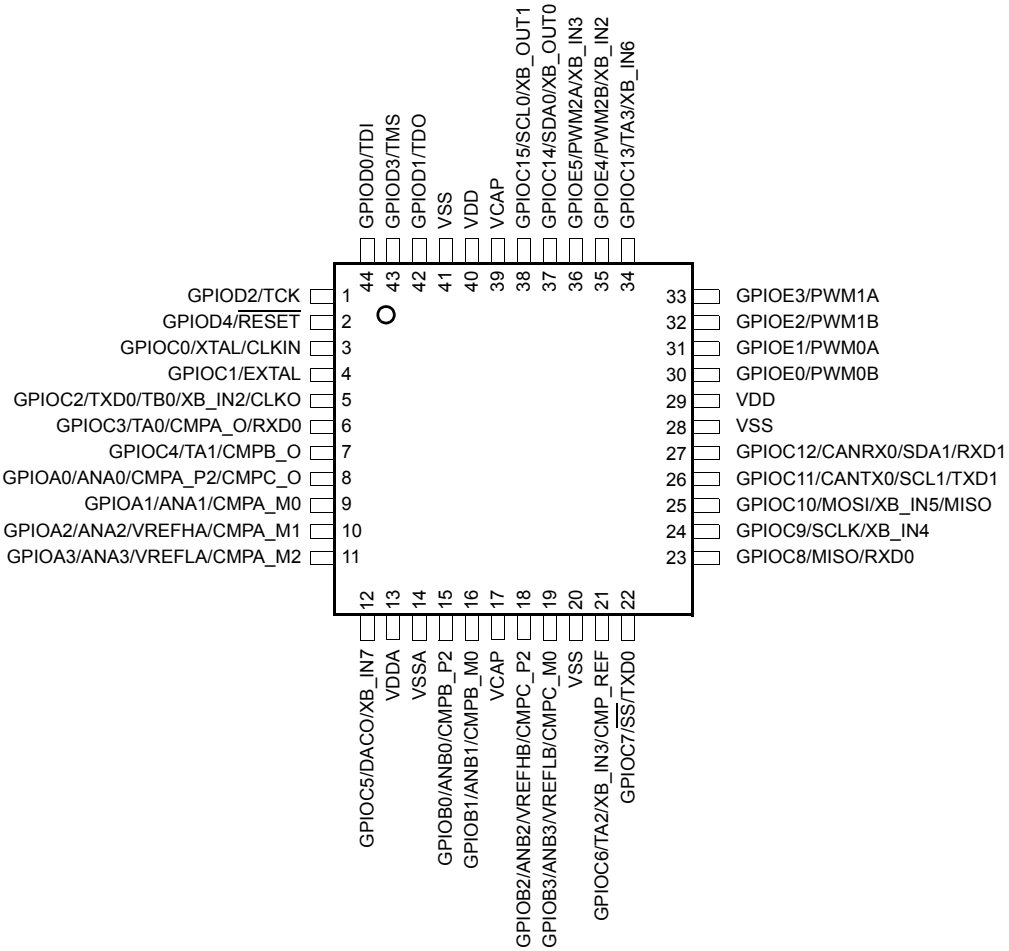


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB0 *(ANB0& CMPB_P2)*	15	17	24	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0 and CMPB_P2 — Analog input to channel 0 of ADCB and positive input 2 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_P2. After reset, the default state is GPIOB0.
GPIOB1 *(ANB1& CMPB_M0)*	16	18	25	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1 and CMPB_M0— Analog input to channel 1 of ADCB and negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_M0. After reset, the default state is GPIOB1.
GPIOB2 *(ANB2& VREFHB& CMPC_P2)*	18	20	27	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2 and VREFHB and CMPC_P2 — Analog input to channel 2 of ADCB and analog references high of ADCB and positive input 2 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_P2. ADC control register configures this input as ANB2 or VREFHB. After reset, the default state is GPIOB2.
GPIOB3 *(ANB3& VREFLB& CMPC_M0)*	19	21	28	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3 and VREFLB and CMPC_M0 — Analog input to channel 3 of ADCB and analog references low of ADCB and negative input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and MPC_M0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOE4 *(PWM2B)* *(XB_IN2)*	35	39	51	Input/ Output Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2B — NanoEdge PWM submodule 2 output B XB_IN2 — Crossbar module input 2 After reset, the default state is GPIOE4.
GPIOE5 *(PWM2A)* *(XB_IN3)*	36	40	52	Input/ Output Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2A — NanoEdge PWM submodule 2 output A XB_IN3 — Crossbar module input 3 After reset, the default state is GPIOE5.
GPIOE6 *(PWM3B)* *(XB_IN4)*			53	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM3B — Enhanced PWM submodule 3 output B or input capture B XB_IN4 — Crossbar module input 4 After reset, the default state is GPIOE6.
GPIOE7 *(PWM3A)* *(XB_IN5)*			54	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM3A — Enhanced PWM submodule 3 output A or input capture A XB_IN5 — Crossbar module input 5 After reset, the default state is GPIOE7.
GPIOF0 *(XB_IN6)*		28	36	Input/ Output Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOF0.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF1		38	50	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOF1.
GPIOF2			39	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCL1)				Input/ Open-drain Output		SCL1 — The I^2C1 serial clock.
(XB_OUT2)				Output		XB_OUT2 — Crossbar module output 2 After reset, the default state is GPIOF2.
GPIOF3			40	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SDA1)				Input/ Open-drain Output		SDA1 — The I^2C1 serial data line.
(XB_OUT3)				Output		XB_OUT3 — Crossbar module output 3 After reset, the default state is GPIOF3.
GPIOF4			41	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD1)				Output		TXD1 — The SCI1 transmit data output or transmit/receive in single wire operation.
(XB_OUT4)				Output		XB_OUT4 — Crossbar module output 4 After reset, the default state is GPIOF4.
GPIOF5			42	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(RXD1)				Output		RXD1 — The SCI1 receive data input.
(XB_OUT5)				Output		XB_OUT5 — Crossbar module output 5 After reset, the default state is GPIOF5.

1 All addresses are 16-bit word addresses.
2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 7.

Table 9. Program Memory Map[1] for 56F8245/46 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8BFF P: 0x00 8000	On-chip RAM[2]: 6 KB
P: 0x00 7FFF P: 0x00 2000	• Internal program flash: 48 KB • Interrupt vector table locates from 0x00 2000 to 0x00 2085 • COP reset address = 0x00 2002 • Boot location = 0x00 2000
P: 0x00 2000 P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.
2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 7.

4.3 Data Map

The MC56F825x/MC56F824x series contains dual access memory. It can be accessed from core primary data buses (XAB1, CDBW, CDBR) and secondary data buses (XAB2, XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map appears in Table 10 and Table 11.

Table 10. 56F8247 and 56F8255/56/57 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-chip peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 9000	RESERVED
X:0x00 8FFF X:0x00 8000	On-chip data RAM alias
X:0x00 7FFF X:0x00 1000	RESERVED
X:0x00 0FFF X:0x00 0000	On-chip data RAM 8 KB[2]

1 All addresses are 16-bit word addresses.

[2] This RAM is shared with program space starting at P: 0x00 8000. See Figure 6 and Figure 7.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This mapping eases online reprogramming of on-chip flash.

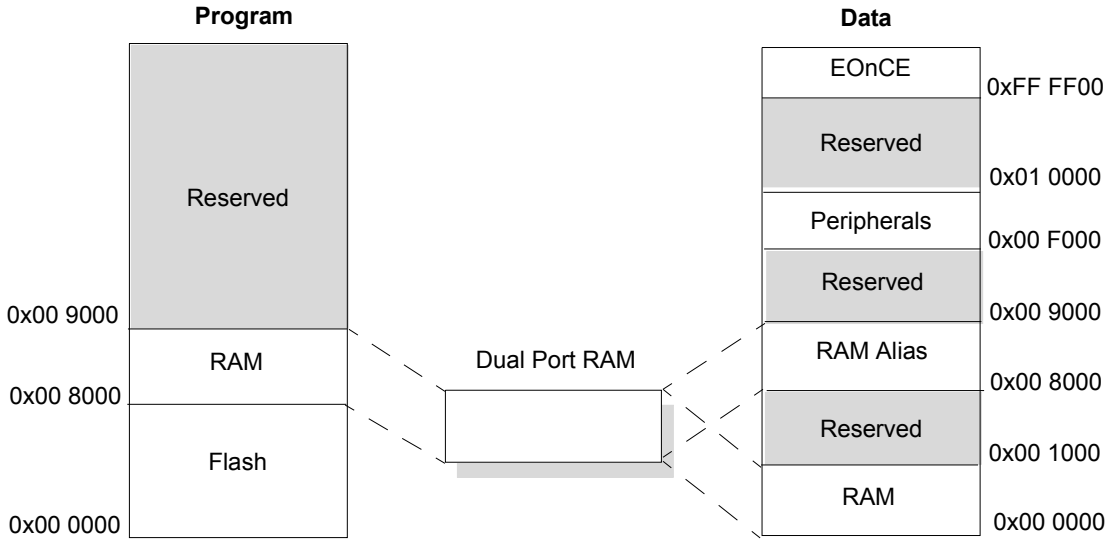


Figure 6. 56F8255/56/57 Dual Port RAM Map

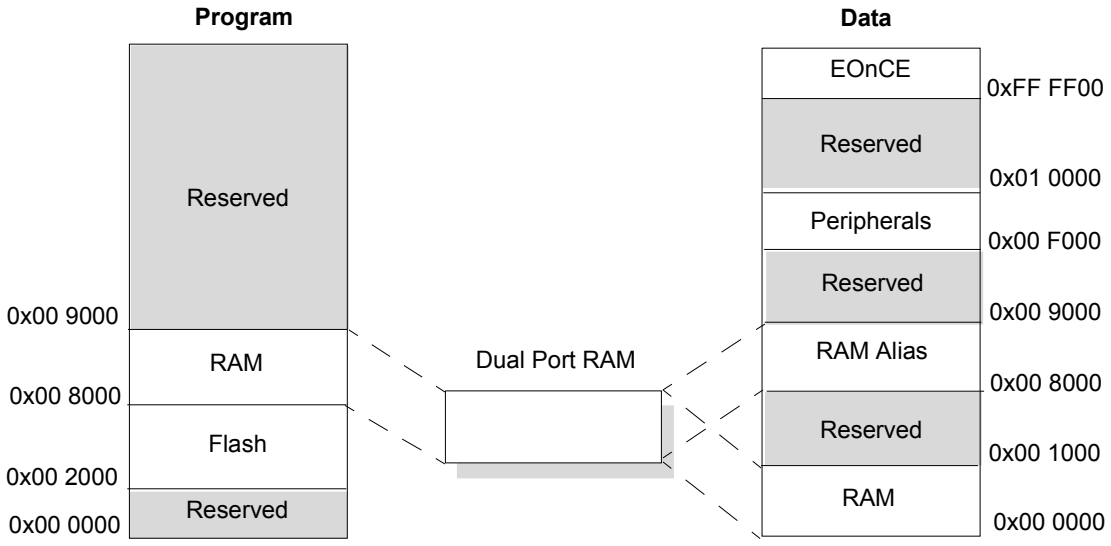


Figure 7. 56F8247 Dual Port RAM Map

- The 56F824x's startup address is located at 0x00 2000. The reset value of VBA is reset to a value of 0x0020 that corresponds to the address 0x00 2000.

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

4.5 Peripheral Memory-Mapped Registers

The locations of on-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary data memory. However, all peripheral registers should be read or written using word accesses only.

Table 12 summarizes the base addresses for the set of peripherals on the MC56F825x/MC56F824x devices. Peripherals are listed in order of the base address.

Table 12. Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address
Quad Timer A	TMRA	X:0x00 F000
Quad Timer B	TMRB	X:0x00 F040
Analog-to-Digital Converter	ADC	X:0x00 F080
Interrupt Controller	INTC	X:0x00 F0C0
System Integration Module	SIM	X:0x00 F0E0
Crossbar module	XBAR	X:0x00 F100
Computer Operating Properly module	COP	X:0x00 F110
On-Chip Clock Synthesis module	OCCS	X:0x00 F120
Power Supervisor	PS	X:0x00 F130
GPIO Port A	GPIOA	X:0x00 F140
GPIO Port B	GPIOB	X:0x00 F150
GPIO Port C	GPIOC	X:0x00 F160
GPIO Port D	GPIOD	X:0x00 F170
GPIO Port E	GPIOE	X:0x00 F180
GPIO Port F	GPIOF	X:0x00 F190
12-bit Digital-to-Analog Converter	DAC	X:0x00 F1A0
Analog Comparator A	CMPA	X:0x00 F1B0
Analog Comparator B	CMPB	X:0x00 F1C0
Analog Comparator C	CMPC	X:0x00 F1D0
Queued Serial Communication Interface 0	QSCI0	X:0x00 F1E0
Queued Serial Communication Interface 1	QSCI1	X:0x00 F1F0
Queued Serial Peripheral Interface	QSPI	X:0x00 F200
Inter-Integrated Circuit 0	I^2C0	X:0x00 F210
Inter-Integrated Circuit 1	I^2C1	X:0x00 F220

Table 12. Data Memory Peripheral Base Address Map Summary (continued)

Peripheral	Prefix	Base Address
Cyclic Redundancy Check Generator	CRC	X:0x00 F230
Comparator Voltage Reference A	REFA	X:0x00 F240
Comparator Voltage Reference B	REFB	X:0x00 F250
Comparator Voltage Reference C	REFB	X:0x00 F260
Enhanced Flex PWM Module	eFlexPWM	X:0x00 F300
Flash Memory Interface	FM	X:0x00 F400
Freescale Controller Area Network [1]	MSCAN	X:0x00 F440

[1] The core must enable clocks to the Freescale Controller Area Network module prior to accessing MSCAN addresses. For details, refer to the MSCAN chapter of the device's reference manual.

4.6 EOnCE Memory Map

Control registers of the EOnCE are located at the top of data memory space. These locations are fixed by the 56800E core. These registers can also be accessed through the JTAG port if flash security is not set. Table 13 lists all EOnCE registers necessary to access or control the EOnCE.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FFFF	OTX1/ORX1	Transmit Register Upper Word Receive Register Upper Word
X:0xFF FFFE	OTX/ORX (32 bits)	Transmit Register Receive Register
X:0xFF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:0xFF FFFC	OCLSR	Core Lock/Unlock Status Register
X:0xFF FFFB– X:0xFF FFA1		Reserved
X:0xFF FFA0	OCR	Control Register
X:0xFF FF9F–X:0xFF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:0xFF FF9D	OSR	Status Register
X:0xFF FF9C	OBASE	Peripheral Base Address Register
X:0xFF FF9B	OTBCR	Trace Buffer Control Register
X:0xFF FF9A	OTBPR	Trace Buffer Pointer Register
X:0xFF FF99–X:0xFF FF98	OTB (21–24 bits/stage)	Trace Buffer Register Stages
X:0xFF FF97–X:0xFF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:0xFF FF95–X:0xFF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:0xFF FF93–X:0xFF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed.

CAUTION

Stress beyond the limits specified in Table 17 may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this section apply over the ambient temperature range (–40 ºC to +105 ºC for V temperature devices or –40 ºC to +125 ºC for M temperature devices) over the following supply ranges:
$V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$ V to 3.6 V, CL $\leq$ 50 pF, $f_{OP} = 60$ MHz.

For functional operating conditions, refer to the remaining tables in the section.

Table 17. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic		Symbol	Notes	Min	Max	Unit
Supply Voltage Range		V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range		V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference		V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}		ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}		ΔV_{SS}		–0.3	0.3	V
Digital Input Voltage Range		V_{IN}	Pin Groups 1, 2	–0.3	6.0	V
Oscillator Voltage Range		V_{OSC}	Pin Group 4	–0.4	4.0	V
Analog Input Voltage Range		V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin (V_{IN} < 0)[1]		V_{IC}		—	-20.0	mA
Output clamp current, per pin (V_O < 0)[1]		V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)		V_{OUT}	Pin Group 1	–0.3	4.0	V
Output Voltage Range (Open Drain mode)		V_{OUTOD}	Pin Group 2	–0.3	6.0	V
DAC Output Voltage Range		V_{OUT_DAC}	Pin Group 5	–0.3	4.0	V
Ambient Temperature	Industrial V	T_A		–40	105	°C
	Industrial M	T_A		–40	125	°C
Junction Temperature		T_J		—	150	°C
Storage Temperature Range (Extended Industrial)		T_{STG}		–55	150	°C

1 Continuous clamp current per pin is –2.0 mA.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC analog output

Table 22. Recommended Operating Conditions (continued) (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1 Total chip source or sink current cannot exceed 75 mA

Default Mode
Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: RESET, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC analog output

7.6 DC Electrical Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 29. External Clock Operation Timing Requirements[1] (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

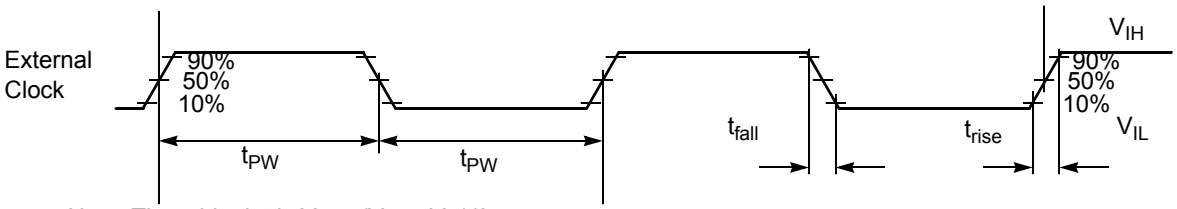
1 Parameters listed are guaranteed by design.

2 See Figure 17 for details on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 17. External Clock Timing

7.14 Phase Locked Loop Timing

Table 30. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	8	MHz
PLL output frequency[2]	f_{op}	120	—	240	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	TBD	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 60 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 60 MHz system clock frequency and using an 8 MHz oscillator frequency.

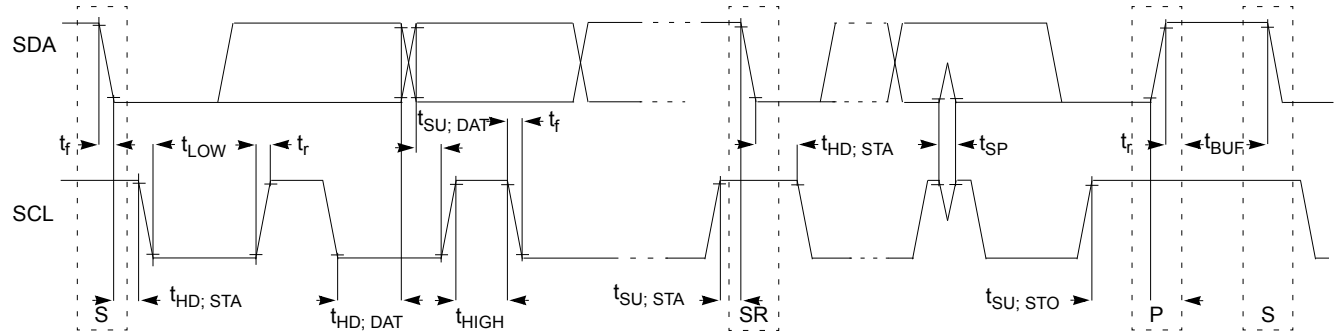


Figure 27. Timing Definition for Standard Mode Devices on the I^2C Bus

7.22 JTAG Timing

Table 38. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	Figure 28
TCK clock pulse width	t_{PW}	50	—	ns	Figure 28
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 29
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 29
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 29
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 29

1 TCK frequency of operation must be less than 1/8 the processor rate.

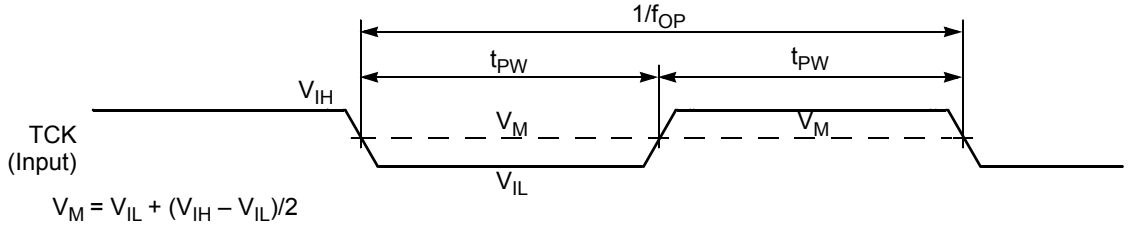


Figure 28. Test Clock Input Timing Diagram

value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case. Refer to Equation 5.

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^{O}C)

Ψ_{JT} = Thermal characterization parameter (^{O}C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical Design Considerations

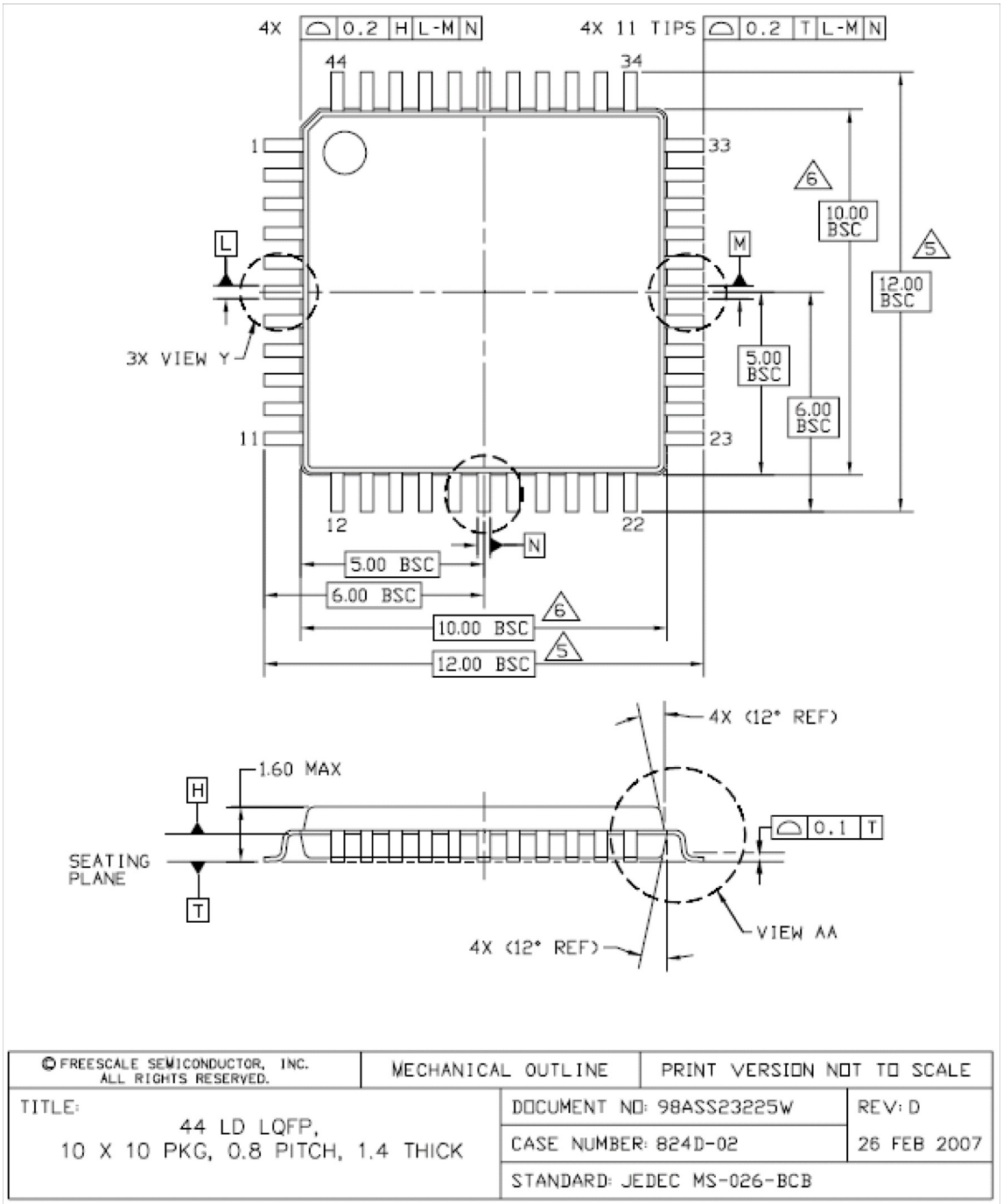
CAUTION

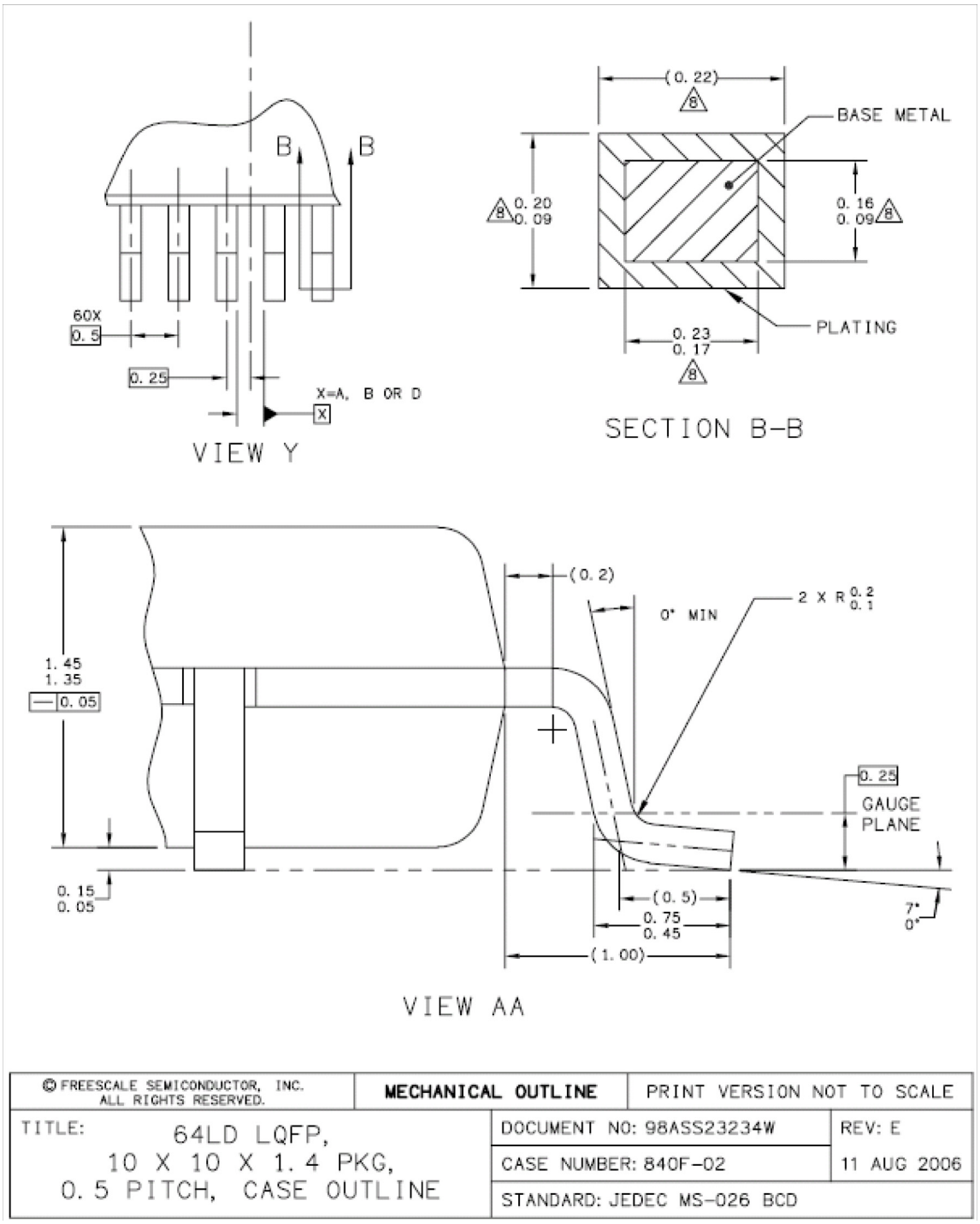
This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

10 Package Mechanical Outline Drawings

To ensure you have the latest version of a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number (shown in the following sections for each package).

10.1 44-pin LQFP





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	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

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