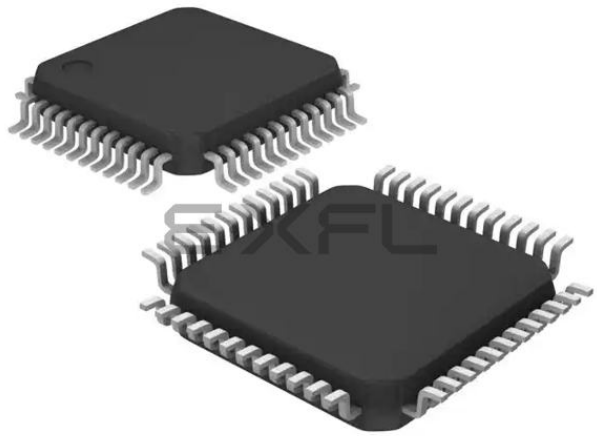

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8246vlfr

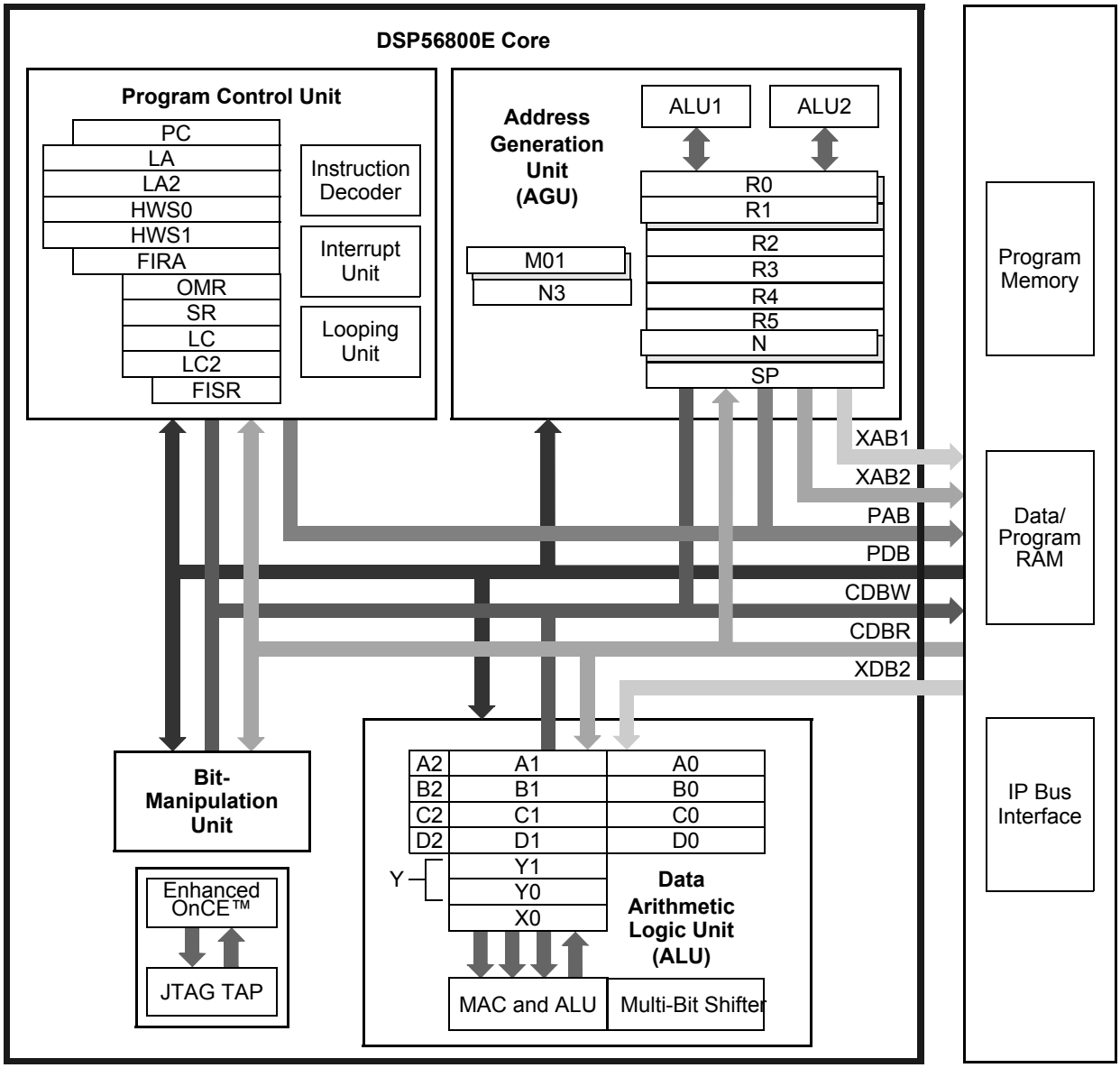


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

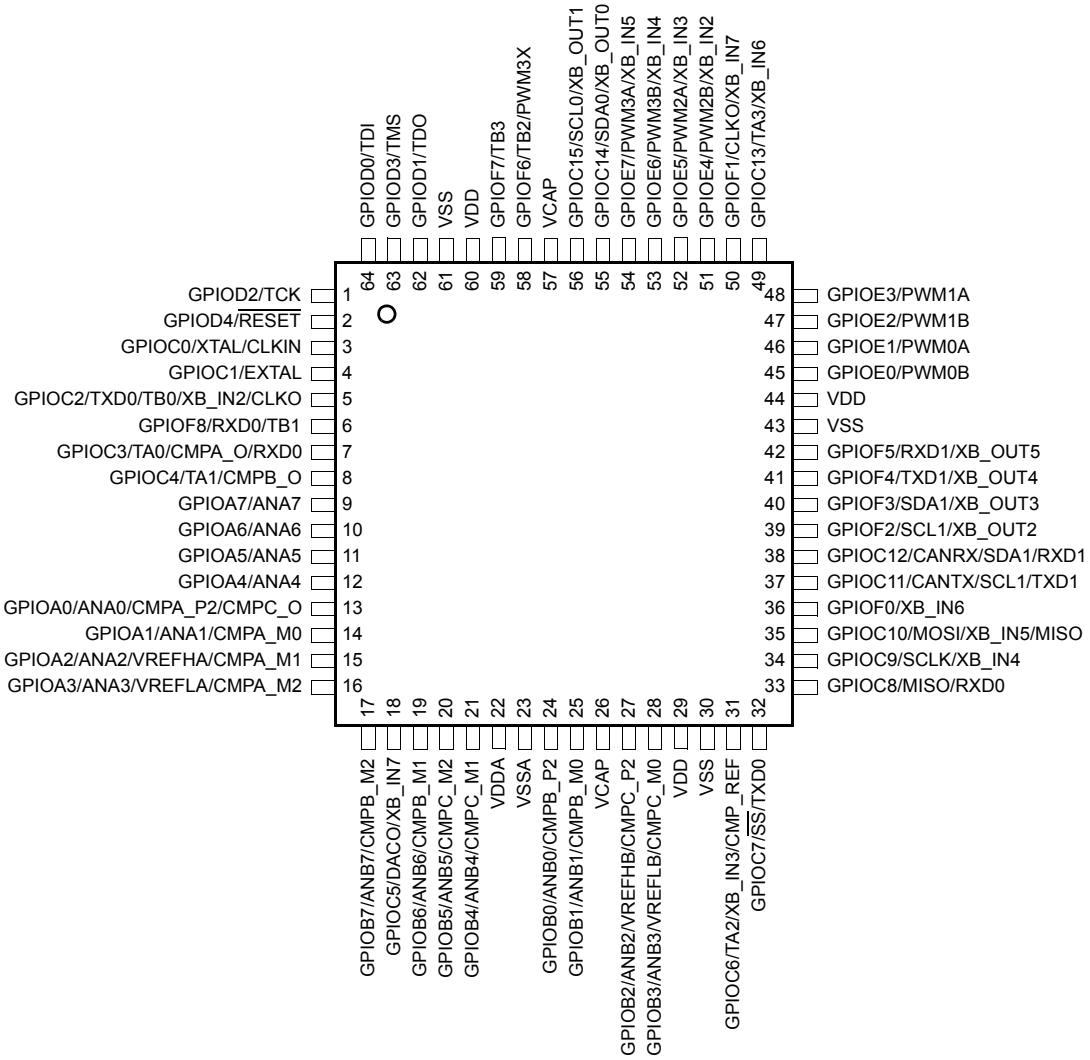


Figure 5. Top View: 56F8247 and 56F8257 64-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB0 *(ANB0& CMPB_P2)*	15	17	24	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0 and CMPB_P2 — Analog input to channel 0 of ADCB and positive input 2 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_P2. After reset, the default state is GPIOB0.
GPIOB1 *(ANB1& CMPB_M0)*	16	18	25	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1 and CMPB_M0— Analog input to channel 1 of ADCB and negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_M0. After reset, the default state is GPIOB1.
GPIOB2 *(ANB2& VREFHB& CMPC_P2)*	18	20	27	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2 and VREFHB and CMPC_P2 — Analog input to channel 2 of ADCB and analog references high of ADCB and positive input 2 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_P2. ADC control register configures this input as ANB2 or VREFHB. After reset, the default state is GPIOB2.
GPIOB3 *(ANB3& VREFLB& CMPC_M0)*	19	21	28	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3 and VREFLB and CMPC_M0 — Analog input to channel 3 of ADCB and analog references low of ADCB and negative input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and MPC_M0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC6	21	23	31	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA2)				Input/ Output		TA2 — Quad timer module A channel 2 input/output
(XB_IN3)				Input		XB_IN3 — Crossbar module input 3
(CMP_REF)				Analog Input		CMP_REF— Positive input 3 of analog comparator A and B and C
						After reset, the default state is GPIOC6
GPIOC7	22	24	32	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS}$)				Input/ Output		$\overline{SS}$ — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(TXD0)				Output		TXD0 — SCI0 transmit data output or transmit/receive in single wire operation
						After reset, the default state is GPIOC7.
GPIOC8	23	25	33	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		RXD0 — SCI0 receive data input
						After reset, the default state is GPIOC8.
GPIOC9	24	26	34	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)				Input/ Output		SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(XB_IN4)				Input		XB_IN4 — Crossbar module input 4
						After reset, the default state is GPIOC9.

Table 12. Data Memory Peripheral Base Address Map Summary (continued)

Peripheral	Prefix	Base Address
Cyclic Redundancy Check Generator	CRC	X:0x00 F230
Comparator Voltage Reference A	REFA	X:0x00 F240
Comparator Voltage Reference B	REFB	X:0x00 F250
Comparator Voltage Reference C	REFB	X:0x00 F260
Enhanced Flex PWM Module	eFlexPWM	X:0x00 F300
Flash Memory Interface	FM	X:0x00 F400
Freescale Controller Area Network [1]	MSCAN	X:0x00 F440

[1] The core must enable clocks to the Freescale Controller Area Network module prior to accessing MSCAN addresses. For details, refer to the MSCAN chapter of the device's reference manual.

4.6 EOnCE Memory Map

Control registers of the EOnCE are located at the top of data memory space. These locations are fixed by the 56800E core. These registers can also be accessed through the JTAG port if flash security is not set. Table 13 lists all EOnCE registers necessary to access or control the EOnCE.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FFFF	OTX1/ORX1	Transmit Register Upper Word Receive Register Upper Word
X:0xFF FFFE	OTX/ORX (32 bits)	Transmit Register Receive Register
X:0xFF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:0xFF FFFC	OCLSR	Core Lock/Unlock Status Register
X:0xFF FFFB– X:0xFF FFA1		Reserved
X:0xFF FFA0	OCR	Control Register
X:0xFF FF9F–X:0xFF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:0xFF FF9D	OSR	Status Register
X:0xFF FF9C	OBASE	Peripheral Base Address Register
X:0xFF FF9B	OTBCR	Trace Buffer Control Register
X:0xFF FF9A	OTBPR	Trace Buffer Pointer Register
X:0xFF FF99–X:0xFF FF98	OTB (21–24 bits/stage)	Trace Buffer Register Stages
X:0xFF FF97–X:0xFF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:0xFF FF95–X:0xFF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:0xFF FF93–X:0xFF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

Table 14. Connections by Comparator Inputs (continued)

Comparator Input	Comparator A	Comparator B	Comparator B
M0 (from package pin)	CMPA_M0	CMPB_M0	CMPC_M0
M1 (from package pin)	CMPA_M1	CMPB_M1	CMPC_M1
M2 (from package pin)	CMPA_M2	CMPB_M2	CMPC_M2
M3 (from internal)	12-bit DAC	12-bit DAC	12-bit DAC

5.7.2 Crossbar Switch Connections

The Crossbar Switch module provides a generic mechanism for making connections between on-chip peripherals as well as between peripherals and pins. It provides a purely combinational path from input to output. The module groups 30 identical multiplexes with 22 shared inputs. All Crossbar control registers that are used to select one of the 22 input signals to output are write protected. Control of the write protection setting is in the SIM_PROT register.

In general, the crossbar module connects the Enhanced Flex PWM, ADC, Quad Timers, and comparators together, which allows synchronization between PWM pulse generation and ADC sampling. In addition, several crossbar inputs and outputs are routed to package pins. For example, the user can define an XB_INn pin as a PWM fault protection input that is routed to the PWM module through the crossbar, increasing the flexibility of pin use and reducing the complexity of PCB layout.

word ensures that the device remains secure after the next reset (caused, for example, by the device powering down). Refer to the flash memory section of the device's reference manual for details.

When flash security mode is enabled, the MC56F825x/MC56F824x disables the core's EOnCE debug capabilities. Normal program execution is otherwise unaffected.

6.2 Flash Access Lock and Unlock Mechanisms

Several methods effectively lock or unlock the on-chip flash.

6.2.1 Disabling EOnCE Access

You can read on-chip flash by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TCK, TMS, TDO, and TDI pins compose a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG port is active and provides the chip's boundary scan capability and access to the ID register. However, proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

6.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field. The erasure disables security by clearing the protection register. This approach does not compromise security. The entire contents of your secured code stored in flash are erased before the next reset or power-up sequence, when security becomes disabled.

To start the lockout recovery sequence via JTAG, first shift the JTAG public instruction (LOCKOUT_RECOVERY) into the chip-level TAP controller's instruction register. Then shift the clock divider value into the corresponding 7-bit data register. Finally, the TAP controller must enter the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the device's reference manual for details, or contact Freescale.

NOTE

After completion of the lockout recovery sequence, you must reset the JTAG TAP controller and the device to return to normal unsecured operation. A power-on reset resets both.

6.2.3 Flash Lockout Recovery Using CodeWarrior

You can use CodeWarrior to unlock a device by selecting the following items in the indicated sequence:

1. Debug menu
2. DSP56800E
3. Unlock Flash

You can accomplish the same task with another CodeWarrior mechanism that uses the device's memory configuration file: the command "Unlock_Flash_on_Connect 1" in the .cfg file.

This lockout recovery mechanism completely erases the internal flash contents, including the configuration field, thereby disabling security (the protection register is cleared).

7.3 ESD Protection and Latch-up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing conforms with AEC-Q100 Stress Test Qualification. During device qualification, ESD stresses are performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing conforms with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification. Comprehensive DC parametric and functional testing is performed according to the applicable device specification at room temperature and then at hot temperature, unless specified otherwise in the device specification.

Table 18. MC56F825x/MC56F824x ESD/Latch-up Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A = 85 °C (I_{LAT})	± 100			mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions, unless otherwise noted

7.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the device design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 19. 44LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	57	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	30	°C/W
Junction to case		$R_{\theta JC}$	13	°C/W
Junction to package top	Natural convection	Ψ_{JT}	2	°C/W

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic		Symbol	Notes	Min	Typ	Max	Unit
Supply voltage		V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High		V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}		ΔV_{DD}		–0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}		ΔV_{SS}		–0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source		FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)		V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)		V_{IL}	Pin Groups 1, 2	–0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source		V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low		V_{ILOSC}	Pin Group 4	–0.3		0.8	V
DAC Output Load Resistance		R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance		C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature	Industrial V	T_A		–40		105	°C
	Industrial M	T_A		–40		125	°C
Flash Endurance (Program Erase Cycles)		N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention		T_R	T_J <= 85°C avg	15		—	years

Table 22. Recommended Operating Conditions (continued) (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1 Total chip source or sink current cannot exceed 75 mA

Default Mode
Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: RESET, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC analog output

7.6 DC Electrical Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 23. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	-15 —	-30 0	-60 +/- 2.5	µA	V_{IN} = 0 V
Internal Pull-Up Resistance	$R_{Pull-Up}$		60	110	220	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40 mV	—	Typically V_{DDA} – 40 mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

[1] See Figure 14.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC Analog Output

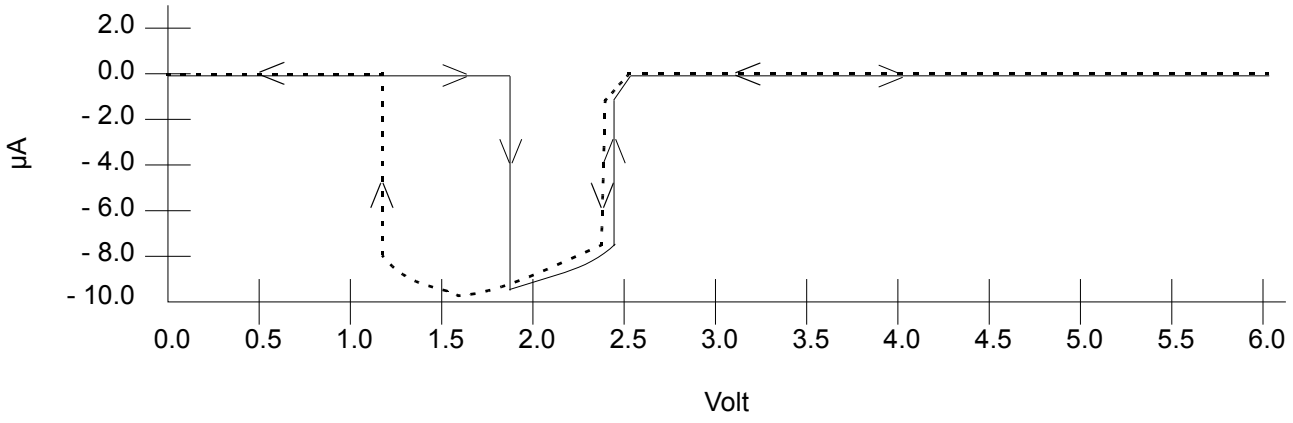


Figure 14. I_{IN}/I_{OZ} versus V_{IN} (Typical; Pull-Up Disabled)

1 No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2 LSB = 0.806 mV

7.27 5-Bit Digital-to-Analog Converter (DAC) Parameters

Table 43. 5-Bit DAC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Inputs	Vin	V_{DDA}	—	V_{DDA}	mV
Setup Delay	t_{PRGST}	TBD	TBD	TBD	ns
Step size	V_{STEP}	3Vin/128	Vin/32	5Vin/128	V
Output Range	V_{DACOUT}	Vin/32	—	Vin	ns

7.28 HSCMP Specifications

Table 44. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Analog input voltage	V_{AIN}	V_{SSA} – 0.01	—	V_{DDA} + 0.01	V
Analog input offset voltage[1]	V_{AIO}	—	—	40	mV
Analog comparator hysteresis[2]	V_H	—	1 to 16	—	mV
Propagation Delay, high speed mode (EN=1, PMODE=1),	t_{DHSN}[3]	—	70	140	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0),	t_{AINIT}[4]	—	400	600	ns

1 Offset when the degree of hysteresis is set to its minimum value.
2 The range of hysteresis is based on simulation only. This range varies from part to part.
3 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.

7.29 Optimize Power Consumption

See Section 7.7, "Supply Current Characteristics," for a list of I_{DD} requirements for the MC56F825x/MC56F824x. This section provides additional details for optimizing power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static] component
+B: internal [state-dependent] component
+C: internal [dynamic] component
+D: external [dynamic] component
+E: external [static] component

A, the internal [static] component, consists of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case. Refer to Equation 5.

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^{O}C)

Ψ_{JT} = Thermal characterization parameter (^{O}C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

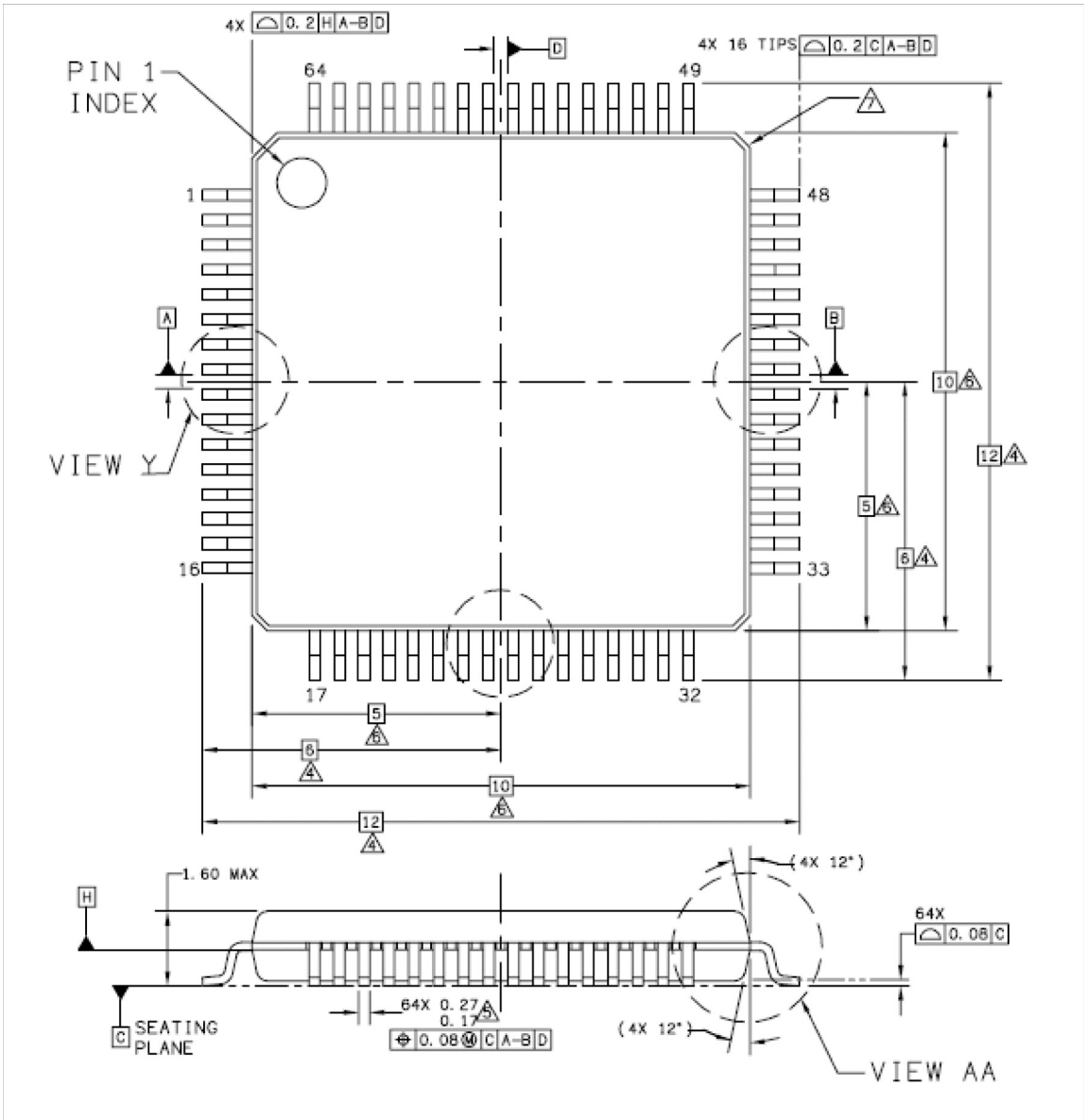
Use the following list of considerations to assure correct operation of the MC56F825x/MC56F824x:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the MC56F825x/MC56F824x and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} is recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ to 10 kΩ; the capacitor value should be in the range of 0.22 µF to 4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if a JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 110 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have an RC filter of no less than 33 pF 10 Ω.
- External clamp diodes on analog input pins are recommended.

9 Ordering Information

Table 46 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

10.3 64-pin LQFP



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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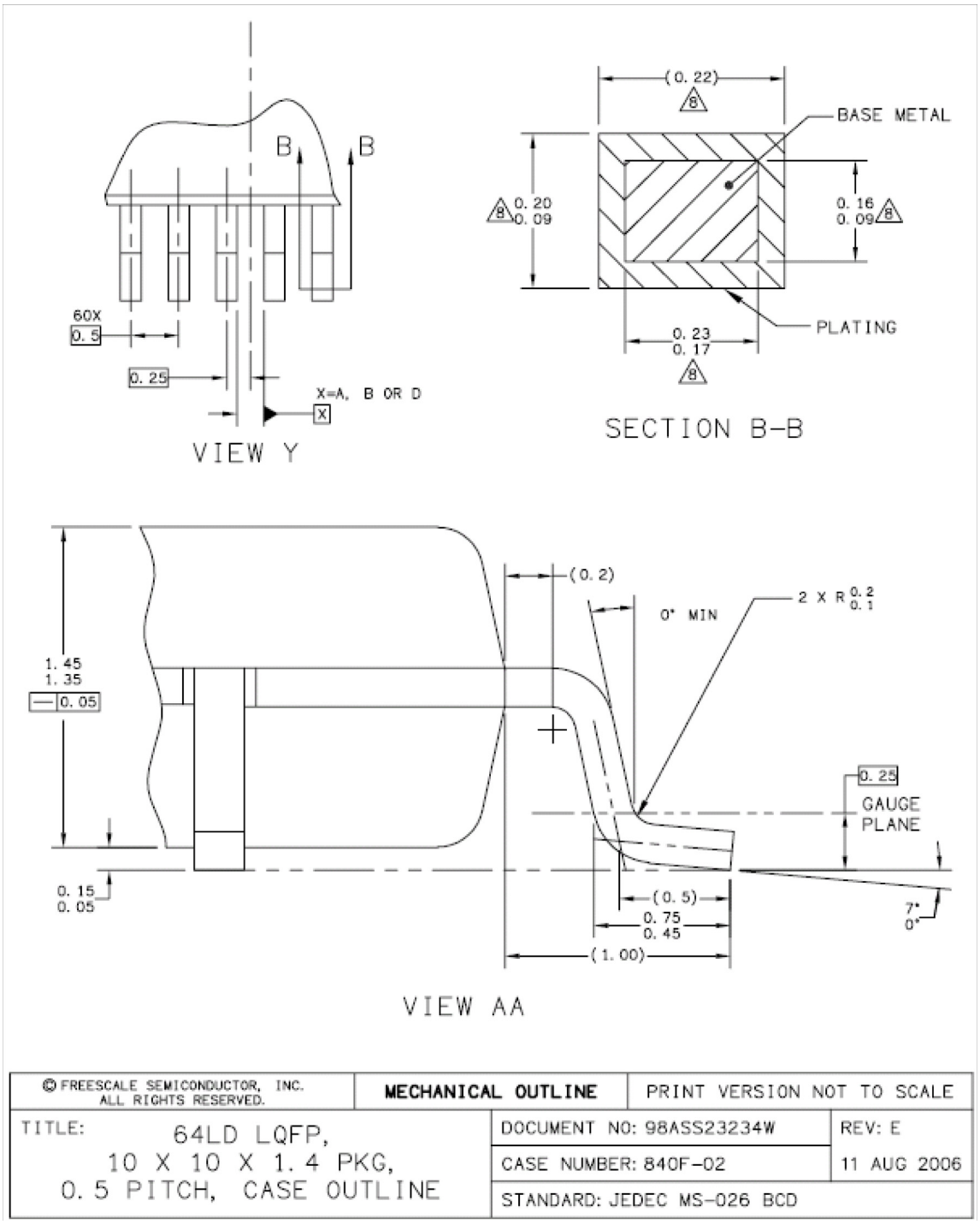
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)
Rev. 4	2014-06-13	Table 17 on page 49: Added data about junction temperature. Added data about M temperature grade devices to operating temperature range information. Operating temperature range information that was present in previous revision is unchanged but now refers to V temperature grade devices. Changes were made at these locations: Table 1 on page 3; Section 2.1.2, “Operation Range” on page 4; Table 17 on page 49; Table 22 on page 52; Table 24 on page 55.