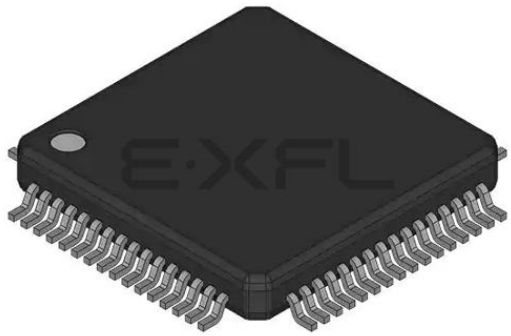


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8247vlhr

1 MC56F825x/MC56F824x Family Configuration

Table 1 compares the MC56F825x/MC56F824x devices.

Table 1. MC56F825x/MC56F824x Device Comparison

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Operation Frequency (MHz)		60					
High Speed Peripheral Clock (MHz)		120					
Flash memory size (KB) with 1024 words per page		48	48	48	64	64	64
RAM size (KB)		6	6	8	8	8	8
Enhanced Flex PWM (eFlexPWM)	High resolution NanoEdge PWM (520 ps res.)	6	6	6	6	6	6
	Enhanced Flex PWM with Input Capture	0	0	3	0	0	3
	PWM Fault Inputs (from Crossbar Input)	4	4	4	4	4	4
12-bit ADC with x1, 2x, 4x Programmable Gain		2 x 4Ch	2 x 5Ch	2 x 8Ch	2 x 4Ch	2 x 5 Ch	2 x 8 Ch
Analog comparators (ACMP) each with integrated 5-bit DAC		3					
12-bit DAC		1					
Cyclic Redundancy Check (CRC)		Yes					
Inter-Integrated Circuit (I^2C) / SMBus		2					
Queued Serial peripheral Interface (QSPI)		1					
High speed Queued Serial Communications Interface (QSCI)[1]		2					
Controller Area Network (MSCAN)		0			1		
High Speed 16-bit multi-purpose timers (TMR)[2]		8					
Computer operating properly (COP) watchdog timer		Yes					
Integrated Power-On Reset and low voltage detection		Yes					
Phase-locked loop (PLL)		Yes					
8 MHz (400 kHz at standby mode) on-chip ROSC		Yes					
Crystal/resonator oscillator		Yes					
Crossbar	Input pins	6	6	6	6	6	6
	Output pins	2	2	6	2	2	6
General purpose I/O (GPIO)[3]		35	39	54	35	39	54
IEEE 1149.1 Joint Test Action Group (JTAG) interface		Yes					
Enhanced on-chip emulator (EOnCE)		Yes					
Operating temperature range	V temperature devices	–40 °C to 105 °C					
	M temperature devices	–40 °C to 125 °C					
Package		44LQFP	48LQFP	64LQFP	44LQFP	48LQFP	64LQFP

1 Can be clocked by high speed peripheral clock up to 120 MHz

2 Can be clocked by high speed peripheral clock up to 120 MHz

3 Shared with other function pins

2.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, and SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, and EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Nested interrupts: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

The masking of interrupt priority level is managed by the 56800E core.

2.1.5 Peripheral Highlights

- One Enhanced Flex Pulse Width Modulator (eFlexPWM) module
  - Up to nine output channels
  - 16-bit resolution for center aligned, edge aligned, and asymmetrical PWMs
  - Each complementary pair can operate with its own PWM frequency based and deadtime values
    - 4 Time base
    - Independent top and bottom deadtime insertion
  - PWM outputs can operate as complimentary pairs or independent channels
  - Independent control of both edges of each PWM output
  - 6-channel NanoEdge high resolution PWM
    - Fractional delay for enhanced resolution of the PWM period and edge placement
    - Arbitrary eFlexPWM edge placement - PWM phase shifting
    - NanoEdge implementation: 520 ps PWM frequency resolution
  - 3 Channel PWM with full Input Capture features
    - Three PWM Channels - PWMA, PWMB, and PWMX
    - Enhanced input capture functionality
  - Support for synchronization to external hardware or other PWM
  - Double buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half cycle reload capability
  - Multiple output trigger events can be generated per PWM cycle via hardware
  - Support for double switching PWM outputs
  - Up to four fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
  - Independently programmable PWM output polarity
  - Individual software control for each PWM output
  - All outputs can be programmed to change simultaneously via a FORCE_OUT event
  - PWMX pin can optionally output a third PWM signal from each submodule
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality

  - Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8 channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency: up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First 8 samples have Offset, Limit and Zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger
- Inter-module Crossbar Switch (XBAR)
  - Programmable internal module connections among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, Timer input/output, ADC triggers, and Comparator outputs
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator
- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power down mode
  - Output can be routed to internal comparator, or off chip
- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - Support LIN slave operation

- One queued serial peripheral interface (QSPI) module
  - Full-duplex operation
  - Four-word deep FIFOs available on both transmit and receive buffers
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency/2
  - 13-bit baud rate divider for low speed communication
- Two inter-integrated circuit (I^2C) ports
  - Operation at up to 100 kbps
  - Support for master and slave operation
  - Support for 10-bit address mode and broadcasting mode
  - Support for SMBus, Version 2
- One Freescale Scalable Controller Area Network (MSCAN) module
  - Fully compliant with CAN protocol Version 2.0 A/B
  - Support for standard and extended data frames
  - Support for data rate up to 1 Mbit/s
  - Five receive buffers and three transmit buffers
- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IP bus to 60 MHz)
- Power supervisor (PS)
  - On-chip linear regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated low voltage detection to generate warning interrupt if VDD is below low voltage detection (LVI) threshold
  - Integrated power-on reset (POR)
    - Reliable reset process during power-on procedure
    - POR is released after VDD passes low voltage detection (LVI) threshold
  - Integrated brown-out reset
  - Run, wait, and stop modes
- Phase lock loop (PLL) providing a high-speed clock to the core and peripherals
  - 2x system clock provided to Quad Timers and SCIs
  - Loss of lock interrupt
  - Loss of reference clock interrupt
- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Cyclic Redundancy Check (CRC) Generator
  - Hardware CRC generator circuit using 16-bit shift register

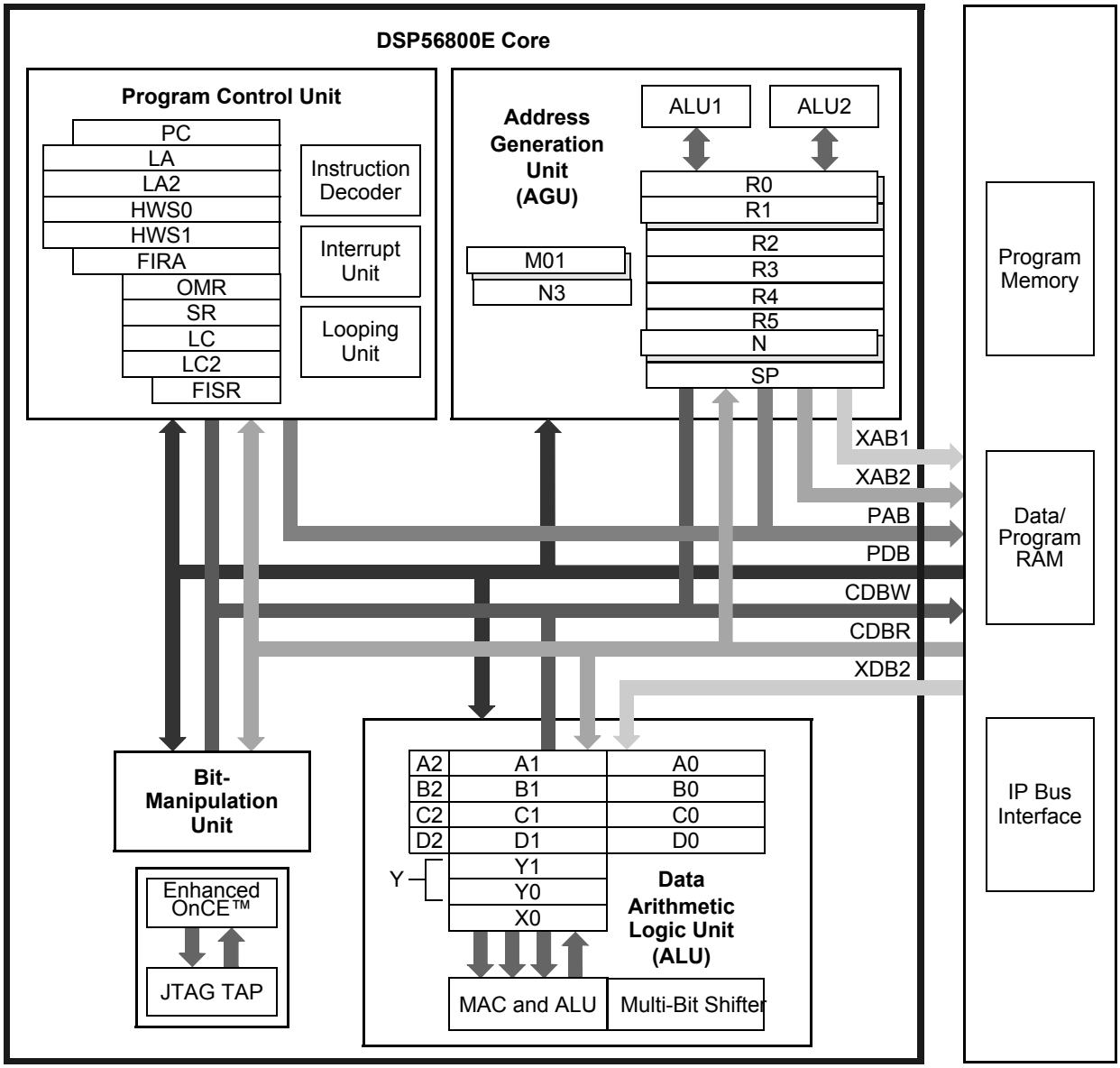


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC14 *(SDA0)* *(XB_OUT0)*	37	41	55	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA0 — I^2C0 serial data line XB_OUT0 — Crossbar module output 0 After reset, the default state is GPIOC14.
GPIOC15 *(SCL0)* *(XB_OUT1)*	38	42	56	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCL0 — I^2C0 serial clock XB_OUT1 — Crossbar module output 1 After reset, the default state is GPIOC15.
GPIOE0 *PWM0B*	30	33	45	Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0B — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE0.
GPIOE1 *(PWM0A)*	31	34	46	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0A — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE1.
GPIOE2 *(PWM1B)*	32	35	47	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1B — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE2.
GPIOE3 *(PWM1A)*	33	36	48	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1A — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE3.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

- Peripheral clocks for Quad Timers and SCIs with a high-speed (2x) option
- Power-saving clock gating for peripherals
- Controls for enabling/disabling functions of large regulator standby mode with write protection capability
- Allowing selected peripherals to run in stop mode to generate stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls for output of internal clock sources to CLKO pin
- Four general-purpose software control registers that are reset only at power-on
- Peripheral stop mode clocking control

5.7 Inter-Module Connections

The operations between on-chip peripherals can be synchronized or cascaded through internal module connections to support particular applications. Examples include synchronization between ADC sampling and PWM waveform generation for a power conversion application, and synchronization between timer pulse outputs and DAC waveform generation for a printer application. The user can program the internal Crossbar Switch or Comparator input multiplexes to connect one on-chip peripheral's outputs to other peripherals' inputs.

5.7.1 Comparator Connections

The MC56F825x/MC56F824x includes three high-speed comparators. Each comparator input has a 4-to-1 input mux, allowing it to sample a variety of analog sources. Some of these inputs share package pins with the on-chip ADCs; see Table 5 on page 18.

Each comparator is paired with a dedicated, programmable, 5-bit on-chip voltage reference DAC (VREF_DAC). Optionally, an on-chip 12-bit DAC can be internally fed to each comparator's positive input 1 (CMPn_P1) or negative input 3 (CMPn_M3). In addition, all three comparators' positive input 3 (CMPn_P3) can be connected together to package pin CMP_REF. Other inputs can be routed to package pins when the corresponding pin is configured for peripheral mode in the GPIO module.

Table 15. Crossbar Input Signal Assignments

XBAR_INn	Input from	Function
XBAR_IN0	Logic Zero	V_{SS}
XBAR_IN1	Logic One	V_{DD}
XBAR_IN2	XB_IN2	Package pin
XBAR_IN3	XB_IN3	Package pin
XBAR_IN4	XB_IN4	Package pin
XBAR_IN5	XB_IN5	Package pin
XBAR_IN6	XB_IN6	Package pin
XBAR_IN7	XB_IN7	Package pin
XBAR_IN8	Unused	
XBAR_IN9	CMPA_OUT	Comparator A Output
XBAR_IN10	CMPB_OUT	Comparator B Output
XBAR_IN11	CMPC_OUT	Comparator C Output
XBAR_IN12	TB0	Quad Timer B0 Output
XBAR_IN13	TB1	Quad Timer B1 Output
XBAR_IN14	TB2	Quad Timer B2 Output
XBAR_IN15	TB3	Quad Timer B3 Output
XBAR_IN16	PWM0_TRIG_COMB	eFlexPWM submodule 0: PWM0_OUT_TRIG0 or PWM0_OUT_TRIG1
XBAR_IN17	PWM1_TRIG_COMB	eFlexPWM submodule 1: PWM1_OUT_TRIG0 or PWM1_OUT_TRIG1
XBAR_IN18	PWM2_TRIG_COMB	eFlexPWM submodule 2: PWM2_OUT_TRIG0 or PWM2_OUT_TRIG1
XBAR_IN19	PWM[012]_TRIG_COMB	eFlexPWM submodule 0, 1, or 2; PWM0_TRIG_COMB or PWM1_TRIG_COMB or PWM2_TRIG_COMB
XBAR_IN20	PWM3_TRIG0	eFlexPWM submodule 3: PWM3_OUT_TRIG0
XBAR_IN21	PWM3_TRIG1	eFlexPWM submodule 3: PWM3_OUT_TRIG1

5.7.2.2 Crossbar Switch Outputs

Table 16 lists the signal assignments of Crossbar Switch outputs.

Table 16. Crossbar Output Signal Assignments

XBAR_OUTn	Output to	Function
XBAR_OUT0	XB_OUT0	Package pin
XBAR_OUT1	XB_OUT1	Package pin
XBAR_OUT2	XB_OUT2	Package pin
XBAR_OUT3	XB_OUT3	Package pin
XBAR_OUT4	XB_OUT4	Package pin
XBAR_OUT5	XB_OUT5	Package pin
XBAR_OUT6	ADCA	ADCA Trigger

- If the ADC conversion result in SAMPLE1 is less than the value programmed into the low limit register 1, PWM1_EXTB is driven high.

State of PWM2_EXTB:

- If the ADC conversion result in SAMPLE2 is greater than the value programmed into the high limit register 2, PWM2_EXTB is driven low.
- If the ADC conversion result in SAMPLE2 is less than the value programmed into the low limit register 2, PWM2_EXTB is driven high.

5.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The 56800E family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation (EOnCE) module and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the MC56F825x/MC56F824x into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The 56800E's EOnCE module is a Freescale-designed module for developing and debugging application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the 56800E core. Among the many features of the EOnCE module is support, in real-time program execution, for data communication between the controller and the host software development and debug systems. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources must be sacrificed to perform debugging operations.

The 56800E's JTAG port provides an interface for the EOnCE module to the JTAG pins. The Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state (if this pin is not configured as GPIO).

6 Security Features

The MC56F825x/MC56F824x offers security features intended to prevent unauthorized users from gaining access to and reading the contents of the flash memory (FM) array. The MC56F825x/MC56F824x's flash memory security consists of several hardware interlocks.

After flash memory security is set, the application software can allow an authorized user to access on-chip memory by including a user-defined software subroutine that reads and transfers the contents of internal memory via peripherals. This application software can communicate over a serial port, for example, to validate the authenticity of the requested access and then to grant it until the next device reset. The system designer must use discretion when deciding whether to support this type of "back door" access technique.

6.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of programming the flash with the application code, you can secure the MC56F825x/MC56F824x by programming the values 1 and 0 into bits 1 and 0, respectively, of program memory location 0x00_7FF7. The CodeWarrior IDE menu flash lock command can also accomplish this task. The nonvolatile security

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic		Symbol	Notes	Min	Typ	Max	Unit
Supply voltage		V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High		V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}		ΔV_{DD}		–0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}		ΔV_{SS}		–0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source		FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)		V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)		V_{IL}	Pin Groups 1, 2	–0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source		V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low		V_{ILOSC}	Pin Group 4	–0.3		0.8	V
DAC Output Load Resistance		R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance		C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature	Industrial V	T_A		–40		105	°C
	Industrial M	T_A		–40		125	°C
Flash Endurance (Program Erase Cycles)		N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention		T_R	T_J <= 85°C avg	15		—	years

7.7 Supply Current Characteristics

The following table specifies supply current characteristics.

Table 24. Current Consumption

Mode	Conditions	Typical @ 3.3 V 25°C (mA)		Maximum @ 3.6 V 105 °C (V temperature) 125 °C (M temperature) (mA)	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	60 MHz device clock Relaxation oscillator on PLL powered on Continuous MAC instructions with fetches from program flash memory All peripheral modules enabled; TMRs and SCIs using 1X Clock ADC/DAC powered on and clocked Comparator powered on	92	38	97	44
WAIT	60 MHz device clock Relaxation oscillator on PLL powered on Processor core in WAIT state All peripheral modules enabled; TMRs and SCIs using 1X Clock ADC/DAC/comparator powered off	49	4.5	53	5.5
STOP	4 MHz device clock Relaxation oscillator on PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC/DAC/comparator powered off	8.0	3.6	9.2	4.9
STANDBY > STOP	100 kHz device clock Relaxation oscillator in standby mode PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC/DAC/comparator powered off Voltage regulator in standby mode	0.76	0	3.0	0
POWERDOWN	Device clock is off Relaxation oscillator powered off PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC /DAC/comparator powered off Voltage regulator in standby mode	0.66	0	2.0	0

1 No output switching
All ports configured as inputs
All inputs low
No DC loads

7.17 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 33. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration [3]	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 19
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

3 This minimum number guarantees that a reliable reset occurs.

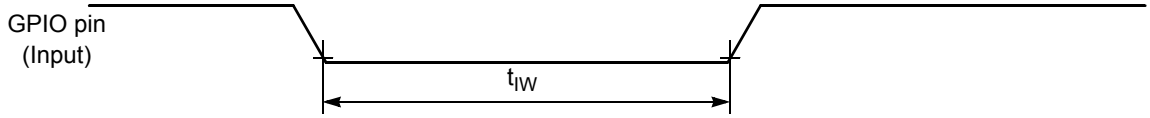


Figure 19. GPIO Interrupt Timing (Negative Edge-Sensitive)

7.18 Queued Serial Peripheral Interface (SPI) Timing

Table 34. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	Refer to
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 23
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 23
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 23

Table 34. SPI Timing[1] (continued)

Characteristic	Symbol	Min	Max	Unit	Refer to
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 23
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23

1 Parameters listed are guaranteed by design.

7.20 Freescale's Scalable Controller Area Network (MSCAN)

Table 36. MSCAN Timing

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs

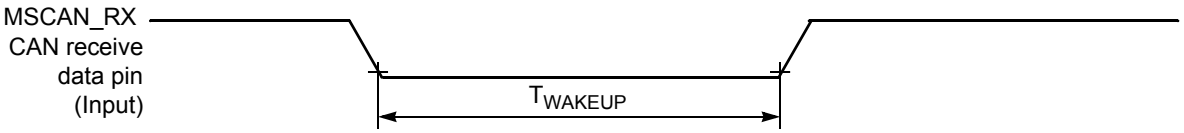


Figure 26. Bus Wake-up Detection

7.21 Inter-Integrated Circuit Interface (I^2C) Timing

Table 37. I^2C Timing

Characteristic	Symbol	Standard Mode		Unit
		Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	ns
Fall time of SDA and SCL signals	t_f	—	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	ns

1 The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2 The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3 A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

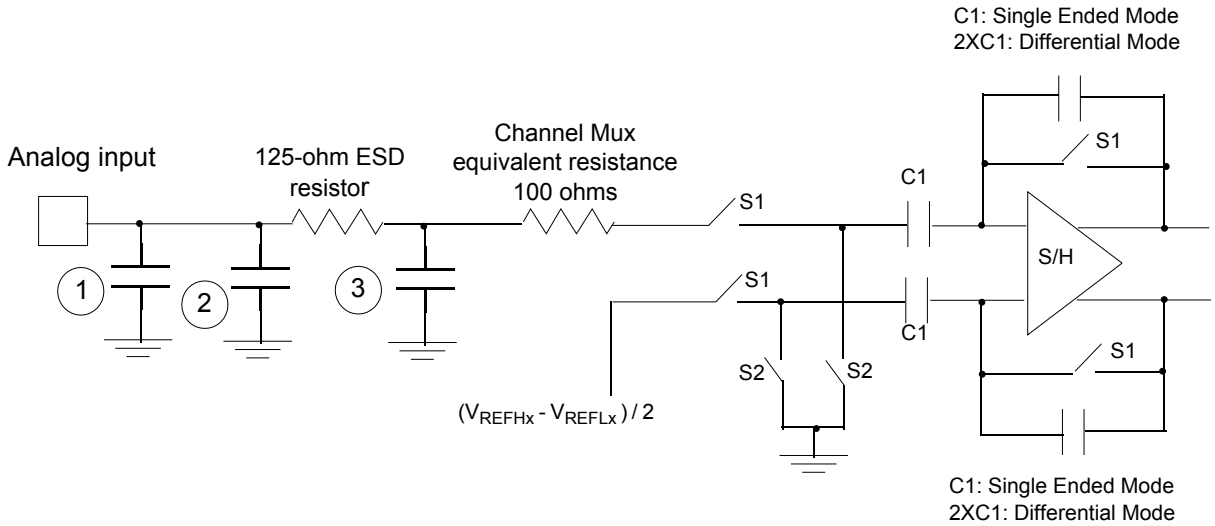
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.



1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

2. Parasitic capacitance due to the chip bond pad, ESD protection devices, and signal routing: 2.04 pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time: C_{gain} = 1.4 pF for x1 gain, 2.8 pF for x2 gain, and 5.6 pF for x4 gain.
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency.

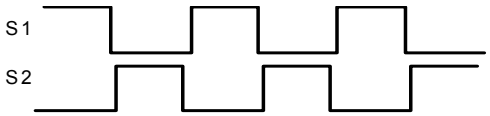


Figure 31. Equivalent Circuit for A/D Loading

7.26 Digital-to-Analog Converter (DAC) Parameters

Table 42. DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	—	12	bits
Settling time	At output load R_{LD} = 3 KΩ C_{LD} = 400 pf		TBD	—	2	µS
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µS
Accuracy						
Integral non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 8.0	LSB[2]
Differential non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 1.0	LSB[2]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+/- 40	mV
Gain error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- .5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{REFLX} or V_{REFHX}	V_{OUT}	V_{REFLX} +0.04V	—	V_{REFHX} - 0.04V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	TBD	—	dB
Spurious free dynamic range		SFDR	—	TBD	—	dB
Effective number of bits		ENOB	—	—	—	Bits

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These resources include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This component is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 45. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 45 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases, Equation 2 applies.

$$TotalPower = \Sigma((Intercept + Slope*C_{load})*frequency/10\ MHz) \quad \textit{Eqn. 2}$$

where:

— Summation is performed over all output pins with capacitive loads.

— Total power is expressed in mW.

— C_{load} is expressed in pF.

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static] component, reflects the effects of placing resistive loads on the outputs of the device. Total all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of nine PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasites associated with pure input pins is ignored and assumed to be negligible.

8 Design Considerations

8.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from Equation 3.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_A = Ambient temperature for the package (^oC)

$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which

Table 46. MC56F825x/MC56F824x Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number[1]
MC56F8245	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8245VLD MC56F8245MLD
MC56F8246	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8246VLF MC56F8246MLF
MC56F8247	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8247VLH MC56F8247MLH
MC56F8255	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8255VLD MC56F8255MLD
MC56F8256	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8256VLF MC56F8256MLF
MC56F8257	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8257VLH MC56F8257MLH

[1] All of the packages are RoHS compliant.