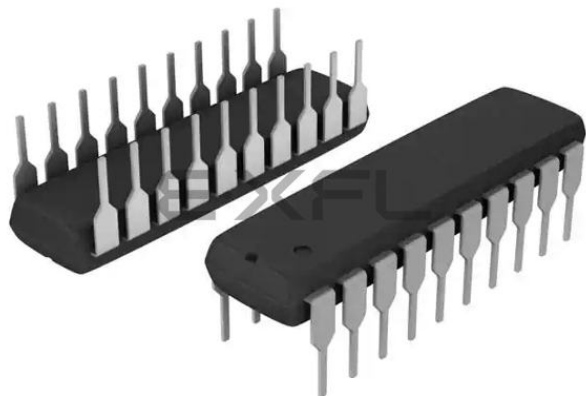




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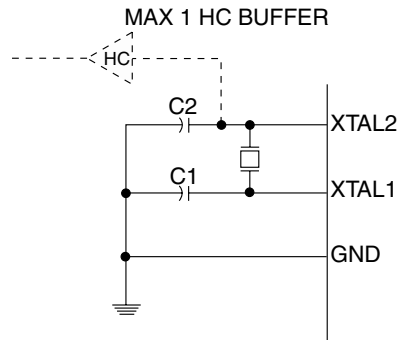
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

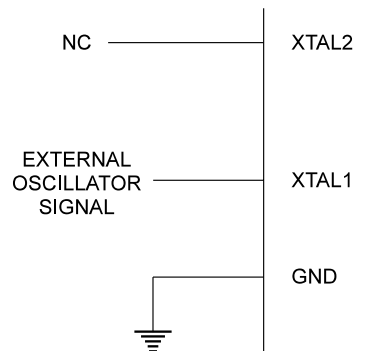
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	12MHz
Connectivity	SPI
Peripherals	POR, WDT
Number of I/O	15
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s1200-12pc

Figure 2. Oscillator Connections



Note: When using the MCU Oscillator as a clock for an external device, an HC buffer should be connected as indicated in the figure.

Figure 3. External Clock Drive Configuration



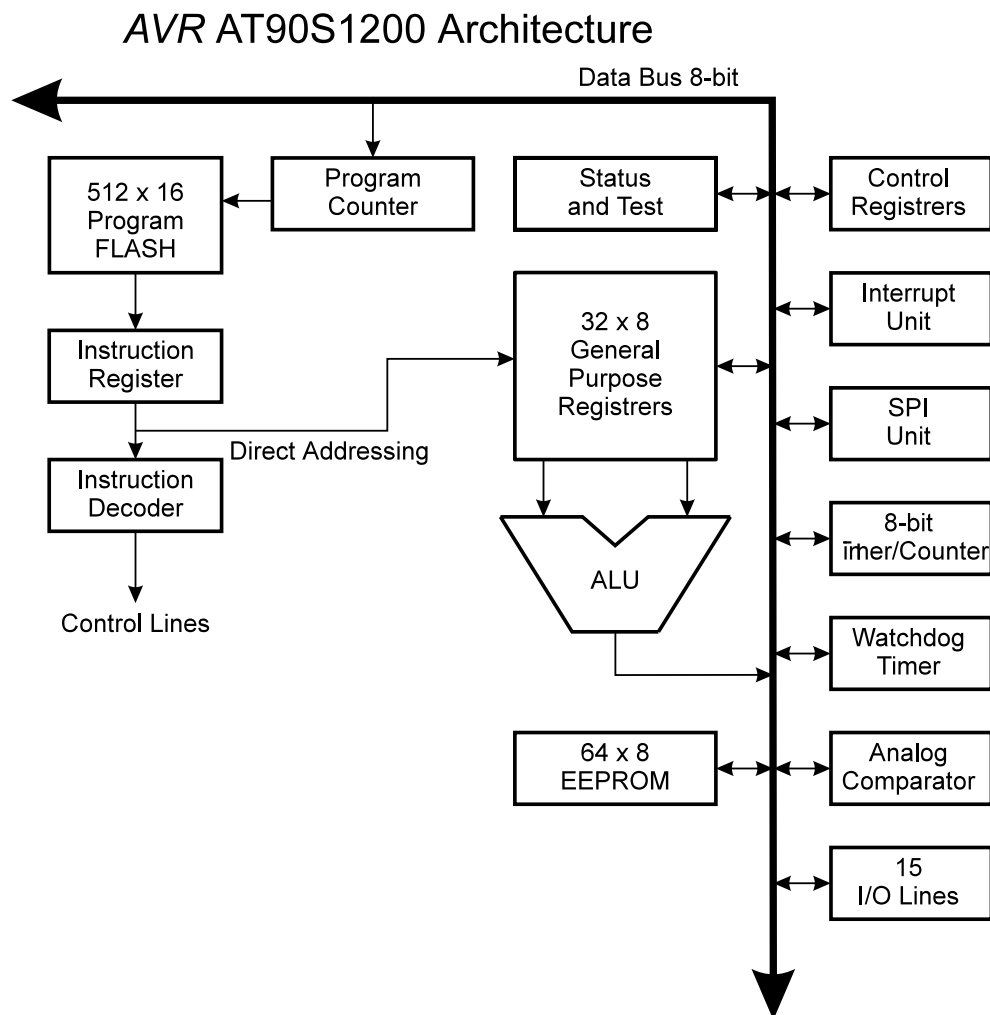
On-chip RC Oscillator

An On-chip RC Oscillator running at a fixed frequency of 1 MHz can be selected as the MCU clock source. If enabled, the AT90S1200 can operate with no external components. A control bit (RCEN) in the Flash Memory selects the On-chip RC Oscillator as the clock source when programmed ("0"). The AT90S1200 is normally shipped with this bit unprogrammed ("1"). Parts with this bit programmed can be ordered as AT90S1200A. The RCEN-bit can be changed by parallel programming only. When using the On-chip RC Oscillator for Serial Program downloading, the RCEN bit must be programmed in Parallel Programming mode first.

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Figure 4. The AT90S1200 AVR RISC Architecture



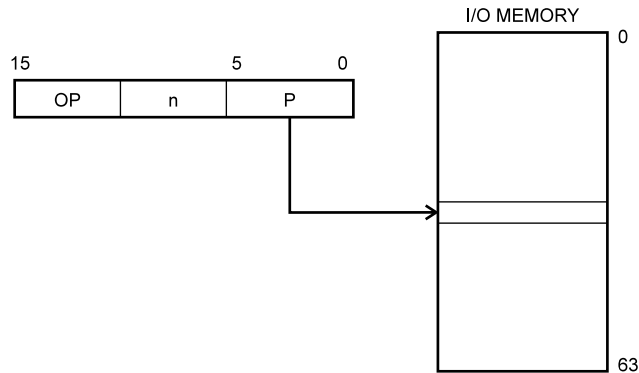
The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S1200 AVR RISC microcontroller architecture. The AVR uses a Harvard architecture concept – with separate memories and buses for program and data memories. The program memory is accessed with a 2-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and relative call instructions, the whole 512 address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

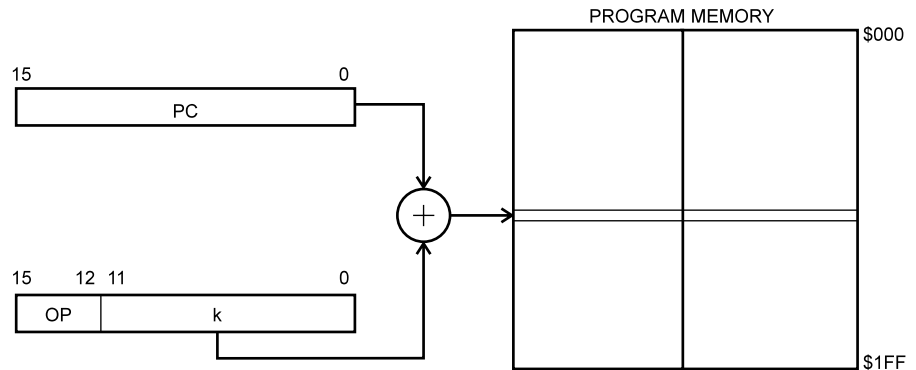
Figure 9. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

Relative Program Addressing, RJMP and RCALL

Figure 10. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

Subroutine and Interrupt Hardware Stack

The AT90S1200 uses a 3 level deep hardware stack for subroutines and interrupts. The hardware stack is 9 bits wide and stores the Program Counter (PC) return address while subroutines and interrupts are executed.

RCALL instructions and interrupts push the PC return address onto stack level 0, and the data in the other stack levels 1 - 2 are pushed one level deeper in the stack. When a RET or RETI instruction is executed the returning PC is fetched from stack level 0, and the data in the other stack levels 1 - 2 are popped one level in the stack.

If more than three subsequent subroutine calls or interrupts are executed, the first values written to the stack are overwritten.

Figure 13. Reset Logic

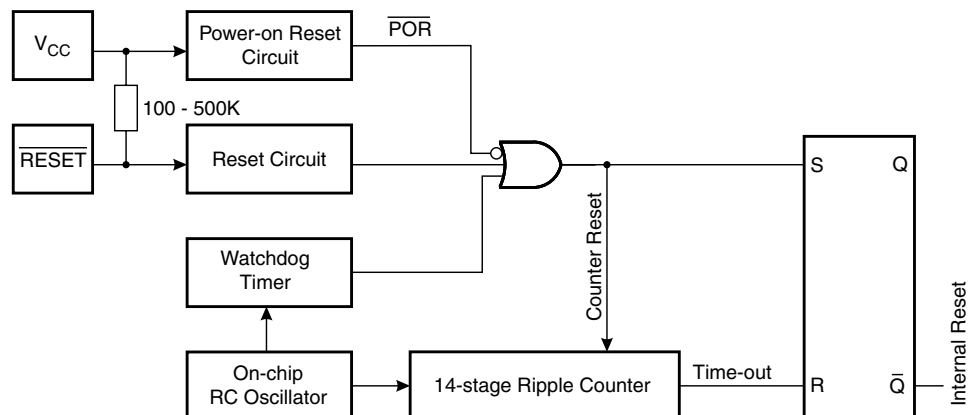


Table 3. Reset Characteristics ($V_{CC} = 5.0V$)

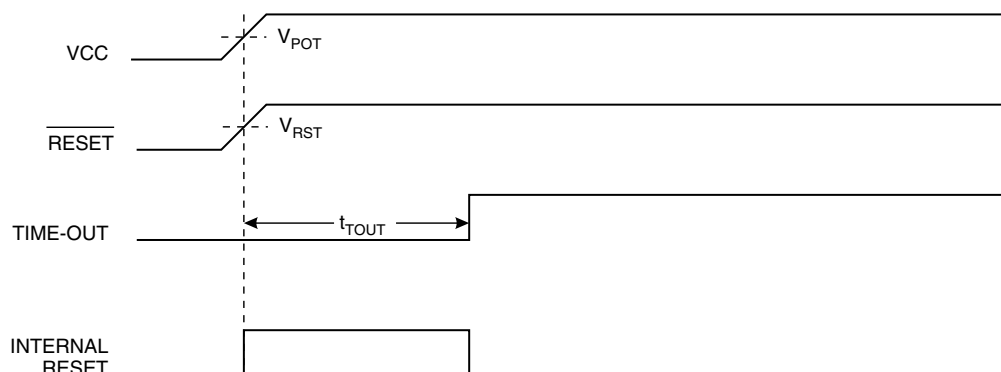
Symbol	Parameter	Min	Typ	Max	Units
$V_{POT}^{(1)}$	Power-on Reset Threshold Voltage (rising)	0.8	1.2	1.6	V
	Power-on Reset Threshold Voltage (falling)	0.2	0.4	0.6	V
V_{RST}	Pin Threshold Voltage	—	—	$0.85 V_{CC}$	V
t_{POR}	Power-on Reset Period	2.0	3.0	4.0	ms
t_{TOUT}	Reset Delay Time-out Period (The Time-out period equals 16K WDT cycles. See "Typical Characteristics" on page 51. for typical WDT frequency at different voltages).	11.0	16.0	21.0	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Power-on Reset

A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 13, an internal timer clocked from the Watchdog timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage (V_{POT}), regardless of the V_{CC} rise time (see Figure 14).

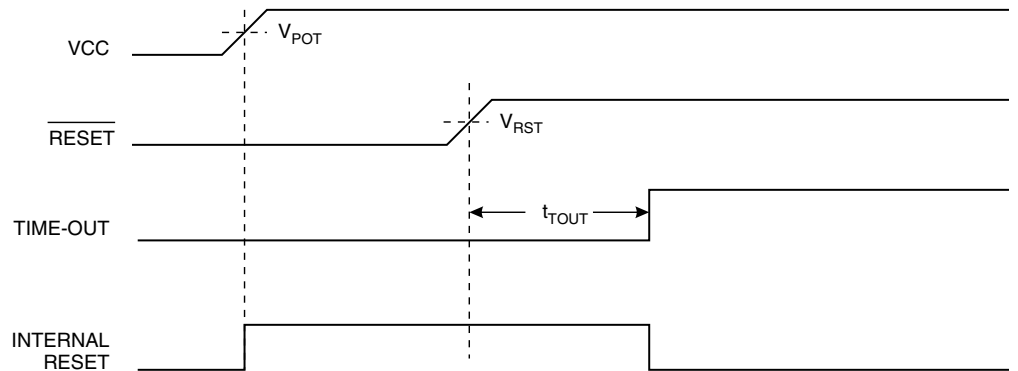
Figure 14. MCU Start-up, $\overline{RESET}$ Tied to V_{CC} .



If the built-in start-up delay is sufficient, $\overline{RESET}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the $\overline{RESET}$ pin low for a period after V_{CC} has

been applied, the Power-on Reset period can be extended. Refer to Figure 15 for a timing example on this.

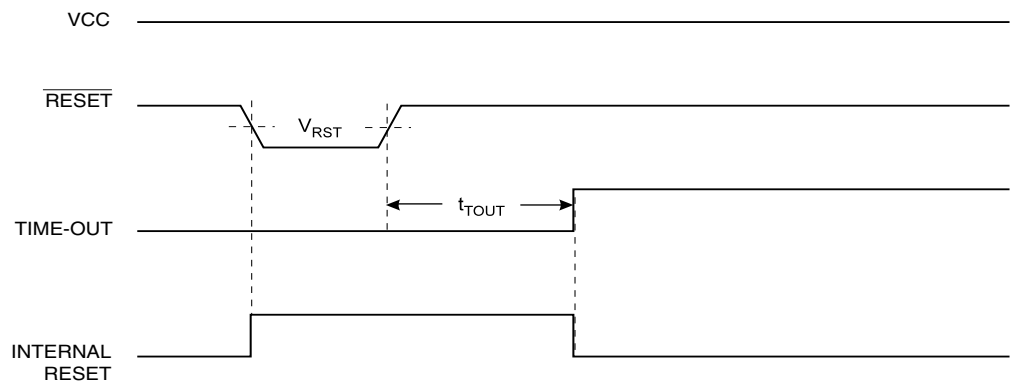
Figure 15. MCU Start-up, $\overline{\text{RESET}}$ Controlled Externally



External Reset

An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the delay timer starts the MCU after the Time-out period t_{TOUT} has expired.

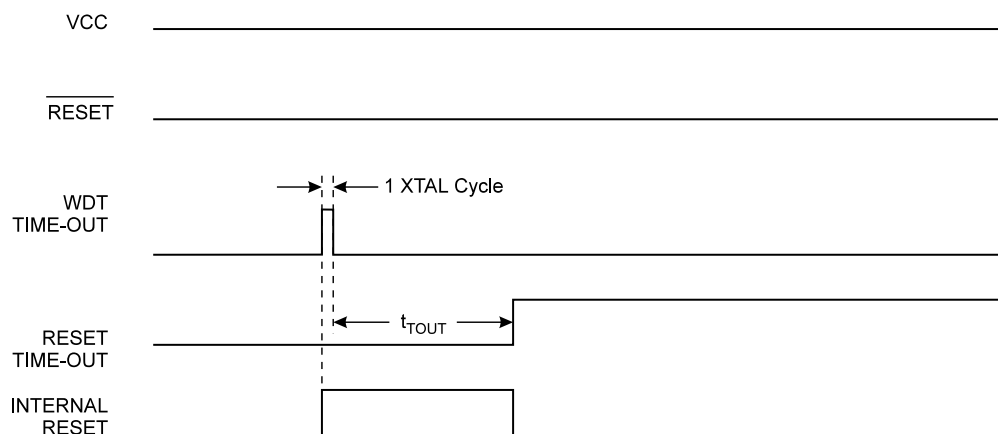
Figure 16. External Reset during Operation



Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT} . Refer to page 23 for details on operation of the Watchdog.

Figure 17. Watchdog Reset during Operation



Interrupt Handling

The AT90S1200 has two Interrupt Mask Control Registers: the GIMSK (General Interrupt Mask Register) at I/O space address \$3B and the TIMSK (Timer/Counter Interrupt Mask Register) at I/O address \$39.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the interrupt flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software.

If one or more interrupt conditions occur when the global interrupt enable bit is cleared (zero), the corresponding interrupt flag(s) will be set and remembered until the global interrupt enable bit is set (one), and will be executed by order of priority.

Note that external level interrupt does not have a flag, and will only be remembered for as long as the interrupt condition is active.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

General Interrupt Mask Register – GIMSK

Bit	7	6	5	4	3	2	1	0	
\$3B	-	INT0	-	-	-	-	-	-	GIMSK
Read/Write	R	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

• Bit 7 – Res: Reserved Bit

This bit is a reserved bit in the AT90S1200 and always reads as zero.

Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the register file and the I/O memory are unaltered. If a Reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction makes the MCU enter the Idle mode, stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and Watchdog Reset. If wakeup from the Analog Comparator interrupt is not required, the Analog Comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register (ACSR). This will reduce power consumption in Idle mode. When the MCU wakes up from Idle mode, the CPU starts program execution immediately.

Power-down Mode

When the SM bit is set (one), the SLEEP instruction makes the MCU enter Power-down mode. In this mode, the External Oscillator is stopped while the External Interrupts and the Watchdog (if enabled) continue operating. Only an External Reset, a Watchdog Reset (if enabled), an external level interrupt on INT0 can wake up the MCU.

Note that when a level triggered interrupt is used for wake-up from Power-down, the low level must be held for a time longer than the reset delay time-out period t_{TOUT} . Otherwise, the device will not wake up.

Port D

Three I/O memory address locations are allocated for Port D, one each for the Data Register – PORTD (\$12), Data Direction Register – DDRD (\$11), and the Port D Input Pins – PIND (\$10). The Port D Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

Port D has seven bi-directional I/O pins with internal pull-up resistors, PD6..PD0. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Some Port D pins have alternate functions as shown in Table 10.

Table 10. Port D Pin Alternate Functions

Port Pin	Alternate Function
PD2	INT0 (External Interrupt 0 input)
PD4	T0 (Timer/Counter 0 external input)

Port D Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
\$12	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port D Data Direction Register – DDRD

Bit	7	6	5	4	3	2	1	0	
\$11	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port D Input Pins Address – PIND

Bit	7	6	5	4	3	2	1	0	
\$10	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port D Input Pins address (PIND) is not a register, and this address enables access to the physical value on each Port D pin. When reading PORTD, the Port D Data Latch is read; and when reading PIND, the logical values present on the pins are read.

Port D as General Digital I/O

PDn, general I/O pin: The DDDn bit in the DDRD Register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PORTDn is set (one) when DDDn is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PORTDn bit has to be cleared (zero) or the pin has to be configured as an output pin. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Memory Programming

Program and Data Memory Lock Bits

The AT90S1200 MCU provides two Lock bits that can be left unprogrammed ("1") or can be programmed ("0") to obtain the additional features listed in Table 12. The Lock bits can only be erased with the Chip Erase command.

Table 12. Lock Bit Protection Modes

Memory Lock Bits			Protection Type
Mode	LB1	LB2	
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled. ⁽¹⁾
3	0	0	Same as mode 2, and verify is also disabled.

Note: 1. In Parallel mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

Fuse Bits

The AT90S1200 has two Fuse bits: SPIEN and RCEN.

- When the SPIEN Fuse bit is programmed ("0"), Serial Program Downloading is enabled. Default value is programmed ("0").
- When the RCEN Fuse bit is programmed ("0"), MCU clocking from the Internal RC Oscillator is selected. Default value is erased ("1"). Parts with this bit pre-programmed ("0") can be delivered on demand.
- The Fuse bits are not accessible in Serial Programming mode. The status of the Fuse bits is not affected by Chip Erase.

Signature Bytes

All Atmel microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both Serial and Parallel modes. The three bytes reside in a separate address space.

For the AT90S1200 they are:

1. \$00: \$1E (indicates manufactured by Atmel)
2. \$01: \$90 (indicates 1 Kb Flash memory)
3. \$02: \$01 (indicates AT90S1200 device when \$01 is \$90)

Note: When both Lock bits are programmed (lock mode 3), the signature bytes cannot be read in Serial mode. Reading the signature bytes will return: \$00, \$01 and \$02.

Programming the Flash and EEPROM

Atmel's AT90S1200 offers 1K byte of in-System Reprogrammable Flash program memory and 64 bytes of EEPROM data memory.

The AT90S1200 is normally shipped with the On-chip Flash program memory and EEPROM data memory arrays in the erased state (i.e., contents = \$FF) and ready to be programmed. This device supports a High-voltage (12V) Parallel Programming mode and a Low-voltage Serial Programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The Serial Programming mode provides a convenient way to download program and data into the AT90S1200 inside the user's system.

The program and data memory arrays on the AT90S1200 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided within

the self-timed write instruction in the Serial Programming mode. During programming, the supply voltage must be in accordance with Table 13.

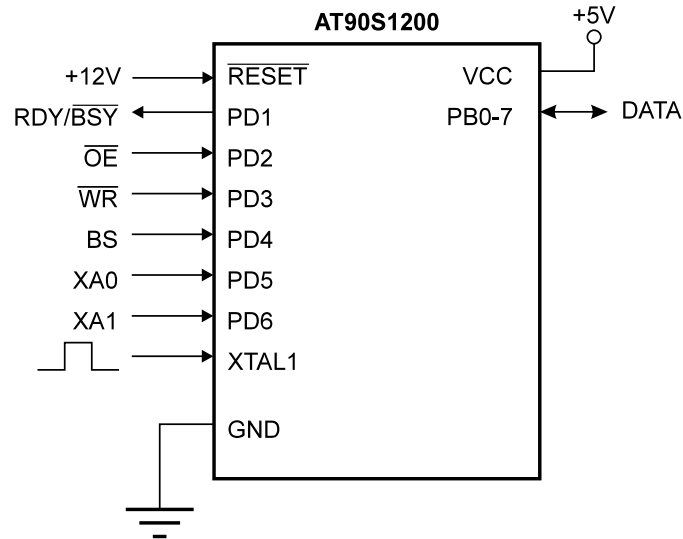
Table 13. Supply Voltage during Programming

Part	Serial Programming	Parallel Programming
AT90S1200	2.7 - 6.0V	4.5 - 5.5V

Parallel Programming

This section describes how to parallel program and verify Flash program memory, EEPROM data memory, Lock bits and Fuse bits in the AT90S1200.

Figure 30. Parallel Programming



Signal Names

In this section, some pins of the AT90S1200 are referenced by signal names describing their function during parallel programming rather than their pin names, see Figure 30 and Table 14. Pins not described in Table 14 are referenced by pin names.

The XA1/XA0 pins determines the action executed when the XTAL1 pin is given a positive pulse. The coding is shown in Table 15.

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The command is a byte where the different bits are assigned functions as shown in Table 16.

Table 14. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/BSY	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active low)
$\overline{WR}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PB0-7	I/O	Bi-directional Data Bus (Output when $\overline{OE}$ is low)

Table 15. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (High or low address byte for Flash determined by BS).
0	1	Load Data (High or low data byte for Flash determined by BS).
1	0	Load Command
1	1	No Action, Idle

Table 16. Command Byte Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Fuse and Lock Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in Parallel Programming mode:

1. Apply supply voltage according to Table 13, between V_{CC} and GND.
2. Set the $\overline{RESET}$ and BS pin to “0” and wait at least 100 ns.
3. Apply 11.5 - 12.5V to $\overline{RESET}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{RESET}$, will cause the device to fail entering Programming mode.

Chip Erase

The Chip Erase command will erase the Flash and EEPROM memories, and the Lock bits. The Lock bits are not Reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

Load Command “Chip Erase”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “1000 0000”. This is the command for Chip Erase.
4. Give XTAL1 a positive pulse. This loads the command.
5. Give $\overline{WR}$ a t_{WLWH_CE} wide negative pulse to execute Chip Erase, t_{WLWH_CE} is found in Table 17. Chip Erase does not generate any activity on the RDY/BSY pin.

Programming the Flash

A: Load Command “Write Flash”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “0001 0000”. This is the command for Write Flash.

4. Give XTAL1 a positive pulse. This loads the command.

B: Load Address High Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "1". This selects high byte.
3. Set DATA = Address high byte (\$00 - \$01).
4. Give XTAL1 a positive pulse. This loads the address high byte.

C: Load Address Low Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "0". This selects low byte.
3. Set DATA = Address low byte (\$00 - \$FF).
4. Give XTAL1 a positive pulse. This loads the address low byte.

D: Load Data Low Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data low byte (\$00 - \$FF).
3. Give XTAL1 a positive pulse. This loads the data low byte.

E: Write Data Low Byte

1. Set BS to "0". This selects low data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/ $\overline{BSY}$ goes low.
3. Wait until RDY/ $\overline{BSY}$ goes high to program the next byte.

(See Figure 31 for signal waveforms.)

F: Load Data High Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data high byte (\$00 - \$FF).
3. Give XTAL1 a positive pulse. This loads the data high byte.

G: Write Data High Byte

1. Set BS to "1". This selects high data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/ $\overline{BSY}$ goes low.
3. Wait until RDY/ $\overline{BSY}$ goes high to program the next byte.

(See Figure 32 for signal waveforms.)

The loaded command and address are retained in the device during programming. For efficient programming, the following should be considered:

- The command needs only be loaded once when writing or reading multiple memory locations.
- Address high byte needs only be loaded before programming a new 256-word page in the Flash.
- Skip writing the data value \$FF; that is, the contents of the entire Flash and EEPROM after a Chip Erase.

These considerations also apply to EEPROM programming and Flash, EEPROM and signature byte reading.

Figure 35. Serial Programming Waveforms

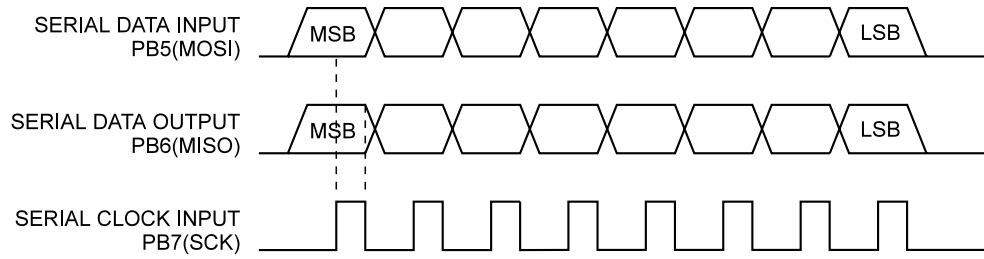


Table 19. Serial Programming Instruction Set for AT90S1200

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable serial programming while $\overline{\text{RESET}}$ is low.
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase both Flash and EEPROM memory arrays.
Read Program Memory	0010 H000	0000 000a	bbbb bbbb	oooo oooo	Read H (high or low) byte o from program memory at word address a:b.
Write Program Memory	0100 H000	0000 000a	bbbb bbbb	iiii iiii	Write H (high or low) byte i to program memory at word address a:b.
Read EEPROM Memory	1010 0000	0000 0000	00bb bbbb	oooo oooo	Read data o from EEPROM memory at address b.
Write EEPROM Memory	1100 0000	0000 0000	00bb bbbb	iiii iiii	Write data i to EEPROM memory at address b.
Write Lock Bits	1010 1100	1111 1211	xxxx xxxx	xxxx xxxx	Write Lock bits. Set bits 1,2 = "0" to program Lock bits.
Read Signature Byte	0011 0000	xxxx xxxx	xxxx xxbb	oooo oooo	Read signature byte o from address b. ⁽¹⁾

Note: a = address high bits, b = address low bits, H = 0 – Low byte, 1 – High byte, o = data out, i = data in, x = don't care, 1 = Lock Bit 1, 2 = Lock Bit 2

Note: 1. The signature bytes are not readable in lock mode 3 (i.e., both Lock bits programmed).

Serial Programming Characteristics

Figure 36. Serial Programming Timing

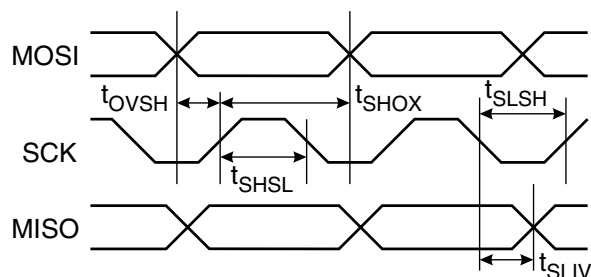


Table 20. Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.7 - 6.0\text{V}$ (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency ($V_{CC} = 2.7 - 4.0\text{V}$)	0		4.0	MHz
t_{CLCL}	Oscillator Period ($V_{CC} = 2.7 - 4.0\text{V}$)	250.0			ns
$1/t_{CLCL}$	Oscillator Frequency ($V_{CC} = 4.0 - 6.0\text{V}$)	0		12.0	MHz
t_{CLCL}	Oscillator Period ($V_{CC} = 4.0 - 6.0\text{V}$)	83.3			ns
t_{SHSL}	SCK Pulse Width High	$4.0 t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	$1.25 t_{CLCL}$			ns
t_{SHOX}	MOSI Hold after SCK High	$2.5 t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10.0	16.0	32.0	ns

Table 21. Minimum Wait Delay after the Chip Erase Instruction

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_ERASE}	18 ms	14 ms	12 ms	8 ms

Table 22. Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_PROG}	9 ms	7 ms	6 ms	4 ms

Figure 43. Idle Supply Current vs. V_{CC} , Device Clocked by Internal Oscillator

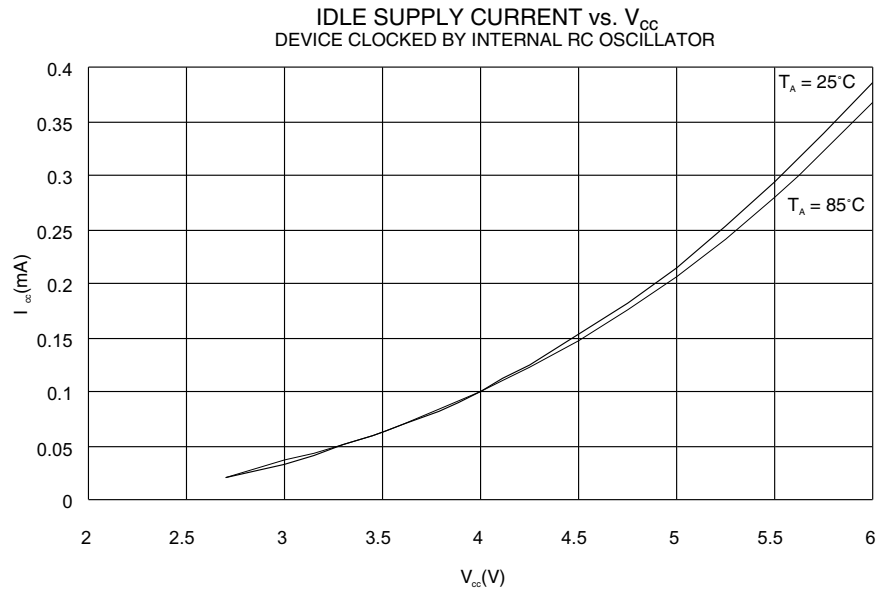


Figure 44. Power-down Supply Current vs. V_{CC} , Watchdog Timer Disabled

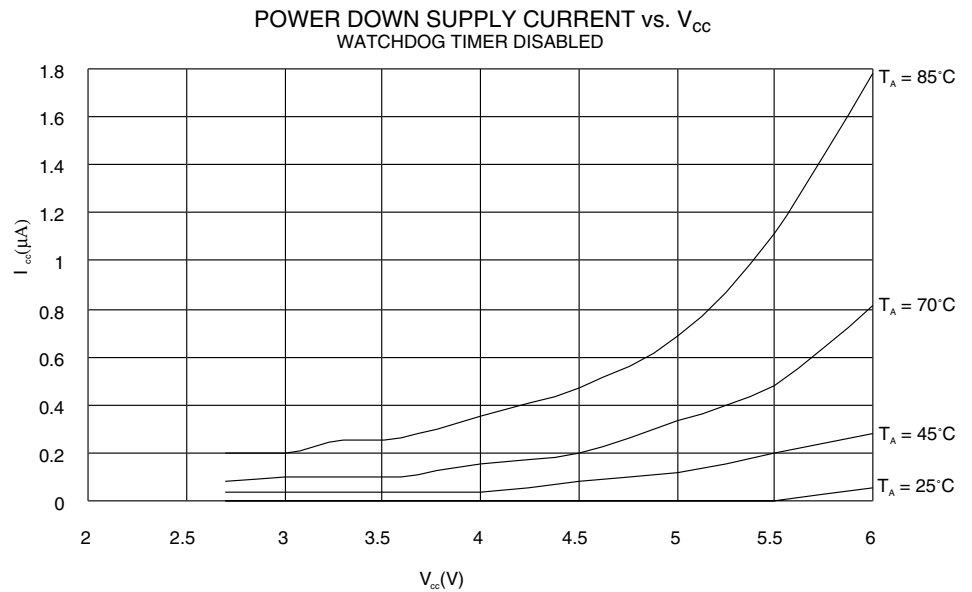


Figure 49. Analog Comparator Offset Voltage vs. Common Mode Voltage

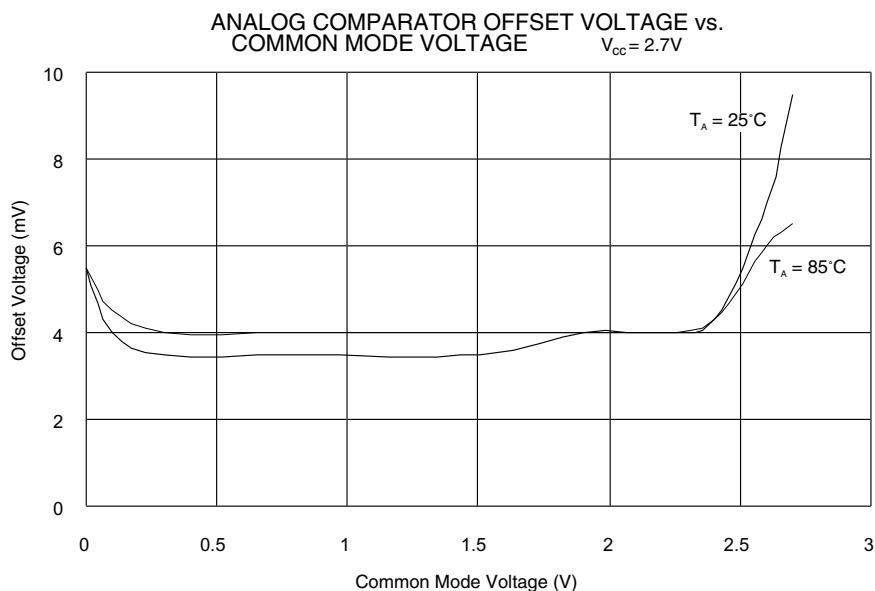
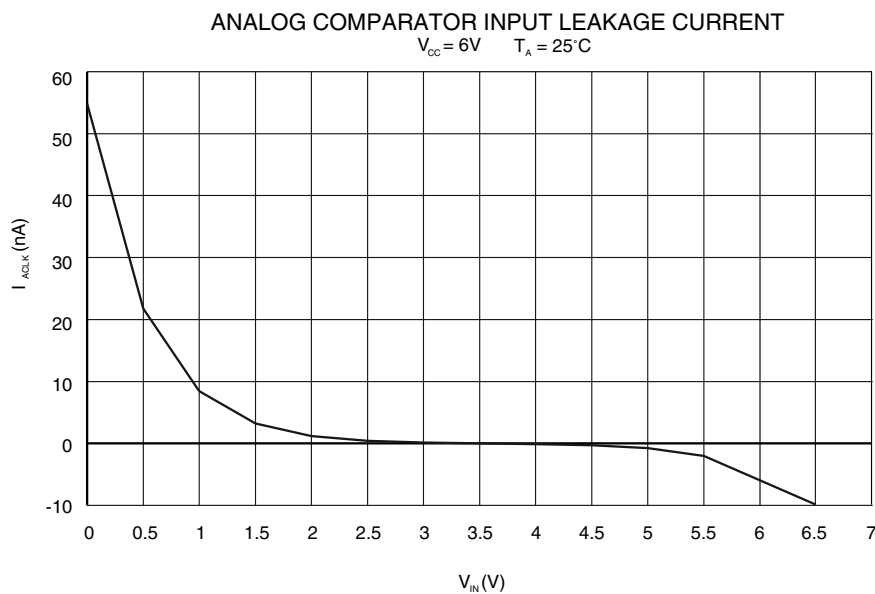


Figure 50. Analog Comparator Input Leakage Current



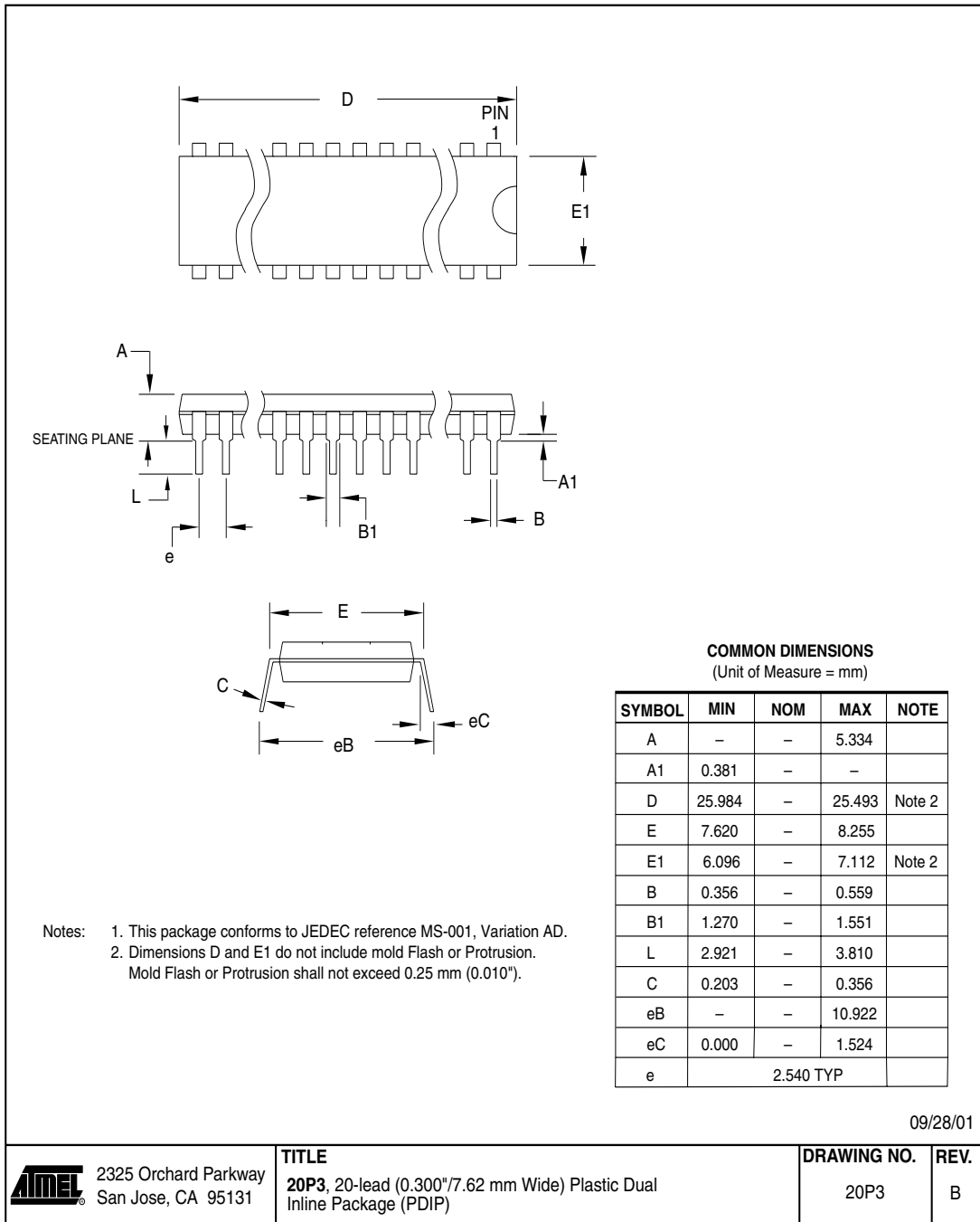
AT90S1200 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F	SREG	I	T	H	S	V	N	Z	C	page 11
\$3E	Reserved									
\$3D	Reserved									
\$3C	Reserved									
\$3B	GIMSK	-	INT0	-	-	-	-	-	-	page 15
\$3A	Reserved									
\$39	TIMSK	-	-	-	-	-	-	TOIE0	-	page 16
\$38	TIFR	-	-	-	-	-	-	TOV0	-	page 16
\$37	Reserved									
\$36	Reserved									
\$35	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00	page 18
\$34	Reserved									
\$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 21
\$32	TCNT0	Timer/Counter0 (8 Bits)								page 22
\$31	Reserved									
\$30	Reserved									
\$2F	Reserved									
\$2E	Reserved									
\$2D	Reserved									
\$2C	Reserved									
\$2B	Reserved									
\$2A	Reserved									
\$29	Reserved									
\$28	Reserved									
\$27	Reserved									
\$26	Reserved									
\$25	Reserved									
\$24	Reserved									
\$23	Reserved									
\$22	Reserved									
\$21	WDTCR	-	-	-	-	WDE	WDP2	WDP1	WDP0	page 23
\$20	Reserved									
\$1F	Reserved									
\$1E	EEAR	-	EEPROM Address Register							page 25
\$1D	EEDR	EEPROM Data Register								page 25
\$1C	EECR	-	-	-	-	-	-	EEWE	EERE	page 25
\$1B	Reserved									
\$1A	Reserved									
\$19	Reserved									
\$18	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 29
\$17	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 29
\$16	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 29
\$15	Reserved									
\$14	Reserved									
\$13	Reserved									
\$12	PORTD	-	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 34
\$11	DDRD	-	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 34
\$10	PIND	-	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 34
\$0F	Reserved									
...	Reserved									
\$09	Reserved									
\$08	ACSR	ACD	-	ACO	ACI	ACIE	-	ACIS1	ACIS0	page 27
...	Reserved									
\$00	Reserved									

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. Some of the status flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a "1" back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

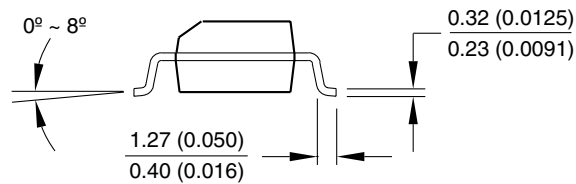
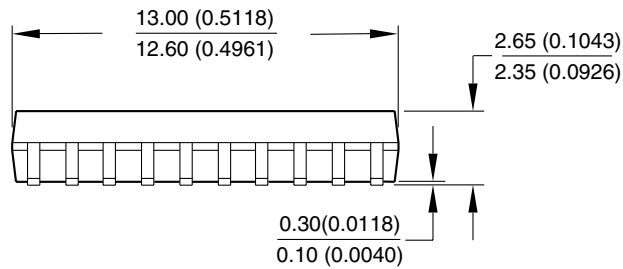
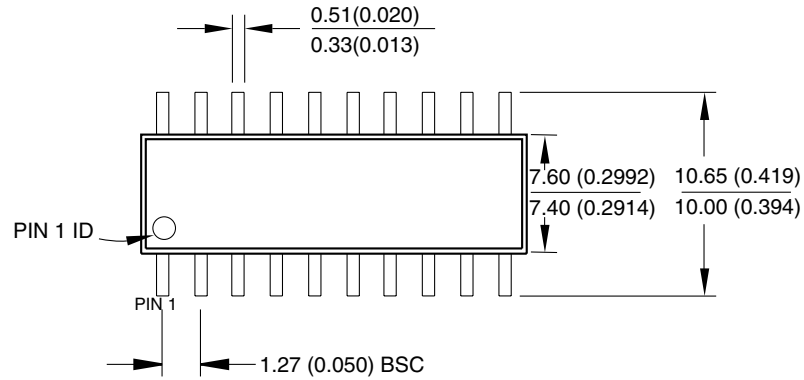
Packaging Information

20P3



20S

20S, 20-lead, Plastic Gull Wing Small
Outline (SOIC), 0.300" body.
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-013



*Controlling dimension: Inches

REV. A 04/11/2001



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