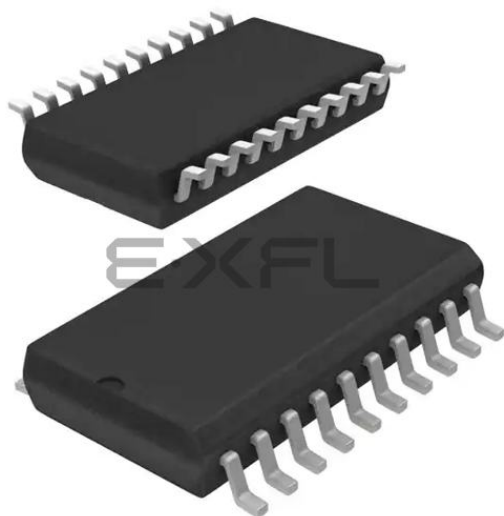




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI
Peripherals	POR, WDT
Number of I/O	15
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s1200-4sc

ing the Registers, Timer/Counter, Watchdog and Interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or hardware Reset.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip In-System Programmable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S1200 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

The AT90S1200 AVR is supported with a full suite of program and system development tools including: macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

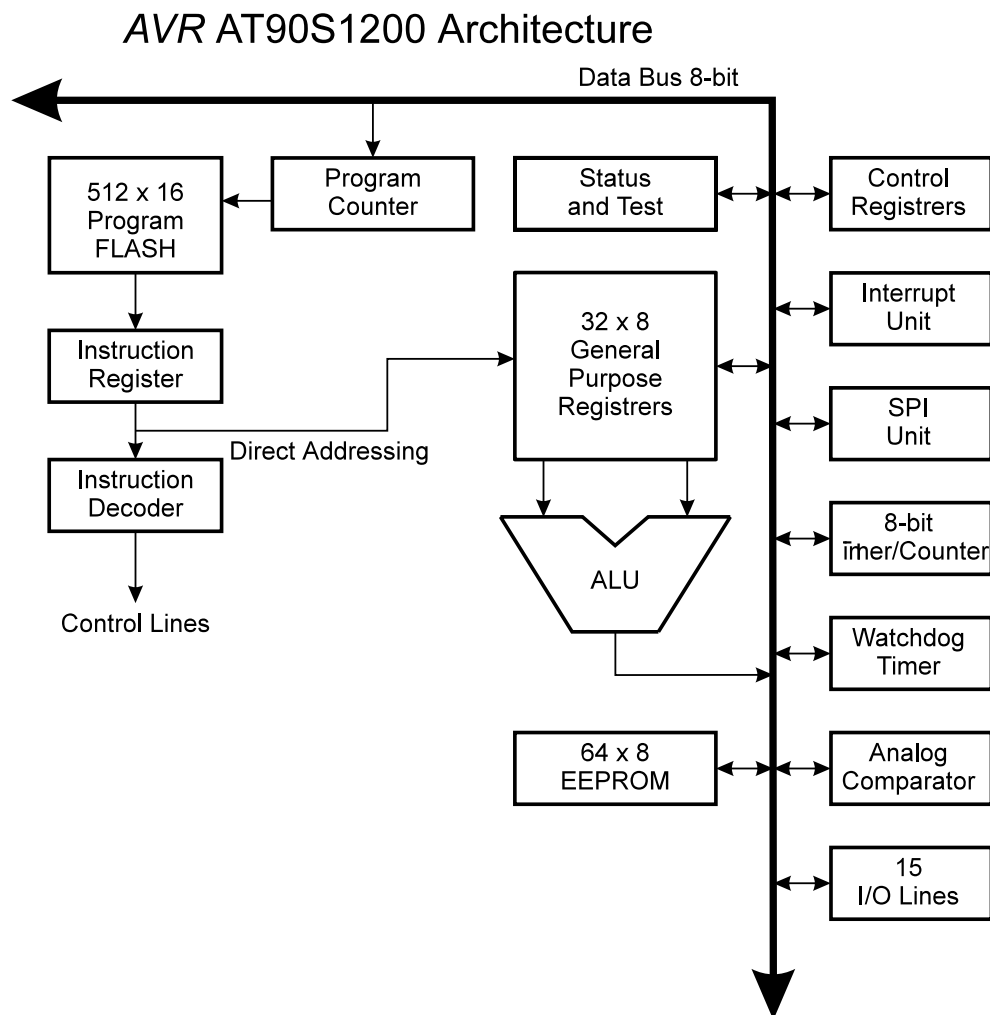
Pin Descriptions

VCC	Supply voltage pin.
GND	Ground pin.
Port B (PB7..PB0)	Port B is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). PB0 and PB1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the On-chip Analog Comparator. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active. Port B also serves the functions of various special features of the AT90S1200 as listed on page 30.
Port D (PD6..PD0)	Port D has seven bi-directional I/O pins with internal pull-up resistors, PD6..PD0. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active. Port D also serves the functions of various special features of the AT90S1200 as listed on page 34.
<u>RESET</u>	Reset input. A low level on this pin for more than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.
XTAL1	Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
XTAL2	Output from the inverting oscillator amplifier.
Crystal Oscillator	XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator, as shown in Figure 2. Either a quartz crystal or a ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 3.

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Figure 4. The AT90S1200 AVR RISC Architecture



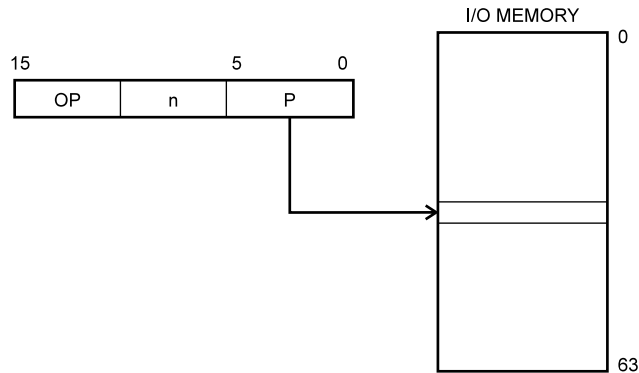
The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S1200 AVR RISC microcontroller architecture. The AVR uses a Harvard architecture concept – with separate memories and buses for program and data memories. The program memory is accessed with a 2-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and relative call instructions, the whole 512 address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

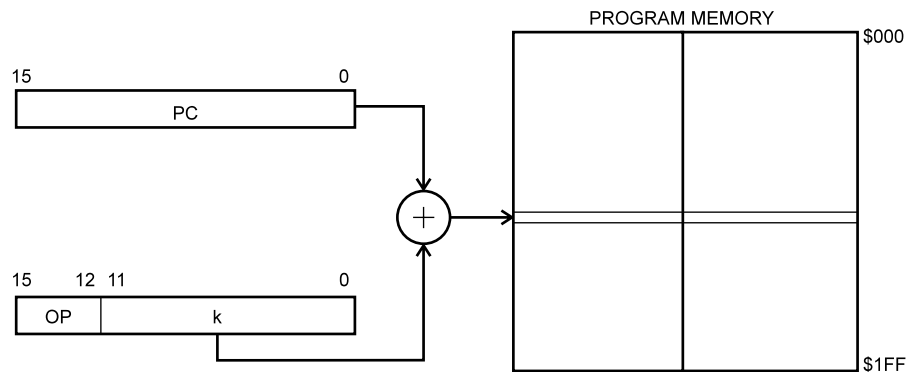
Figure 9. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

Relative Program Addressing, RJMP and RCALL

Figure 10. Relative Program Memory Addressing



Program execution continues at address $PC + k + 1$. The relative address k is -2048 to 2047.

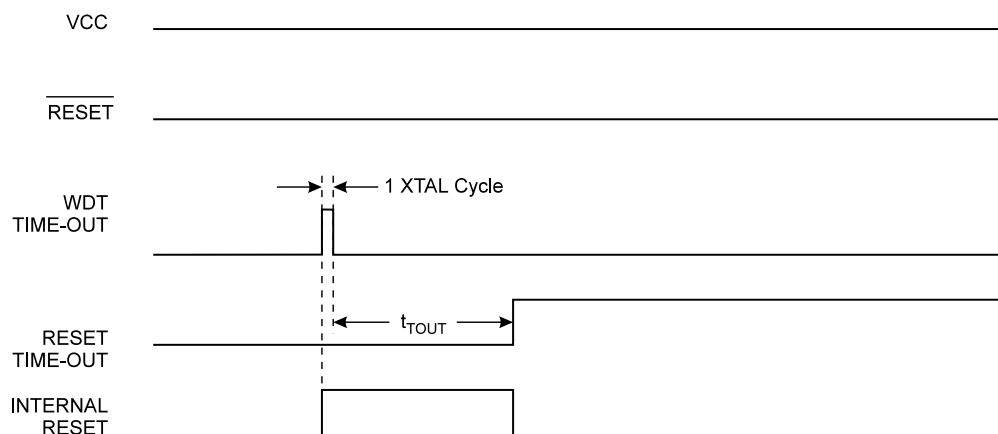
Subroutine and Interrupt Hardware Stack

The AT90S1200 uses a 3 level deep hardware stack for subroutines and interrupts. The hardware stack is 9 bits wide and stores the Program Counter (PC) return address while subroutines and interrupts are executed.

RCALL instructions and interrupts push the PC return address onto stack level 0, and the data in the other stack levels 1 - 2 are pushed one level deeper in the stack. When a RET or RETI instruction is executed the returning PC is fetched from stack level 0, and the data in the other stack levels 1 - 2 are popped one level in the stack.

If more than three subsequent subroutine calls or interrupts are executed, the first values written to the stack are overwritten.

Figure 17. Watchdog Reset during Operation



Interrupt Handling

The AT90S1200 has two Interrupt Mask Control Registers: the GIMSK (General Interrupt Mask Register) at I/O space address \$3B and the TIMSK (Timer/Counter Interrupt Mask Register) at I/O address \$39.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the interrupt flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software.

If one or more interrupt conditions occur when the global interrupt enable bit is cleared (zero), the corresponding interrupt flag(s) will be set and remembered until the global interrupt enable bit is set (one), and will be executed by order of priority.

Note that external level interrupt does not have a flag, and will only be remembered for as long as the interrupt condition is active.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

General Interrupt Mask Register – GIMSK

Bit	7	6	5	4	3	2	1	0	
\$3B	-	INT0	-	-	-	-	-	-	GIMSK
Read/Write	R	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

• Bit 7 – Res: Reserved Bit

This bit is a reserved bit in the AT90S1200 and always reads as zero.

- **Bits 2, 1, 0 – CS02, CS01, CS00: Clock Select0, Bits 2, 1 and 0**

The Clock Select0 bits 2, 1 and 0 define the prescaling source of Timer/Counter0.

Table 5. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, the Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK Oscillator clock. If the external pin modes are used for Timer/Counter0, transitions on PD4/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user SW control of the counting.

Timer/Counter0 – TCNT0

Bit	7	6	5	4	3	2	1	0	
\$32	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the timer clock cycle following the write operation.

- **Bit 3 – ACIE: Analog Comparator Interrupt Enable**

When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the Analog Comparator Interrupt is activated. When cleared (zero), the interrupt is disabled.

- **Bit 2 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S1200 and will always read as zero.

- **Bits 1, 0 – ACIS1, ACIS0: Analog Comparator Interrupt Mode Select**

These bits determine which comparator events trigger the Analog Comparator Interrupt. The different settings are shown in Table 7.

Table 7. ACIS1/ACIS0 Settings

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

Note: When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR register. Otherwise, an interrupt can occur when the bits are changed.

Port B as General Digital I/O

All eight pins in Port B have equal functionality when used as digital I/O pins.

PB_n, General I/O pin: The DDB_n bit in the DDRB Register selects the direction of this pin, if DDB_n is set (one), PB_n is configured as an output pin. If DDB_n is cleared (zero), PB_n is configured as an input pin. If PORTB_n is set (one) and the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, PORTB_n has to be cleared (zero) or the pin has to be configured as an output pin. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Table 9. DDB_n Effect on Port B Pins

DDB _n	PORTB _n	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (High-Z)
0	1	Input	Yes	PB _n will source current if ext. pulled low.
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7,6...0, pin number.

Alternate Functions of Port B

The alternate pin functions of Port B are:

- **SCK – Port B, Bit 7**

SCK, Clock Input pin for memory up/downloading.

- **MISO – Port B, Bit 6**

MISO, Data Output pin for memory uploading.

- **MOSI – Port B, Bit 5**

MOSI, Data Input pin for memory downloading.

- **AIN1 – Port B, Bit 1**

AIN1, Analog Comparator Negative Input. When configured as an input (DDB1 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB1 is cleared [zero]), this pin also serves as the negative input of the On-chip Analog Comparator.

- **AIN0 – Port B, Bit 0**

AIN0, Analog Comparator Positive Input. When configured as an input (DDB0 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB0 is cleared [zero]), this pin also serves as the positive input of the On-chip Analog Comparator.

Figure 35. Serial Programming Waveforms

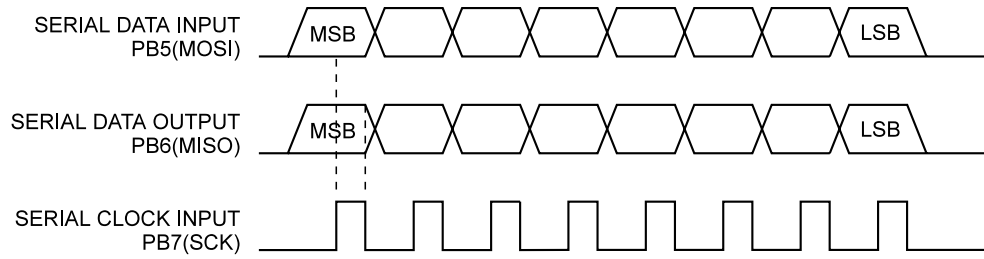


Table 19. Serial Programming Instruction Set for AT90S1200

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable serial programming while $\overline{\text{RESET}}$ is low.
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase both Flash and EEPROM memory arrays.
Read Program Memory	0010 H000	0000 000a	bbbb bbbb	oooo oooo	Read H (high or low) byte o from program memory at word address a:b.
Write Program Memory	0100 H000	0000 000a	bbbb bbbb	iiii iiii	Write H (high or low) byte i to program memory at word address a:b.
Read EEPROM Memory	1010 0000	0000 0000	00bb bbbb	oooo oooo	Read data o from EEPROM memory at address b.
Write EEPROM Memory	1100 0000	0000 0000	00bb bbbb	iiii iiii	Write data i to EEPROM memory at address b.
Write Lock Bits	1010 1100	1111 1211	xxxx xxxx	xxxx xxxx	Write Lock bits. Set bits 1,2 = "0" to program Lock bits.
Read Signature Byte	0011 0000	xxxx xxxx	xxxx xxbb	oooo oooo	Read signature byte o from address b. ⁽¹⁾

Note: a = address high bits, b = address low bits, H = 0 – Low byte, 1 – High byte, o = data out, i = data in, x = don't care, 1 = Lock Bit 1, 2 = Lock Bit 2

Note: 1. The signature bytes are not readable in lock mode 3 (i.e., both Lock bits programmed).

DC Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.7\text{V}$ to 6.0V (unless otherwise noted) (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ACIO}	Analog Comparator Input Offset Voltage	$V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$			40.0	mV
I_{ACLK}	Analog Comparator Input Leakage Current	$V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$	-50.0		50.0	nA
t_{ACPD}	Analog Comparator Propagation Delay	$V_{CC} = 2.7\text{V}$ $V_{CC} = 4.0\text{V}$		750.0 500.0		ns

- Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low.
 2. "Min" means the lowest value where the pin is guaranteed to be read as high.
 3. Although each I/O port can sink more than the test conditions (20 mA at $V_{CC} = 5\text{V}$, 10 mA at $V_{CC} = 3\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1] The sum of all I_{OL} for all ports, should not exceed 200 mA.
 - 2] The sum of all I_{OL} for port D0 - D5 and XTAL2, should not exceed 100 mA.
 - 3] The sum of all I_{OL} for ports B0 - B7 and D6, should not exceed 100 mA.
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
 4. Although each I/O port can source more than the test conditions (3 mA at $V_{CC} = 5\text{V}$, 1.5 mA at $V_{CC} = 3\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1] The sum of all I_{OH} for all ports, should not exceed 200 mA.
 - 2] The sum of all I_{OH} for port D0 - D5 and XTAL2, should not exceed 100 mA.
 - 3] The sum of all I_{OH} for ports B0 - B7 and D6, should not exceed 100 mA.
 If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
 5. Minimum V_{CC} for power-down is 2V.

Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

The power consumption in Power-down mode is independent of clock selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L \cdot V_{CC} \cdot f$ where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

Figure 38. Active Supply Current vs. Frequency

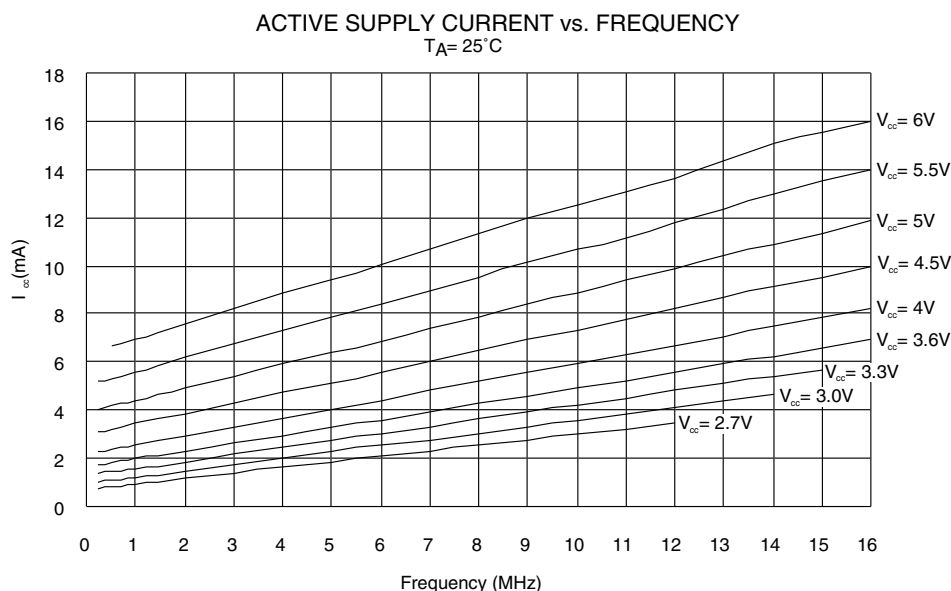


Figure 39. Active Supply Current vs. V_{CC}

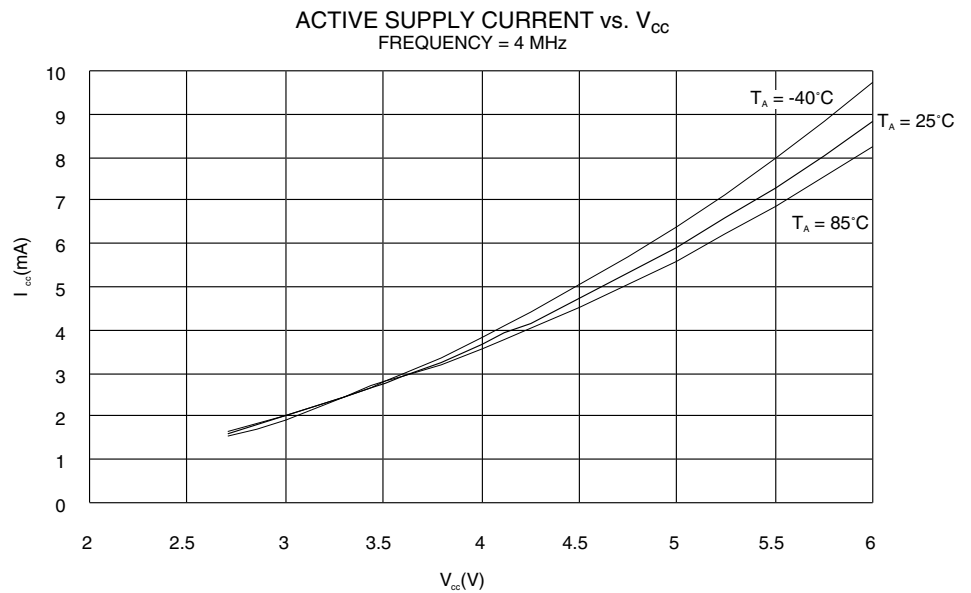


Figure 40. Active Supply Current vs. V_{CC} , Device Clocked by Internal Oscillator

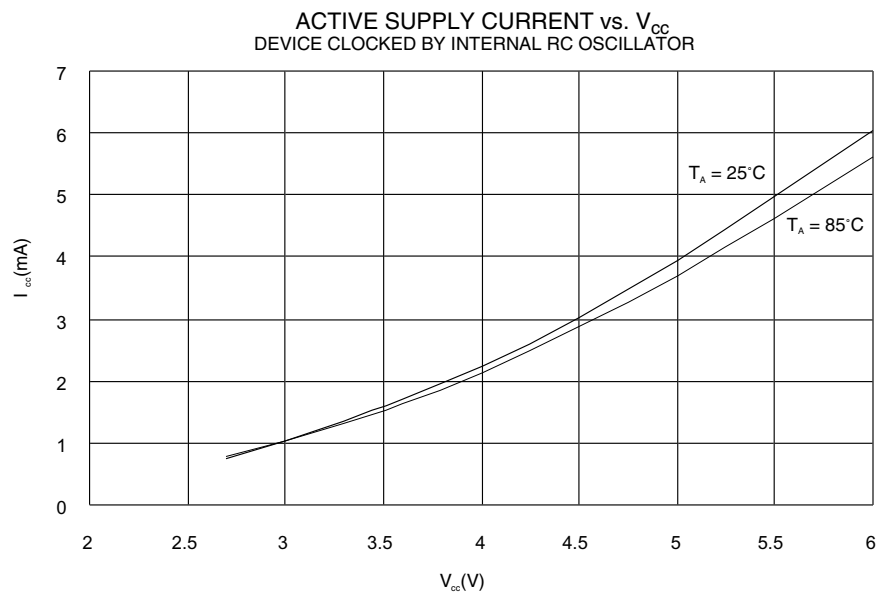


Figure 41. Idle Supply Current vs. Frequency

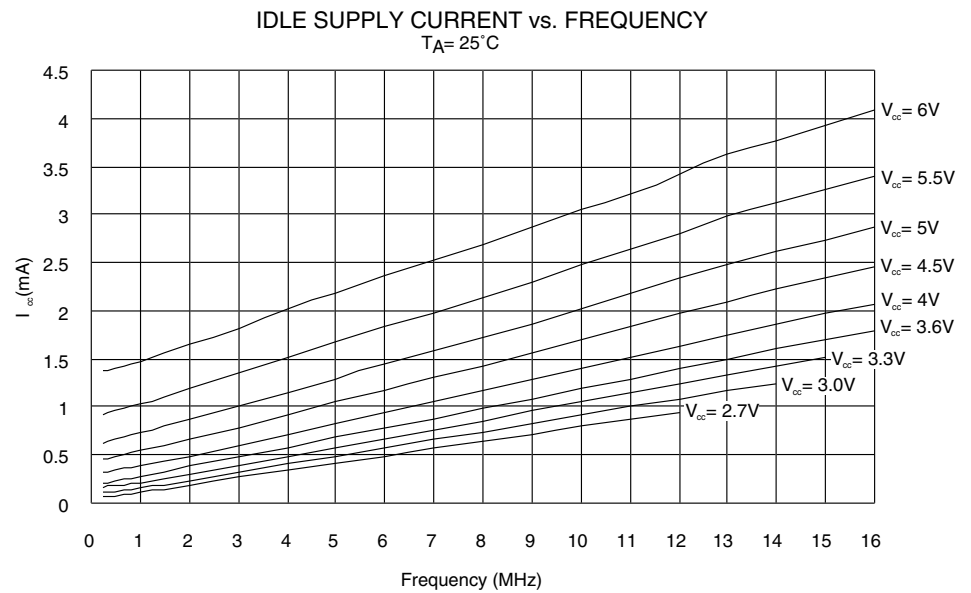


Figure 42. Idle Supply Current vs. V_{CC}

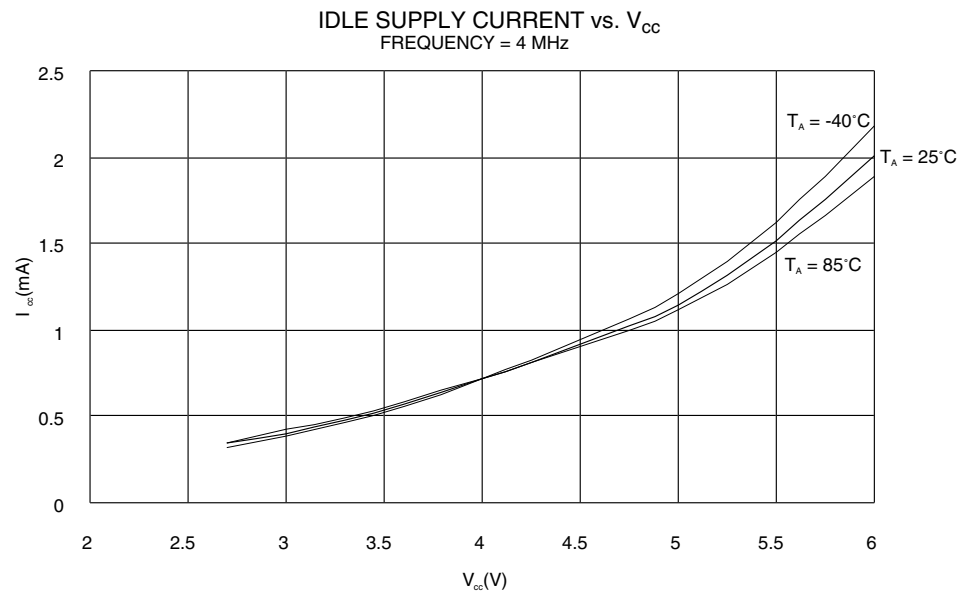


Figure 55. I/O Pin Sink Current vs. Output Voltage

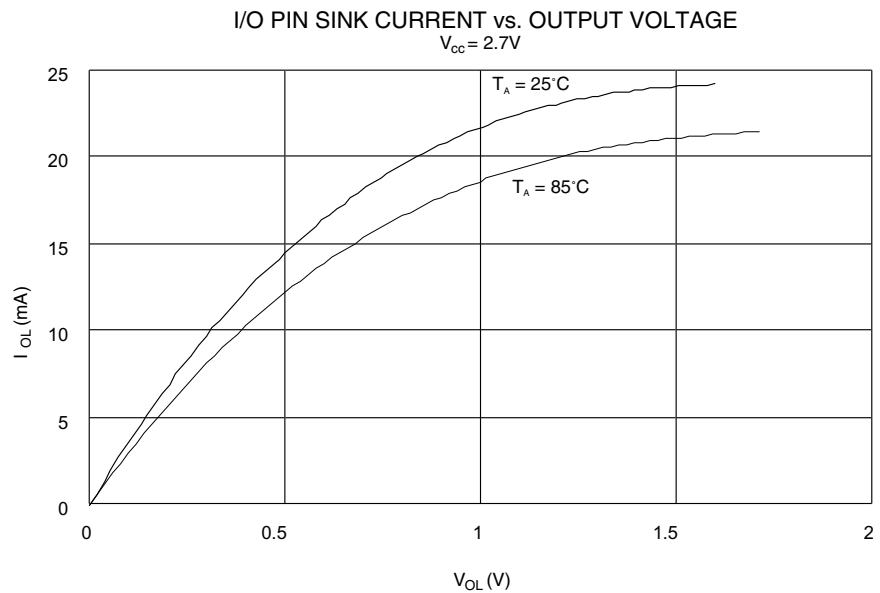
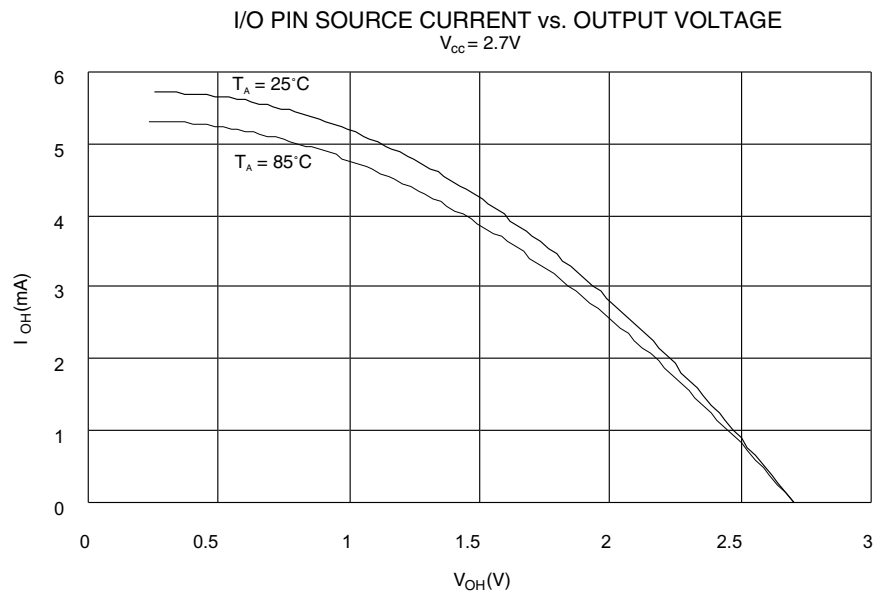


Figure 56. I/O Pin Source Current vs. Output Voltage



Note: Input threshold is measured at the center point of the hysteresis.

Figure 57. I/O Pin Input Threshold Voltage vs. V_{CC}

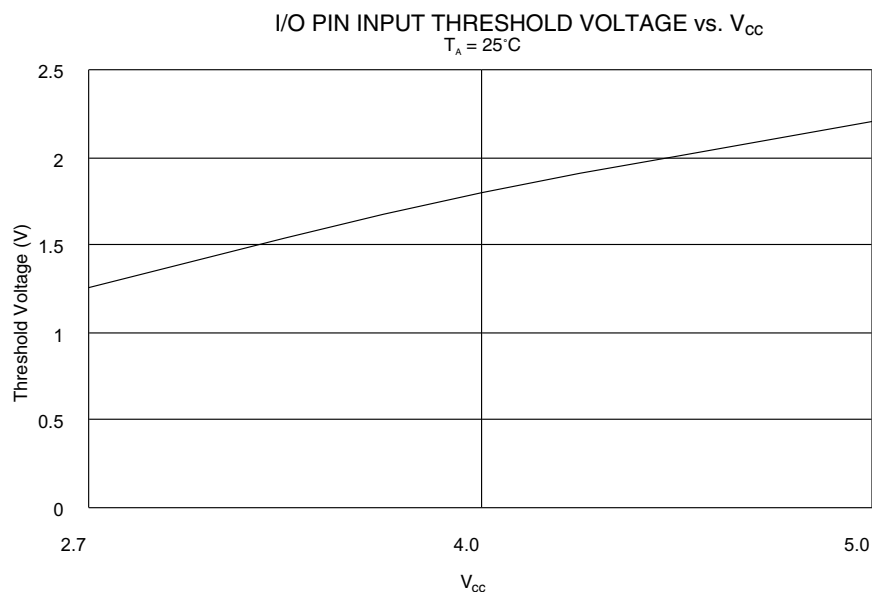
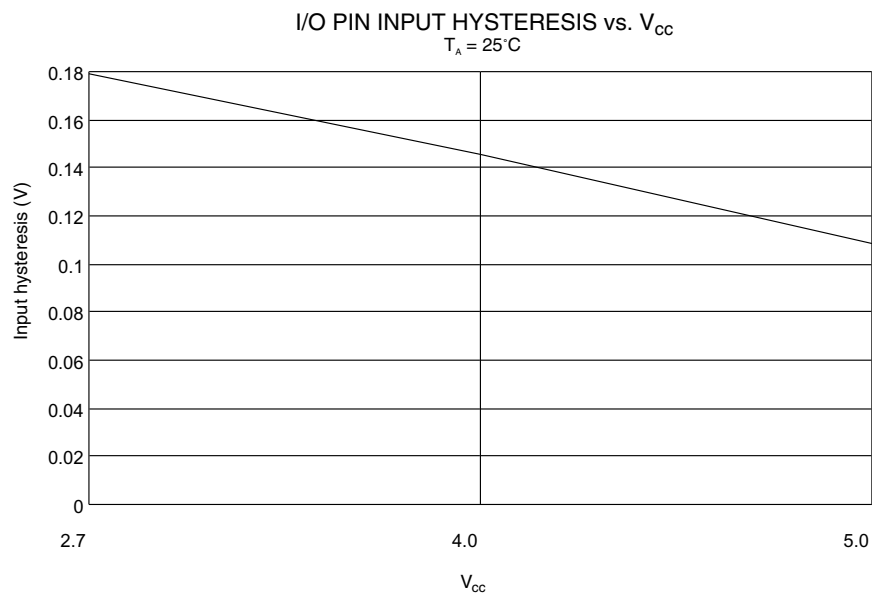


Figure 58. I/O Pin Input Hysteresis vs. V_{CC}



AT90S1200 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F	SREG	I	T	H	S	V	N	Z	C	page 11
\$3E	Reserved									
\$3D	Reserved									
\$3C	Reserved									
\$3B	GIMSK	-	INT0	-	-	-	-	-	-	page 15
\$3A	Reserved									
\$39	TIMSK	-	-	-	-	-	-	TOIE0	-	page 16
\$38	TIFR	-	-	-	-	-	-	TOV0	-	page 16
\$37	Reserved									
\$36	Reserved									
\$35	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00	page 18
\$34	Reserved									
\$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 21
\$32	TCNT0	Timer/Counter0 (8 Bits)								page 22
\$31	Reserved									
\$30	Reserved									
\$2F	Reserved									
\$2E	Reserved									
\$2D	Reserved									
\$2C	Reserved									
\$2B	Reserved									
\$2A	Reserved									
\$29	Reserved									
\$28	Reserved									
\$27	Reserved									
\$26	Reserved									
\$25	Reserved									
\$24	Reserved									
\$23	Reserved									
\$22	Reserved									
\$21	WDTCR	-	-	-	-	WDE	WDP2	WDP1	WDP0	page 23
\$20	Reserved									
\$1F	Reserved									
\$1E	EEAR	-	EEPROM Address Register							page 25
\$1D	EEDR	EEPROM Data Register								page 25
\$1C	EECR	-	-	-	-	-	-	EEWE	EERE	page 25
\$1B	Reserved									
\$1A	Reserved									
\$19	Reserved									
\$18	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 29
\$17	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 29
\$16	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 29
\$15	Reserved									
\$14	Reserved									
\$13	Reserved									
\$12	PORTD	-	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 34
\$11	DDRD	-	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 34
\$10	PIND	-	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 34
\$0F	Reserved									
...	Reserved									
\$09	Reserved									
\$08	ACSR	ACD	-	ACO	ACI	ACIE	-	ACIS1	ACIS0	page 27
...	Reserved									
\$00	Reserved									

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. Some of the status flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a "1" back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

Instruction Set Summary

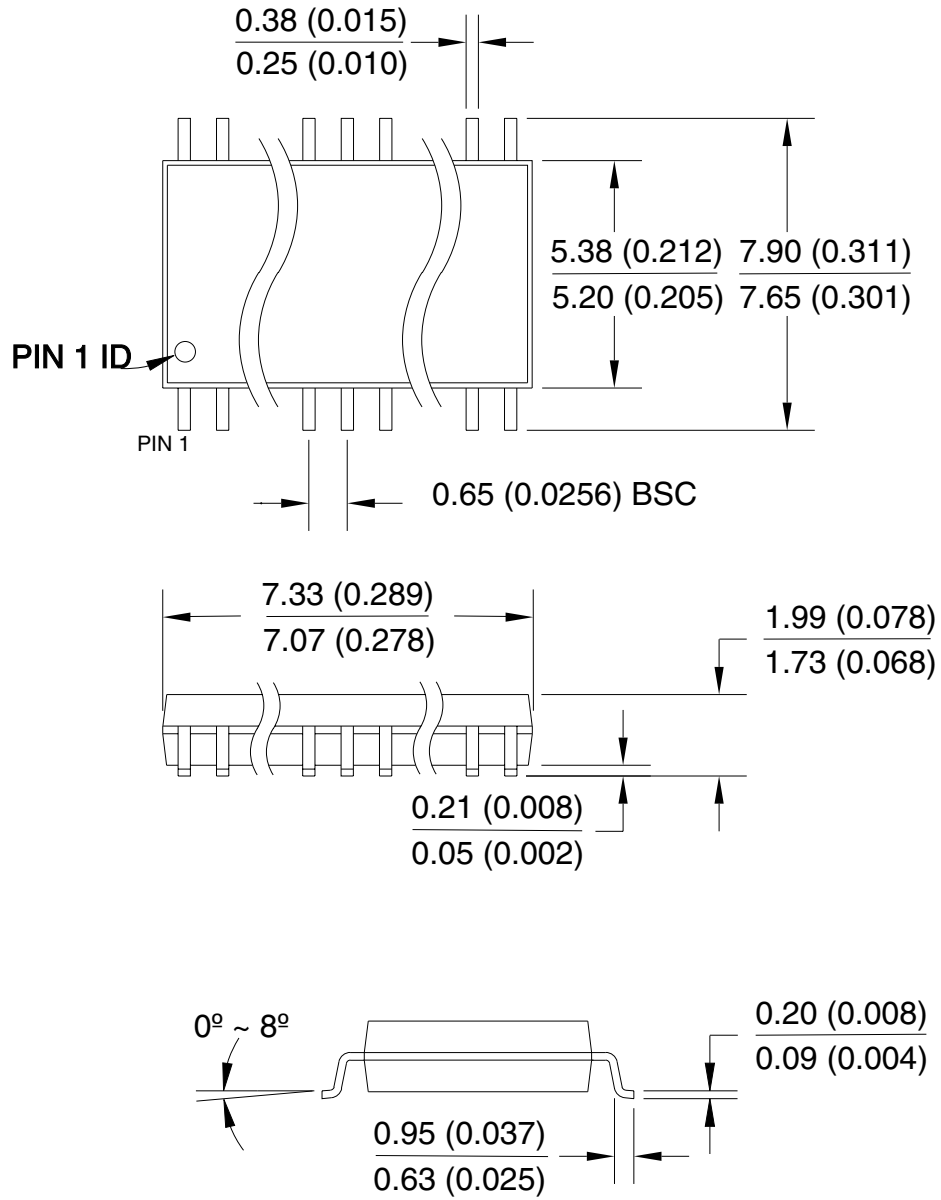
Mnemonic	Operands	Description	Operation	Flags	# Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add Two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry Two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
SUB	Rd, Rr	Subtract Two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry Two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (\text{FFh} - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
RET		Subroutine Return	$PC \leftarrow \text{STACK}$	None	4
RETI		Interrupt Return	$PC \leftarrow \text{STACK}$	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2
CP	Rd, Rr	Compare	$Rd - Rr$	Z,N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	$Rd - Rr - C$	Z,N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	$Rd - K$	Z,N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half-carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half-carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T-Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T-Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
DATA TRANSFER INSTRUCTIONS					
LD	Rd, Z	Load Register Indirect	$Rd \leftarrow (Z)$	None	2
ST	Z, Rr	Store Register Indirect	$(Z) \leftarrow Rr$	None	2
MOV	Rd, Rr	Move between Registers	$Rd \leftarrow Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1

Instruction Set Summary (Continued)

Mnemonic	Operands	Description	Operation	Flags	# Clocks
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P, b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P, b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n = 0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit Load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Two's Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Two's Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half-carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half-carry Flag in SREG	$H \leftarrow 0$	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

20Y

20Y, 20-lead Plastic Shrink Small
Outline (SSOP), 5.3mm body Width.
Dimensions in Millimeters and (inches)*



*Controlling dimension: millimeters

REV. A 04/11/2001



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