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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	12MHz
Connectivity	SPI
Peripherals	POR, WDT
Number of I/O	15
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/at90s1200a-12pi">https://www.e-xfl.com/product-detail/microchip-technology/at90s1200a-12pi</a>

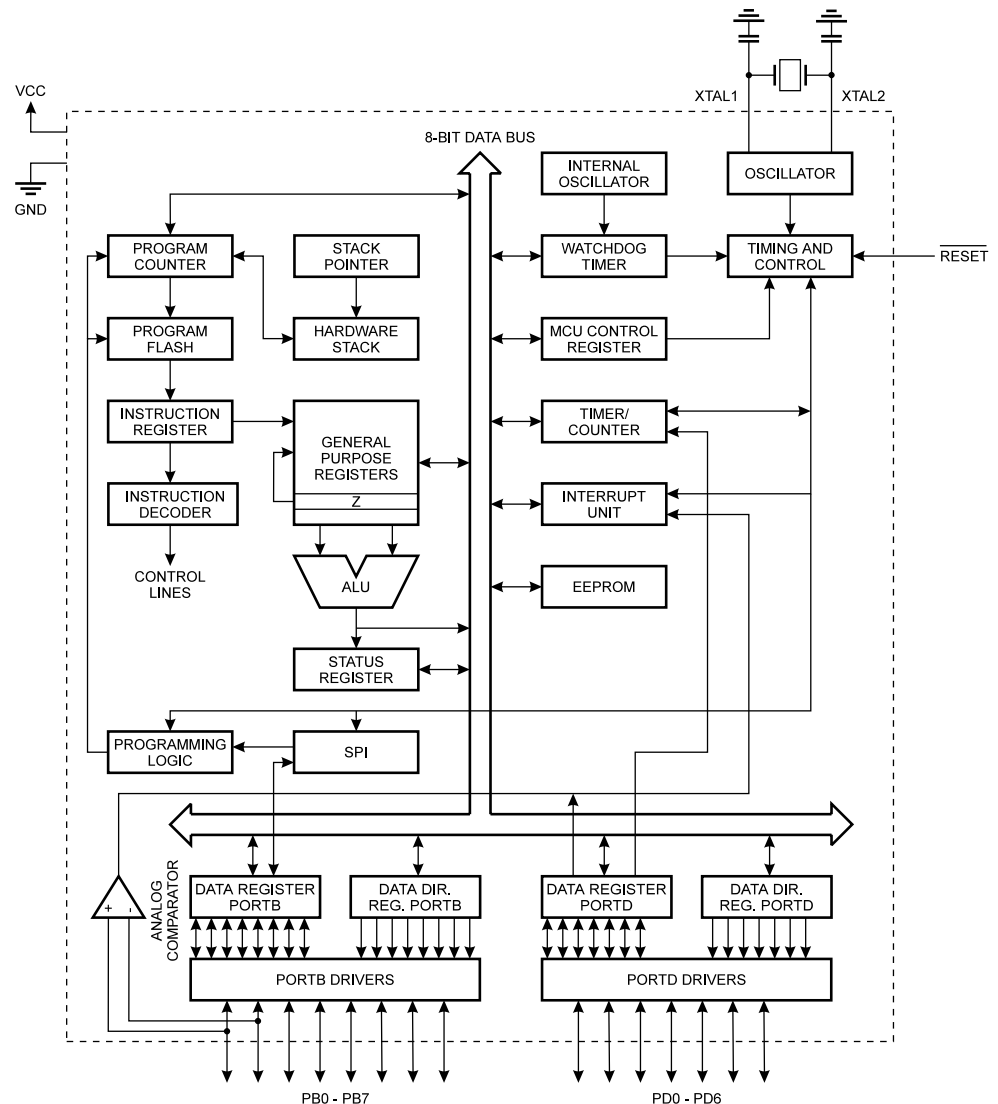
## Description

The AT90S1200 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S1200 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with the 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

## Block Diagram

**Figure 1.** The AT90S1200 Block Diagram

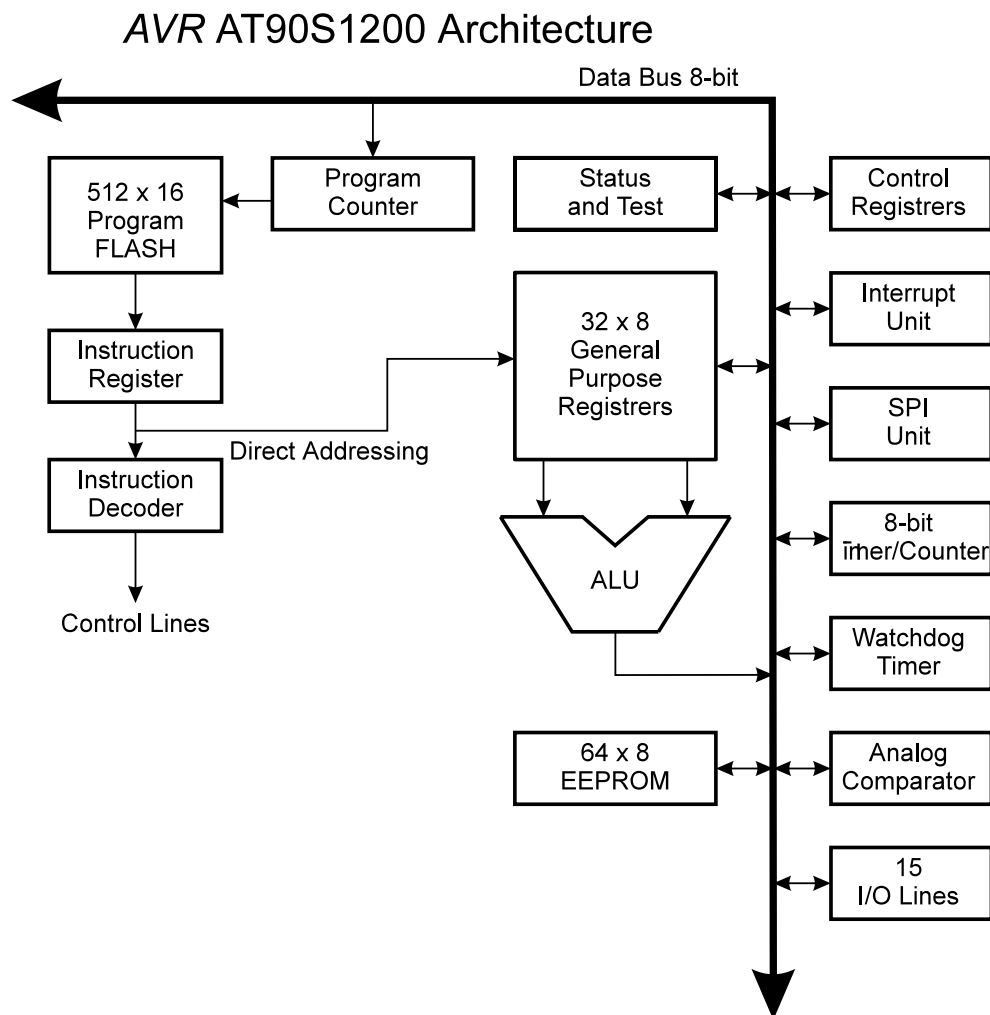


The architecture supports high-level languages efficiently as well as extremely dense assembler code programs. The AT90S1200 provides the following features: 1K byte of In-System Programmable Flash, 64 bytes EEPROM, 15 general purpose I/O lines, 32 general purpose working registers, internal and external interrupts, programmable watchdog timer with internal oscillator, an SPI serial port for program downloading and two software selectable power-saving modes. The Idle Mode stops the CPU while allow-

## Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

**Figure 4.** The AT90S1200 AVR RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S1200 AVR RISC microcontroller architecture. The AVR uses a Harvard architecture concept – with separate memories and buses for program and data memories. The program memory is accessed with a 2-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and relative call instructions, the whole 512 address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the stack. The stack is a 3-level-deep hardware stack dedicated for subroutines and interrupts.

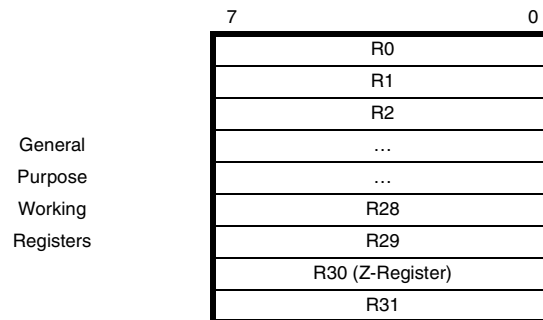
The I/O memory space contains 64 addresses for CPU peripheral functions such as Control Registers, Timer/Counters, A/D Converters and other I/O functions. The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

## General Purpose Register File

Figure 5 shows the structure of the 32 general purpose registers in the CPU.

**Figure 5.** AVR CPU General Purpose Working Registers



All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exception is the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, ORI between a constant and a register and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the register file (R16..R31). The general SBC, SUB, CP, AND, OR and all other operations between two registers or on a single register apply to the entire register file.

Register 30 also serves as an 8-bit pointer for indirect address of the register file.

## ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories – arithmetic, logic and bit-functions.

## In-System Programmable Flash Program Memory

The AT90S1200 contains 1K bytes On-chip In-System Programmable Flash memory for program storage. Since all instructions are single 16-bit words, the Flash is organized as 512 x 16. The Flash memory has an endurance of at least 1000 write/erase cycles.

The AT90S1200 Program Counter is 9 bits wide, thus addressing the 512 words Flash program memory.

See page 37 for a detailed description on Flash data downloading.

## I/O Memory

The I/O space definition of the AT90S1200 is shown in the following table.

**Table 1.** The AT90S1200 I/O Space

Address Hex	Name	Function
\$3F	SREG	Status REGister
\$3B	GIMSK	General Interrupt MaSK register
\$39	TIMSK	Timer/Counter Interrupt MaSK register
\$38	TIFR	Timer/Counter Interrupt Flag register
\$35	MCUCR	MCU general Control Register
\$33	TCCR0	Timer/Counter0 Control Register
\$32	TCNT0	Timer/Counter0 (8-bit)
\$21	WDTCR	Watchdog Timer Control Register
\$1E	EEAR	EEPROM Address Register
\$1D	EEDR	EEPROM Data Register
\$1C	EECR	EEPROM Control Register
\$18	PORTB	Data Register, Port B
\$17	DDRB	Data Direction Register, Port B
\$16	PINB	Input Pins, Port B
\$12	PORTD	Data Register, Port D
\$11	DDRD	Data Direction Register, Port D
\$10	PIND	Input Pins, Port D
\$08	ACSR	Analog Comparator Control and Status Register

Note: Reserved and unused locations are not shown in the table.

All AT90S1200 I/Os and peripherals are placed in the I/O space. The different I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set chapter for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

The different I/O and peripherals control registers are explained in the following sections.

## Status Register – SREG

The AVR status register (SREG) at I/O space location \$3F is defined as:

Bit	7	6	5	4	3	2	1	0	
\$3F	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### • Bit 7 – I: Global Interrupt Enable

The global interrupt enable bit must be set (one) for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the global interrupt enable bit is cleared (zero), none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts.

### • Bit 6 – T: Bit Copy Storage

The bit copy instructions BLD (Bit Load) and BST (Bit Store) use the T-bit as source and destination for the operated bit. A bit from a register in the register file can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the register file by the BLD instruction.

### • Bit 5 – H: Half-carry Flag

The half-carry flag H indicates a half carry in some arithmetic operations. See the Instruction Set description for detailed information.

### • Bit 4 – S: Sign Bit, $S = N \oplus V$

The S-bit is always an exclusive or between the negative flag N and the two's complement overflow flag V. See the Instruction Set description for detailed information.

### • Bit 3 – V: Two's Complement Overflow Flag

The two's complement overflow flag V supports two's complement arithmetics. See the Instruction Set description for detailed information.

### • Bit 2 – N: Negative Flag

The negative flag N indicates a negative result after the different arithmetic and logic operations. See the Instruction Set description for detailed information.

### • Bit 1 – Z: Zero Flag

The zero flag Z indicates a zero result after the different arithmetic and logic operations. See the Instruction Set description for detailed information.

### • Bit 0 – C: Carry Flag

The carry flag C indicates a carry in an arithmetic or logic operation. See the Instruction Set description for detailed information.

Note that the status register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

## Reset and Interrupt Handling

The AT90S1200 provides three different interrupt sources. These interrupts and the separate reset vector, each have a separate program vector in the program memory space. All the interrupts are assigned individual enable bits that must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

**Table 2.** Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	\$000	RESET	Hardware Pin, Power-on Reset and Watchdog Reset
2	\$001	INT0	External Interrupt Request 0
4	\$002	TIMER0, OVFO	Timer/Counter0 Overflow
5	\$003	ANA_COMP	Analog Comparator

The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

Address	Labels	Code	Comments
\$000		rjmp RESET	; Reset Handler
\$001		rjmp EXT_INT0	; IRQ0 Handler
\$002		rjmp TIM0_OVF	; Timer0 Overflow Handler
\$003		rjmp ANA_COMP	; Analog Comparator Handler
			;
\$004	MAIN:	<instr> xxx	; Main program start
...	...	...	...

## Reset Sources

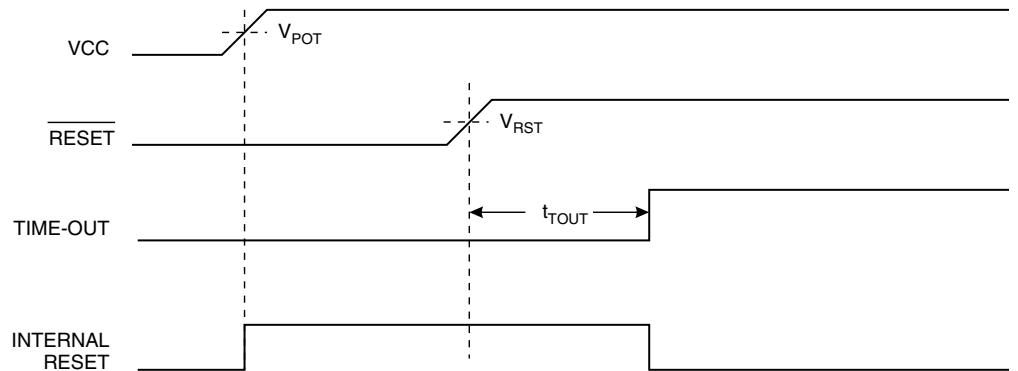
The AT90S1200 has three sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the power-on Reset threshold ( $V_{POT}$ ).
- External Reset. The MCU is reset when a low level is present on the  $\overline{RESET}$  pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.

During Reset, all I/O registers are then set to their initial values, and the program starts execution from address \$000. The instruction placed in address \$000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 13 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry. Note that Power-on Reset timing is clocked by the internal RC Oscillator. Refer to characterization data for RC Oscillator frequency at other  $V_{CC}$  voltages.

been applied, the Power-on Reset period can be extended. Refer to Figure 15 for a timing example on this.

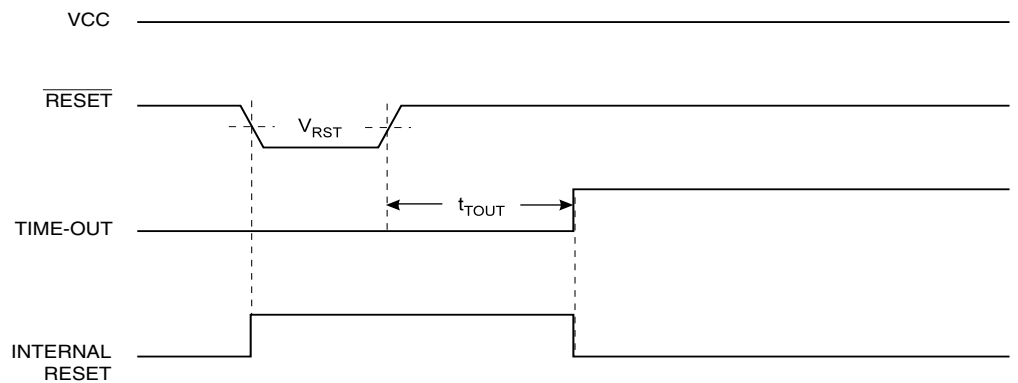
**Figure 15.** MCU Start-up,  $\overline{\text{RESET}}$  Controlled Externally



### External Reset

An External Reset is generated by a low level on the  $\overline{\text{RESET}}$  pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage ( $V_{\text{RST}}$ ) on its positive edge, the delay timer starts the MCU after the Time-out period  $t_{\text{TOUT}}$  has expired.

**Figure 16.** External Reset during Operation



### Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period  $t_{\text{TOUT}}$ . Refer to page 23 for details on operation of the Watchdog.



## **External Interrupts**

The External Interrupt is triggered by the INT0 pin. The interrupt can trigger on rising edge, falling edge or low level. This is set up as described in the specification for the MCU Control Register (MCUCR). When INT0 is level triggered, the interrupt is pending as long as INT0 is held low.

The interrupt is triggered even if INT0 is configured as an output. This provides a way to generate a software interrupt.

The interrupt flag can not be directly accessed by the user. If an external edge-triggered interrupt is suspected to be pending, the flag can be cleared as follows.

1. Disable the External Interrupt by clearing the INT0 flag in GIMSK.
2. Select level triggered interrupt.
3. Select desired interrupt edge.
4. Re-enable the external interrupt by setting INT0 in GIMSK.

## **Interrupt Response Time**

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. Four clock cycles after the interrupt flag has been set, the program vector address for the actual interrupt handling routine is executed. During this 4-clock-cycle period, the Program Counter (9 bits) is pushed onto the Stack. The vector is normally a relative jump to the interrupt routine, and this jump takes two clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (9 bits) is popped back from the Stack and the I-flag in SREG is set. When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Subroutine and Interrupt Stack is a 3-level true hardware stack, and if more than three nested subroutines and interrupts are executed, only the most recent three return addresses are stored.

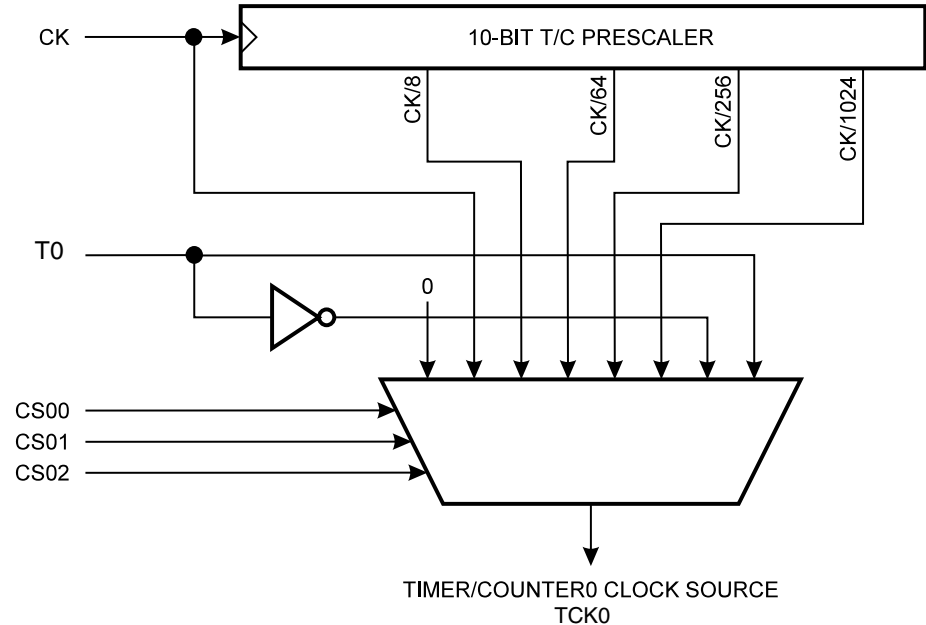
## Timer/Counter0

### Timer/Counter0 Prescaler

The AT90S1200 provides one general purpose 8-bit Timer/Counter. The Timer/Counter0 gets the prescaled clock from the 10-bit prescaling timer. The Timer/Counter0 can either be used as a Timer with an internal clock time base or as a Counter with an external pin connection, which triggers the counting.

Figure 18 shows the general Timer/Counter0 prescaler.

**Figure 18.** Timer/Counter0 Prescaler



The four different prescaled selections are: CK/8, CK/64, CK/256, and CK/1024 where CK is the Oscillator Clock. For the Timer/Counter0, added selections as CK, external clock source and stop, can be selected as clock sources. Figure 19 shows the block diagram for Timer/Counter0.

## I/O Ports

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

### Port B

Port B is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB (\$18), Data Direction Register – DDRB (\$17), and the Port B Input Pins – PINB (\$16). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 8.

**Table 8.** Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	AIN0 (Analog Comparator positive input)
PB1	AIN1 (Analog Comparator negative input)
PB5	MOSI (Data Input line for memory downloading)
PB6	MISO (Data Output line for memory uploading)
PB7	SCK (Serial Clock input)

When the pins are used for the alternate function, the DDRB and PORTB register has to be set according to the alternate function description.

### Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
\$18	<b>PORTB7</b>	<b>PORTB6</b>	<b>PORTB5</b>	<b>PORTB4</b>	<b>PORTB3</b>	<b>PORTB2</b>	<b>PORTB1</b>	<b>PORTB0</b>	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
\$17	<b>DDB7</b>	<b>DDB6</b>	<b>DDB5</b>	<b>DDB4</b>	<b>DDB3</b>	<b>DDB2</b>	<b>DDB1</b>	<b>DDB0</b>	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### Port B Input Pin Address – PINB

Bit	7	6	5	4	3	2	1	0	
\$16	<b>PINB7</b>	<b>PINB6</b>	<b>PINB5</b>	<b>PINB4</b>	<b>PINB3</b>	<b>PINB2</b>	<b>PINB1</b>	<b>PINB0</b>	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port B Input Pins address (PINB) is not a register, and this address enables access to the physical value on each Port B pin. When reading PORTB, the Port B Data Latch is read, and when reading PINB, the logical values present on the pins are read.

Figure 25. Port B Schematic Diagram (Pin PB6)

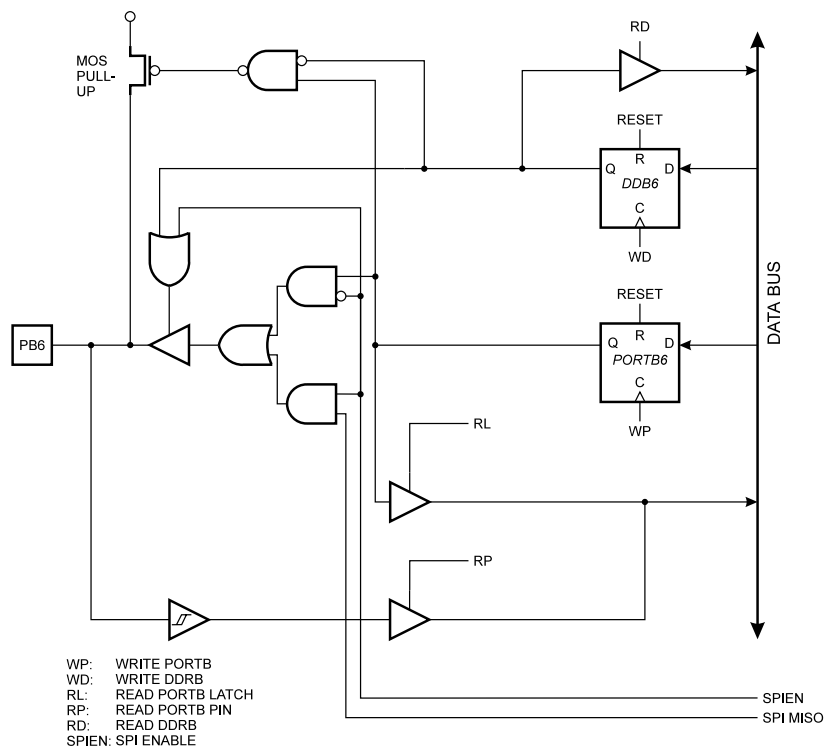
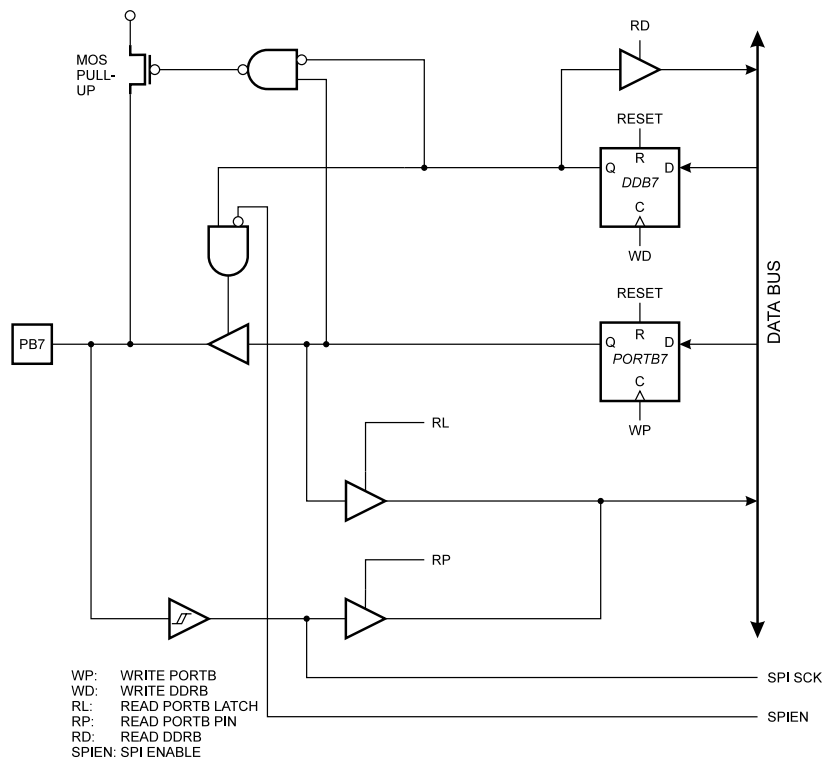
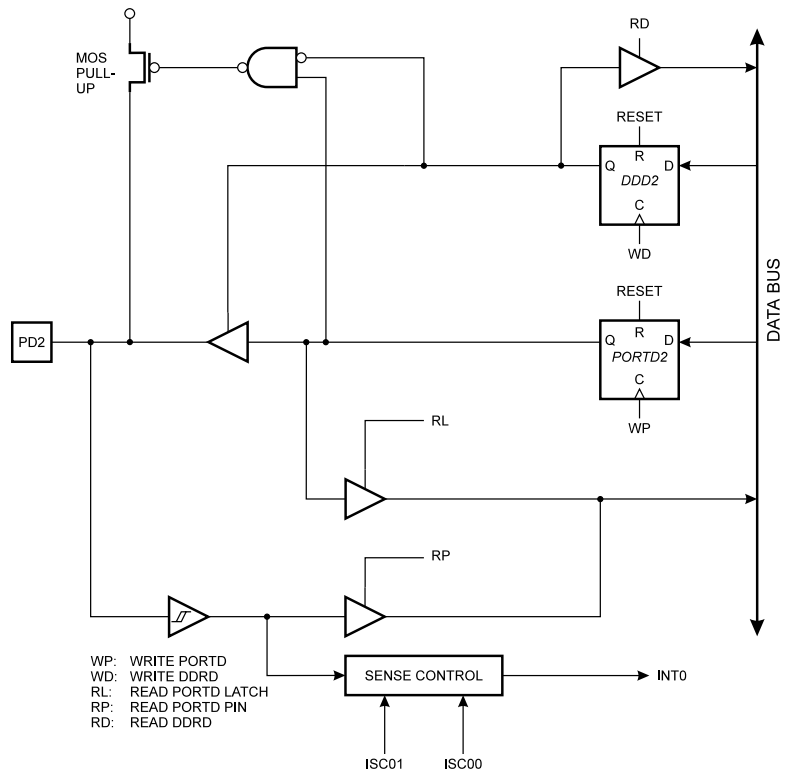


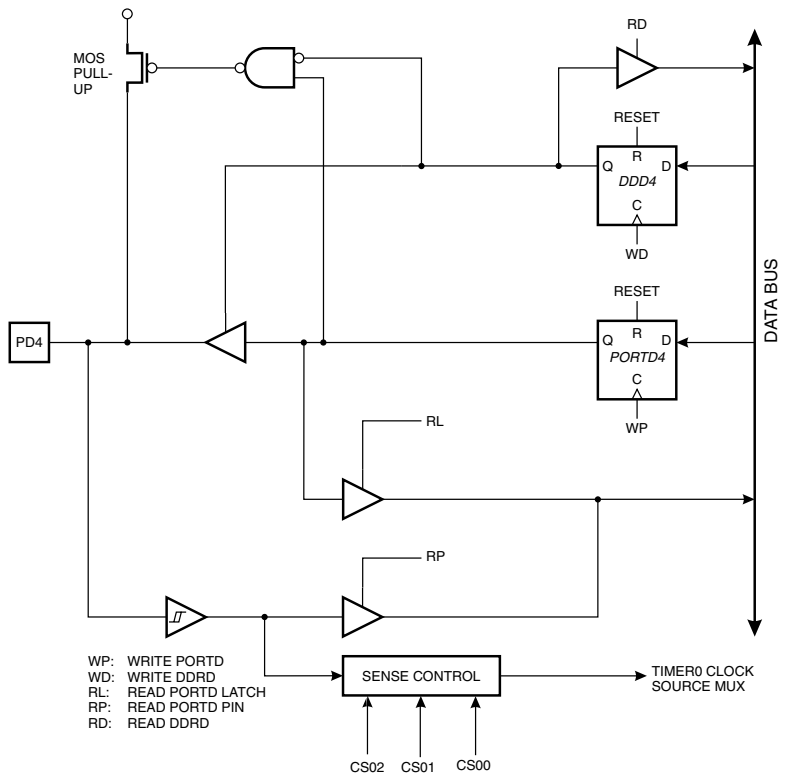
Figure 26. Port B Schematic Diagram (Pin PB7)



**Figure 28. Port D Schematic Diagram (Pin PD2)**



**Figure 29. Port D Schematic Diagram (Pin PD4)**



## Memory Programming

### Program and Data Memory Lock Bits

The AT90S1200 MCU provides two Lock bits that can be left unprogrammed ("1") or can be programmed ("0") to obtain the additional features listed in Table 12. The Lock bits can only be erased with the Chip Erase command.

**Table 12.** Lock Bit Protection Modes

Memory Lock Bits			Protection Type
Mode	LB1	LB2	
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled. <sup>(1)</sup>
3	0	0	Same as mode 2, and verify is also disabled.

Note: 1. In Parallel mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

### Fuse Bits

The AT90S1200 has two Fuse bits: SPIEN and RCEN.

- When the SPIEN Fuse bit is programmed ("0"), Serial Program Downloading is enabled. Default value is programmed ("0").
- When the RCEN Fuse bit is programmed ("0"), MCU clocking from the Internal RC Oscillator is selected. Default value is erased ("1"). Parts with this bit pre-programmed ("0") can be delivered on demand.
- The Fuse bits are not accessible in Serial Programming mode. The status of the Fuse bits is not affected by Chip Erase.

### Signature Bytes

All Atmel microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both Serial and Parallel modes. The three bytes reside in a separate address space.

For the AT90S1200 they are:

1. \$00: \$1E (indicates manufactured by Atmel)
2. \$01: \$90 (indicates 1 Kb Flash memory)
3. \$02: \$01 (indicates AT90S1200 device when \$01 is \$90)

Note: When both Lock bits are programmed (lock mode 3), the signature bytes cannot be read in Serial mode. Reading the signature bytes will return: \$00, \$01 and \$02.

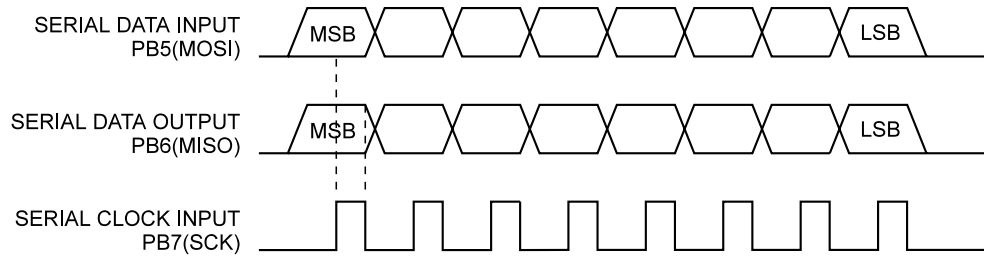
### Programming the Flash and EEPROM

Atmel's AT90S1200 offers 1K byte of in-System Reprogrammable Flash program memory and 64 bytes of EEPROM data memory.

The AT90S1200 is normally shipped with the On-chip Flash program memory and EEPROM data memory arrays in the erased state (i.e., contents = \$FF) and ready to be programmed. This device supports a High-voltage (12V) Parallel Programming mode and a Low-voltage Serial Programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The Serial Programming mode provides a convenient way to download program and data into the AT90S1200 inside the user's system.

The program and data memory arrays on the AT90S1200 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided within

**Figure 35. Serial Programming Waveforms**



**Table 19. Serial Programming Instruction Set for AT90S1200**

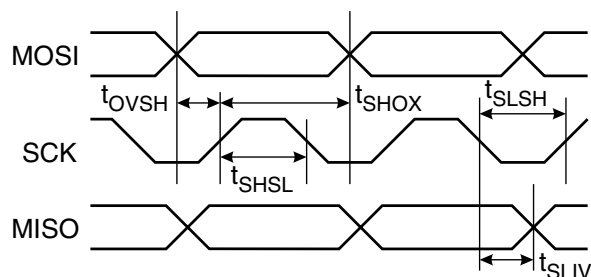
Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable serial programming while $\overline{\text{RESET}}$ is low.
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase both Flash and EEPROM memory arrays.
Read Program Memory	0010 H000	0000 000a	bbbb bbbb	oooo oooo	Read H (high or low) byte o from program memory at word address a:b.
Write Program Memory	0100 H000	0000 000a	bbbb bbbb	iiii iiii	Write H (high or low) byte i to program memory at word address a:b.
Read EEPROM Memory	1010 0000	0000 0000	00bb bbbb	oooo oooo	Read data o from EEPROM memory at address b.
Write EEPROM Memory	1100 0000	0000 0000	00bb bbbb	iiii iiii	Write data i to EEPROM memory at address b.
Write Lock Bits	1010 1100	1111 1211	xxxx xxxx	xxxx xxxx	Write Lock bits. Set bits 1,2 = "0" to program Lock bits.
Read Signature Byte	0011 0000	xxxx xxxx	xxxx xxbb	oooo oooo	Read signature byte o from address b. <sup>(1)</sup>

Note: a = address high bits, b = address low bits, H = 0 – Low byte, 1 – High byte, o = data out, i = data in, x = don't care, 1 = Lock Bit 1, 2 = Lock Bit 2

Note: 1. The signature bytes are not readable in lock mode 3 (i.e., both Lock bits programmed).

## Serial Programming Characteristics

**Figure 36.** Serial Programming Timing



**Table 20.** Serial Programming Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 2.7 - 6.0\text{V}$  (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency ( $V_{CC} = 2.7 - 4.0\text{V}$ )	0		4.0	MHz
$t_{CLCL}$	Oscillator Period ( $V_{CC} = 2.7 - 4.0\text{V}$ )	250.0			ns
$1/t_{CLCL}$	Oscillator Frequency ( $V_{CC} = 4.0 - 6.0\text{V}$ )	0		12.0	MHz
$t_{CLCL}$	Oscillator Period ( $V_{CC} = 4.0 - 6.0\text{V}$ )	83.3			ns
$t_{SHSL}$	SCK Pulse Width High	$4.0 t_{CLCL}$			ns
$t_{SLSH}$	SCK Pulse Width Low	$t_{CLCL}$			ns
$t_{OVSH}$	MOSI Setup to SCK High	$1.25 t_{CLCL}$			ns
$t_{SHOX}$	MOSI Hold after SCK High	$2.5 t_{CLCL}$			ns
$t_{SLIV}$	SCK Low to MISO Valid	10.0	16.0	32.0	ns

**Table 21.** Minimum Wait Delay after the Chip Erase Instruction

Symbol	3.2V	3.6V	4.0V	5.0V
$t_{WD\_ERASE}$	18 ms	14 ms	12 ms	8 ms

**Table 22.** Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	3.2V	3.6V	4.0V	5.0V
$t_{WD\_PROG}$	9 ms	7 ms	6 ms	4 ms



## DC Characteristics

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $6.0\text{V}$  (unless otherwise noted) (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{ACIO}$	Analog Comparator Input Offset Voltage	$V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$			40.0	mV
$I_{ACLK}$	Analog Comparator Input Leakage Current	$V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$	-50.0		50.0	nA
$t_{ACPD}$	Analog Comparator Propagation Delay	$V_{CC} = 2.7\text{V}$ $V_{CC} = 4.0\text{V}$		750.0 500.0		ns

- Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low.
  2. "Min" means the lowest value where the pin is guaranteed to be read as high.
  3. Although each I/O port can sink more than the test conditions (20 mA at  $V_{CC} = 5\text{V}$ , 10 mA at  $V_{CC} = 3\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - 1] The sum of all  $I_{OL}$  for all ports, should not exceed 200 mA.
    - 2] The sum of all  $I_{OL}$  for port D0 - D5 and XTAL2, should not exceed 100 mA.
    - 3] The sum of all  $I_{OL}$  for ports B0 - B7 and D6, should not exceed 100 mA.
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
  4. Although each I/O port can source more than the test conditions (3 mA at  $V_{CC} = 5\text{V}$ , 1.5 mA at  $V_{CC} = 3\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - 1] The sum of all  $I_{OH}$  for all ports, should not exceed 200 mA.
    - 2] The sum of all  $I_{OH}$  for port D0 - D5 and XTAL2, should not exceed 100 mA.
    - 3] The sum of all  $I_{OH}$  for ports B0 - B7 and D6, should not exceed 100 mA.
 If  $I_{OH}$  exceeds the test condition,  $V_{OH}$  may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
  5. Minimum  $V_{CC}$  for power-down is 2V.

## Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

The power consumption in Power-down mode is independent of clock selection.

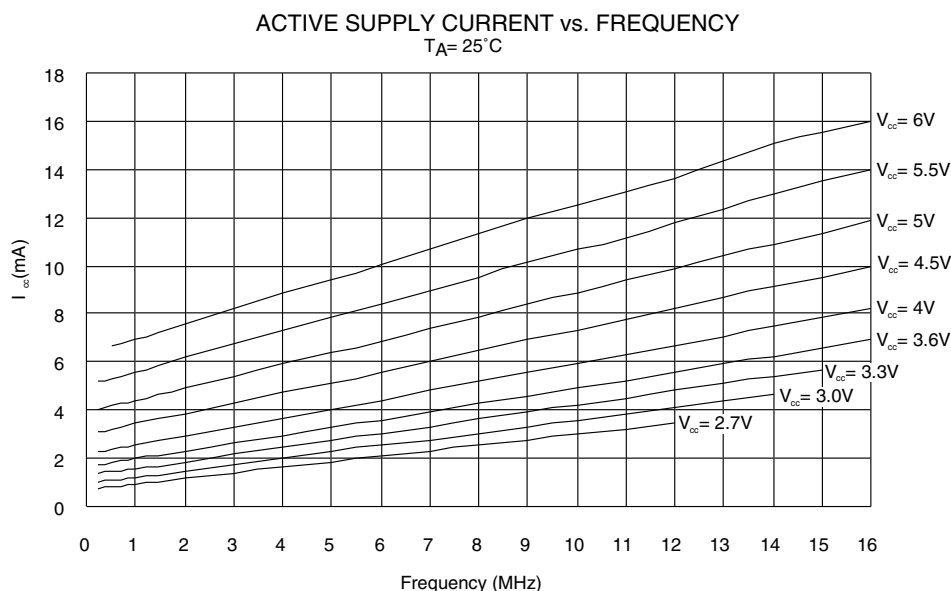
The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as  $C_L \cdot V_{CC} \cdot f$  where  $C_L$  = load capacitance,  $V_{CC}$  = operating voltage and  $f$  = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

**Figure 38.** Active Supply Current vs. Frequency



## Ordering Information<sup>(1)</sup>

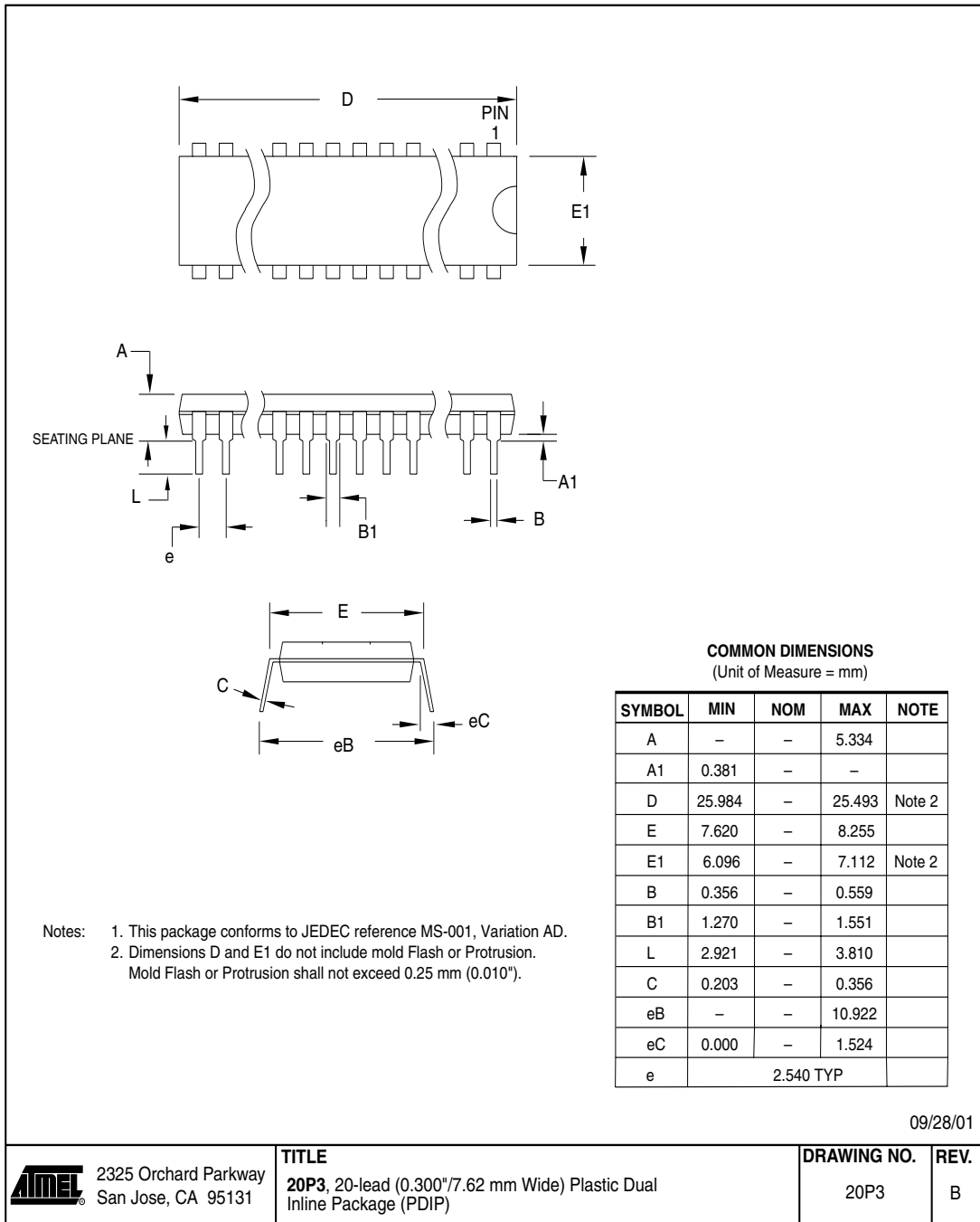
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
4	2.7 - 6.0V	AT90S1200-4PC	20P3	Commercial (0°C to 70°C)
		AT90S1200-4SC	20S	
		AT90S1200-4YC	20Y	
		AT90S1200-4PI	20P3	Industrial (-40°C to 85°C)
		AT90S1200-4SI	20S	
		AT90S1200-4YI	20Y	
12	4.0 - 6.0V	AT90S1200-12PC	20P3	Commercial (0°C to 70°C)
		AT90S1200-12SC	20S	
		AT90S1200-12YC	20Y	
		AT90S1200-12PI	20P3	Industrial (-40°C to 85°C)
		AT90S1200-12SI	20S	
		AT90S1200-12YI	20Y	

Note: 1. Order AT90S1200A-XXX for devices with the RCEN Fuse programmed.

Package Type	
<b>20P3</b>	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>20S</b>	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>20Y</b>	20-lead, 5.3 mm Wide, Plastic Shrink Small Outline Package (SSOP)

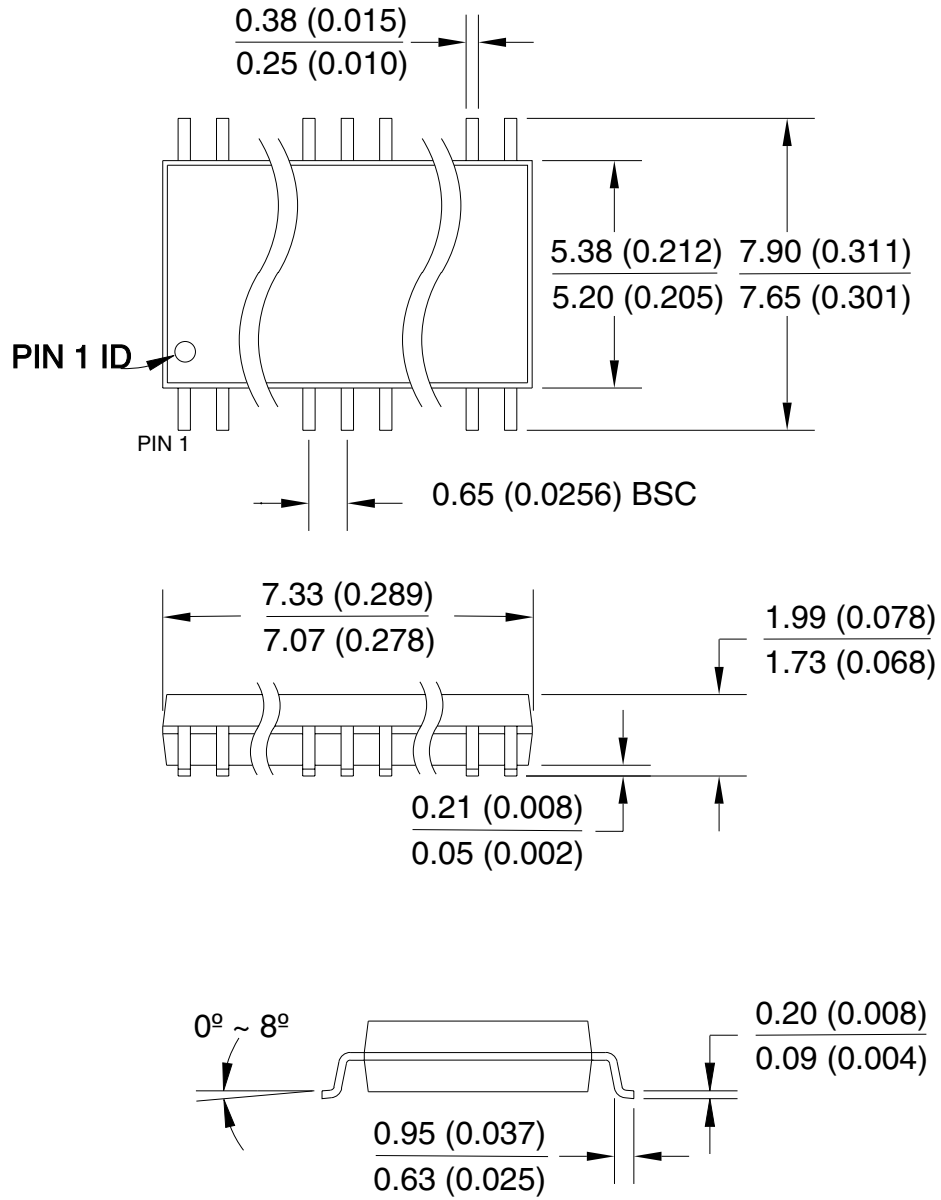
## Packaging Information

### 20P3



20Y

20Y, 20-lead Plastic Shrink Small  
Outline (SSOP), 5.3mm body Width.  
Dimensions in Millimeters and (inches)\*



\*Controlling dimension: millimeters

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