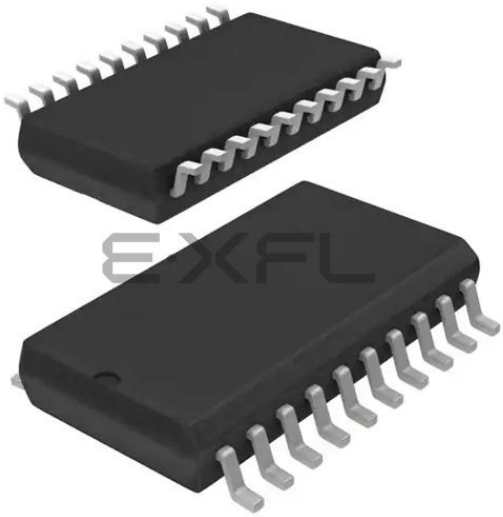

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

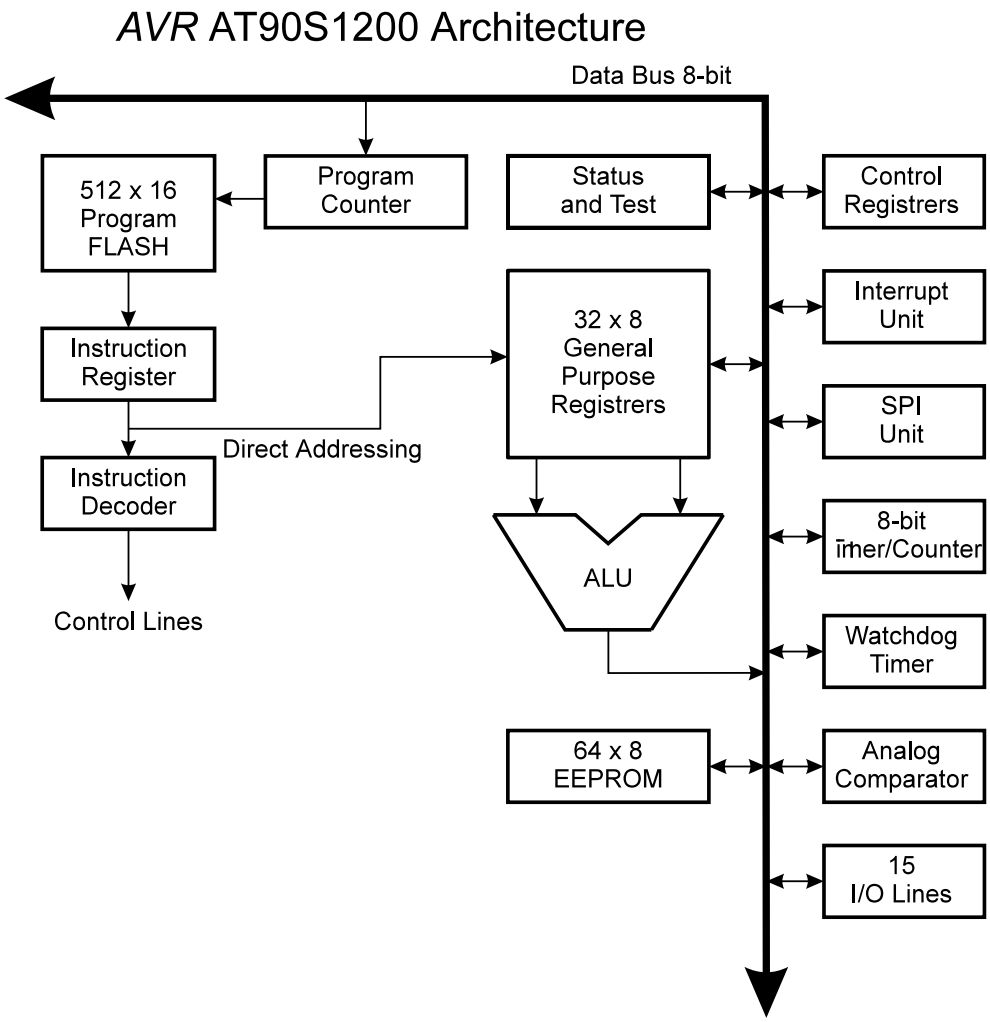
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	12MHz
Connectivity	SPI
Peripherals	POR, WDT
Number of I/O	15
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s1200a-12sc

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Figure 4. The AT90S1200 AVR RISC Architecture



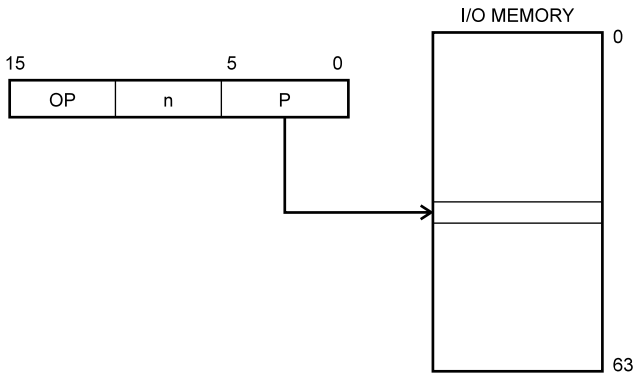
The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S1200 AVR RISC microcontroller architecture. The AVR uses a Harvard architecture concept – with separate memories and buses for program and data memories. The program memory is accessed with a 2-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and relative call instructions, the whole 512 address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

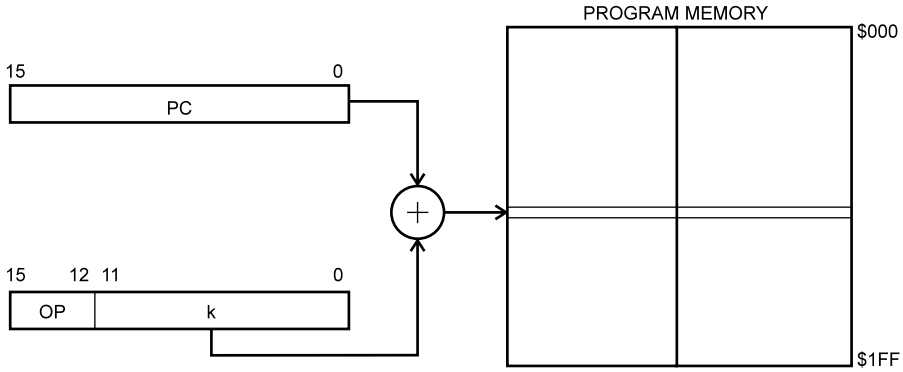
Figure 9. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

Relative Program Addressing, RJMP and RCALL

Figure 10. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

Subroutine and Interrupt Hardware Stack

The AT90S1200 uses a 3 level deep hardware stack for subroutines and interrupts. The hardware stack is 9 bits wide and stores the Program Counter (PC) return address while subroutines and interrupts are executed.

RCALL instructions and interrupts push the PC return address onto stack level 0, and the data in the other stack levels 1 - 2 are pushed one level deeper in the stack. When a RET or RETI instruction is executed the returning PC is fetched from stack level 0, and the data in the other stack levels 1 - 2 are popped one level in the stack.

If more than three subsequent subroutine calls or interrupts are executed, the first values written to the stack are overwritten.

I/O Memory

The I/O space definition of the AT90S1200 is shown in the following table.

Table 1. The AT90S1200 I/O Space

Address Hex	Name	Function
$3F	SREG	Status REGister
$3B	GIMSK	General Interrupt MaSK register
$39	TIMSK	Timer/Counter Interrupt MaSK register
$38	TIFR	Timer/Counter Interrupt Flag register
$35	MCUCR	MCU general Control Register
$33	TCCR0	Timer/Counter0 Control Register
$32	TCNT0	Timer/Counter0 (8-bit)
$21	WDTCR	Watchdog Timer Control Register
$1E	EEAR	EEPROM Address Register
$1D	EEDR	EEPROM Data Register
$1C	EECR	EEPROM Control Register
$18	PORTB	Data Register, Port B
$17	DDRB	Data Direction Register, Port B
$16	PINB	Input Pins, Port B
$12	PORTD	Data Register, Port D
$11	DDRD	Data Direction Register, Port D
$10	PIND	Input Pins, Port D
$08	ACSR	Analog Comparator Control and Status Register

Note: Reserved and unused locations are not shown in the table.

All AT90S1200 I/Os and peripherals are placed in the I/O space. The different I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set chapter for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

The different I/O and peripherals control registers are explained in the following sections.

Figure 13. Reset Logic

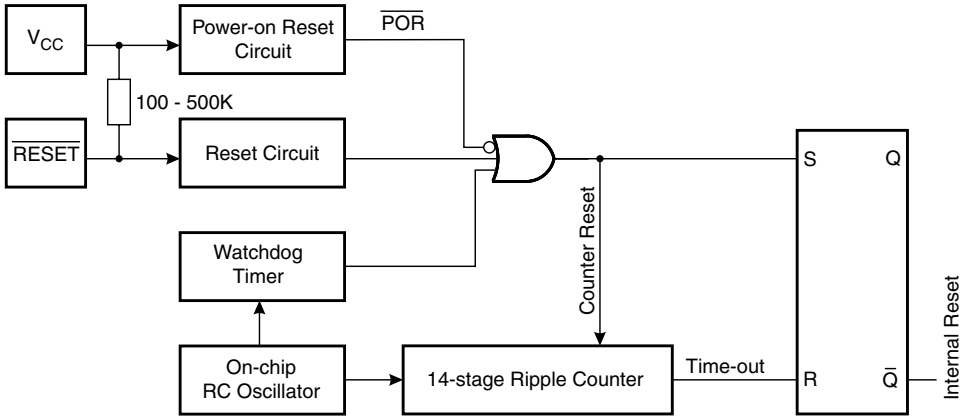


Table 3. Reset Characteristics (V_{CC} = 5.0V)

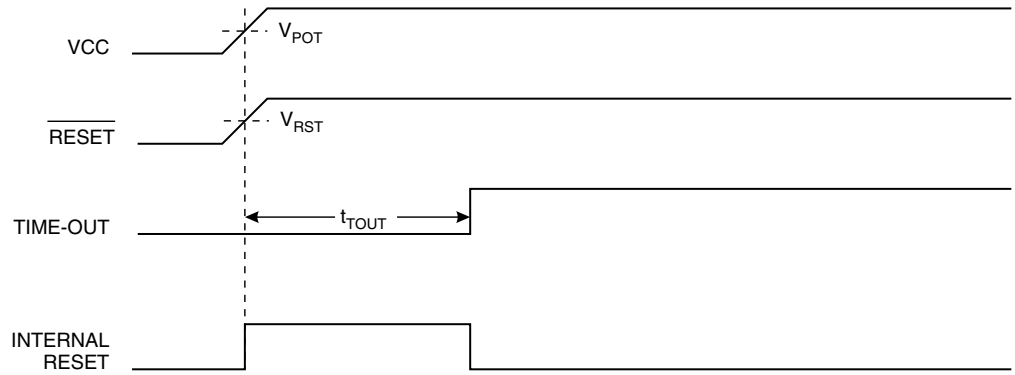
Symbol	Parameter	Min	Typ	Max	Units
V_{POT}(1)	Power-on Reset Threshold Voltage (rising)	0.8	1.2	1.6	V
	Power-on Reset Threshold Voltage (falling)	0.2	0.4	0.6	V
V_{RST}	Pin Threshold Voltage	–	–	0.85 V_{CC}	V
t_{POR}	Power-on Reset Period	2.0	3.0	4.0	ms
t_{TOUT}	Reset Delay Time-out Period (The Time-out period equals 16K WDT cycles. See "Typical Characteristics" on page 51. for typical WDT frequency at different voltages).	11.0	16.0	21.0	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Power-on Reset

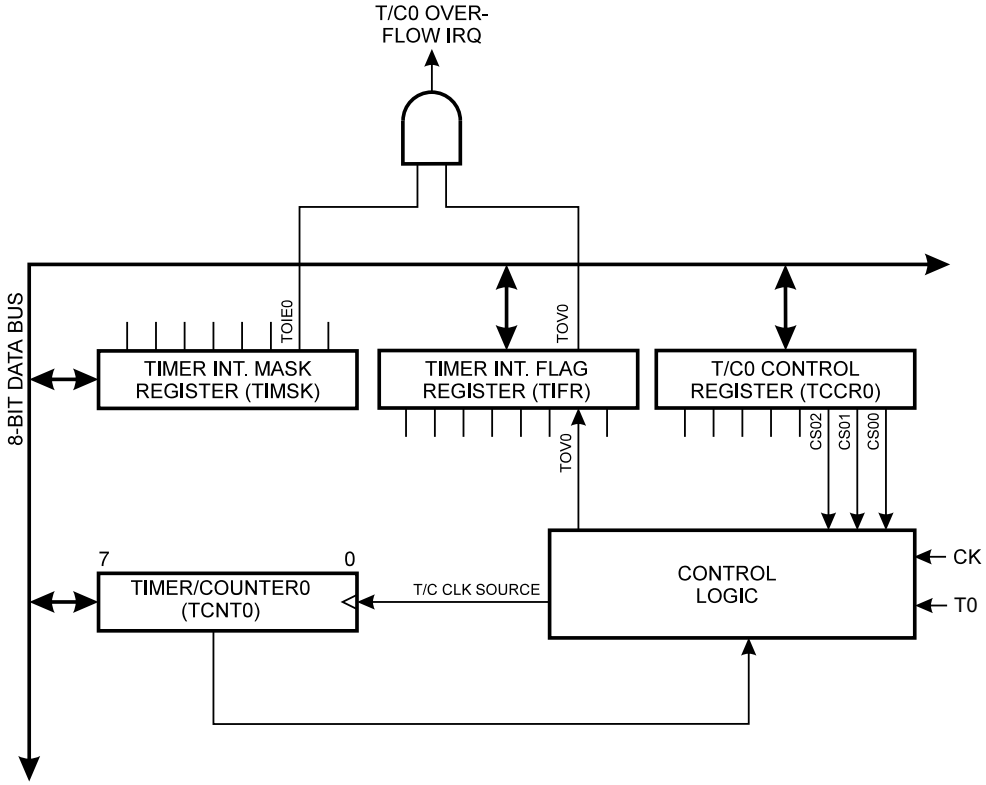
A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 13, an internal timer clocked from the Watchdog timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage (V_{POT}), regardless of the V_{CC} rise time (see Figure 14).

Figure 14. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}.



If the built-in start-up delay is sufficient, $\overline{\text{RESET}}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the $\overline{\text{RESET}}$ pin low for a period after V_{CC} has

Figure 19. Timer/Counter0 Block Diagram



The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK or an external pin. In addition it can be stopped as described in the specification for the Timer/Counter0 Control Register (TCCR0). The overflow status flag is found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter0 Control Register (TCCR0). The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

Timer/Counter0 Control Register – TCCR0

Bit	7	6	5	4	3	2	1	0	
$33	-	-	-	-	-	CS02	CS01	CS00	TCCR0
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..3 – Res: Reserved Bits**

These bits are reserved bits in the AT90S1200 and always read as zero.

- **Bits 2, 1, 0 – CS02, CS01, CS00: Clock Select0, Bits 2, 1 and 0**

The Clock Select0 bits 2, 1 and 0 define the prescaling source of Timer/Counter0.

Table 5. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, the Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK Oscillator clock. If the external pin modes are used for Timer/Counter0, transitions on PD4/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user SW control of the counting.

Timer/Counter0 – TCNT0

Bit	7	6	5	4	3	2	1	0	
$32	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the timer clock cycle following the write operation.

- **Bit 3 – ACIE: Analog Comparator Interrupt Enable**

When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the Analog Comparator Interrupt is activated. When cleared (zero), the interrupt is disabled.

- **Bit 2 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S1200 and will always read as zero.

- **Bits 1, 0 – ACIS1, ACIS0: Analog Comparator Interrupt Mode Select**

These bits determine which comparator events trigger the Analog Comparator Interrupt. The different settings are shown in Table 7.

Table 7. ACIS1/ACIS0 Settings

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

Note: When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR register. Otherwise, an interrupt can occur when the bits are changed.

I/O Ports

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

Port B

Port B is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB ($18), Data Direction Register – DDRB ($17), and the Port B Input Pins – PINB ($16). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 8.

Table 8. Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	AIN0 (Analog Comparator positive input)
PB1	AIN1 (Analog Comparator negative input)
PB5	MOSI (Data Input line for memory downloading)
PB6	MISO (Data Output line for memory uploading)
PB7	SCK (Serial Clock input)

When the pins are used for the alternate function, the DDRB and PORTB register has to be set according to the alternate function description.

Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
$18	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
$17	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Input Pin Address – PINB

Bit	7	6	5	4	3	2	1	0	
$16	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port B Input Pins address (PINB) is not a register, and this address enables access to the physical value on each Port B pin. When reading PORTB, the Port B Data Latch is read, and when reading PINB, the logical values present on the pins are read.

Port B as General Digital I/O

All eight pins in Port B have equal functionality when used as digital I/O pins.

PBn, General I/O pin: The DDBn bit in the DDRB Register selects the direction of this pin, if DDBn is set (one), PBn is configured as an output pin. If DDBn is cleared (zero), PBn is configured as an input pin. If PORTBn is set (one) and the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, PORTBn has to be cleared (zero) or the pin has to be configured as an output pin. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Table 9. DDBn Effect on Port B Pins

DDBn	PORTBn	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (High-Z)
0	1	Input	Yes	PBn will source current if ext. pulled low.
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7,6...0, pin number.

Alternate Functions of Port B

The alternate pin functions of Port B are:

- **SCK – Port B, Bit 7**

SCK, Clock Input pin for memory up/downloading.

- **MISO – Port B, Bit 6**

MISO, Data Output pin for memory uploading.

- **MOSI – Port B, Bit 5**

MOSI, Data Input pin for memory downloading.

- **AIN1 – Port B, Bit 1**

AIN1, Analog Comparator Negative Input. When configured as an input (DDB1 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB1 is cleared [zero]), this pin also serves as the negative input of the On-chip Analog Comparator.

- **AIN0 – Port B, Bit 0**

AIN0, Analog Comparator Positive Input. When configured as an input (DDB0 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB0 is cleared [zero]), this pin also serves as the positive input of the On-chip Analog Comparator.

Figure 23. Port B Schematic Diagram (Pins PB2, PB3, and PB4)

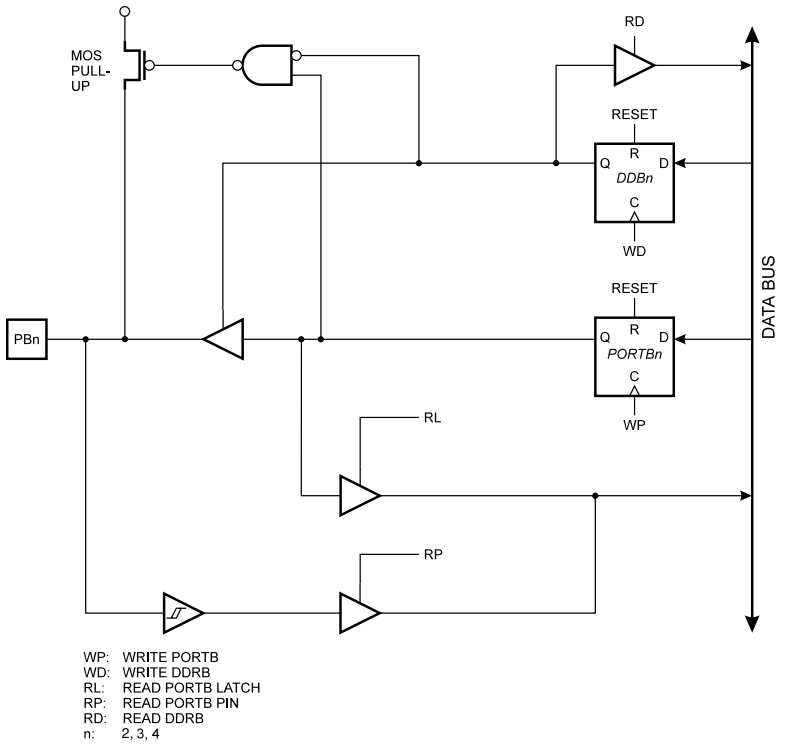


Figure 24. Port B Schematic Diagram (Pin PB5)

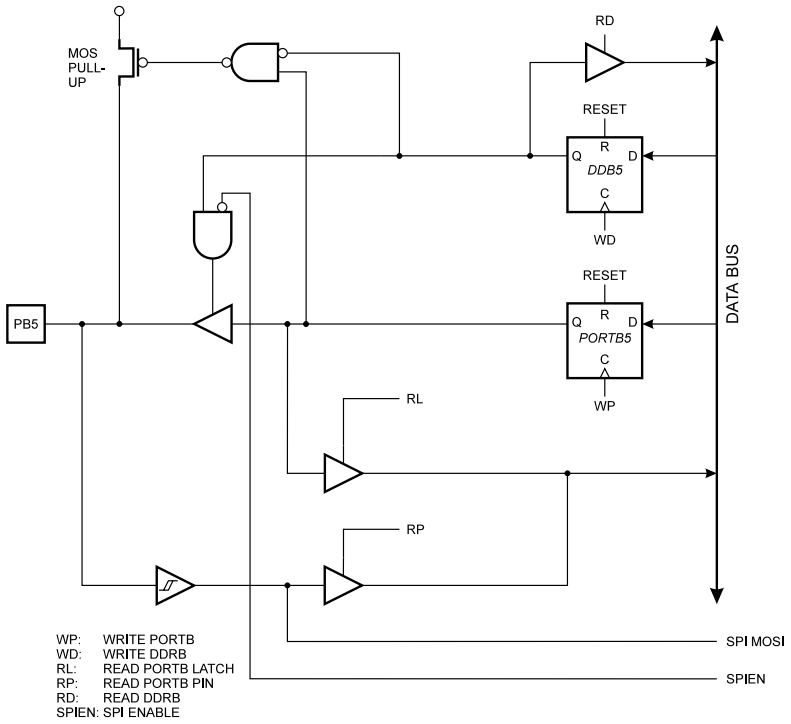


Figure 28. Port D Schematic Diagram (Pin PD2)

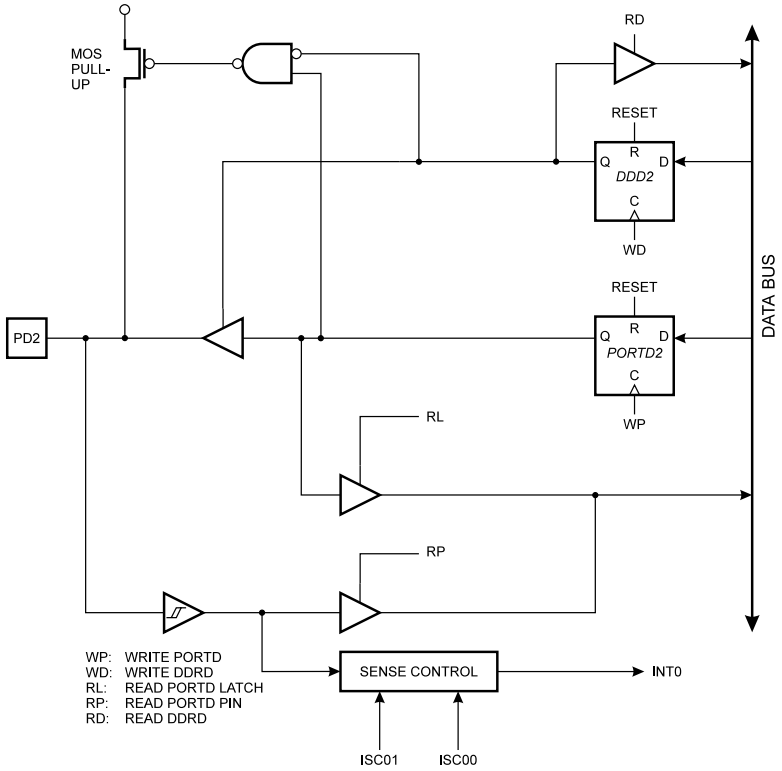
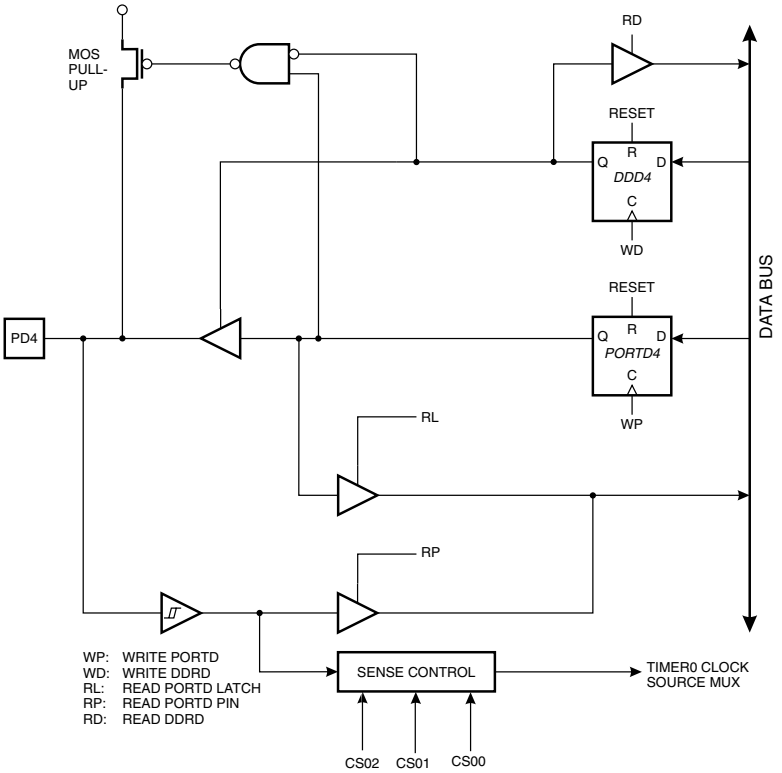


Figure 29. Port D Schematic Diagram (Pin PD4)



the self-timed write instruction in the Serial Programming mode. During programming, the supply voltage must be in accordance with Table 13.

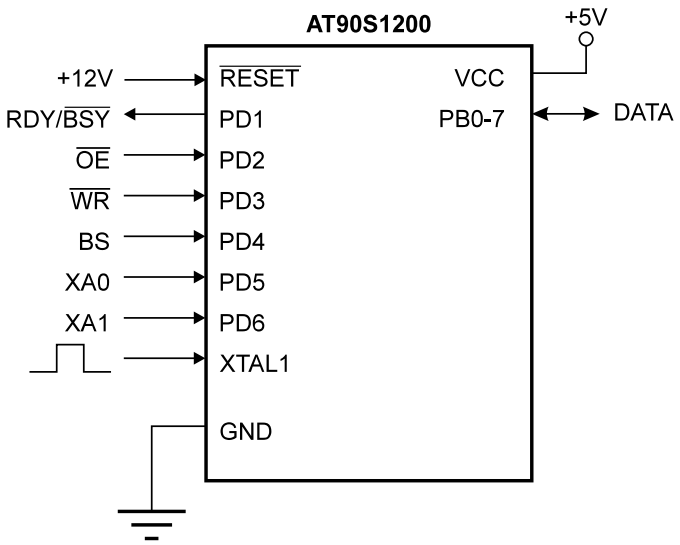
Table 13. Supply Voltage during Programming

Part	Serial Programming	Parallel Programming
AT90S1200	2.7 - 6.0V	4.5 - 5.5V

Parallel Programming

This section describes how to parallel program and verify Flash program memory, EEPROM data memory, Lock bits and Fuse bits in the AT90S1200.

Figure 30. Parallel Programming



Signal Names

In this section, some pins of the AT90S1200 are referenced by signal names describing their function during parallel programming rather than their pin names, see Figure 30 and Table 14. Pins not described in Table 14 are referenced by pin names.

The XA1/XA0 pins determines the action executed when the XTAL1 pin is given a positive pulse. The coding is shown in Table 15.

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The command is a byte where the different bits are assigned functions as shown in Table 16.

Table 14. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/$\overline{BSY}$	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active low)
$\overline{WR}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select (“0” selects low byte, “1” selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PB0-7	I/O	Bi-directional Data Bus (Output when $\overline{OE}$ is low)

Table 15. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (High or low address byte for Flash determined by BS).
0	1	Load Data (High or low data byte for Flash determined by BS).
1	0	Load Command
1	1	No Action, Idle

Table 16. Command Byte Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Fuse and Lock Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in Parallel Programming mode:

1. Apply supply voltage according to Table 13, between V_{CC} and GND.
2. Set the $\overline{\text{RESET}}$ and BS pin to “0” and wait at least 100 ns.
3. Apply 11.5 - 12.5V to $\overline{\text{RESET}}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{\text{RESET}}$, will cause the device to fail entering Programming mode.

Chip Erase

The Chip Erase command will erase the Flash and EEPROM memories, and the Lock bits. The Lock bits are not Reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

Load Command “Chip Erase”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “1000 0000”. This is the command for Chip Erase.
4. Give XTAL1 a positive pulse. This loads the command.
5. Give $\overline{\text{WR}}$ a t_{WLWH_CE} wide negative pulse to execute Chip Erase, t_{WLWH_CE} is found in Table 17. Chip Erase does not generate any activity on the RDY/$\overline{\text{BSY}}$ pin.

Programming the Flash

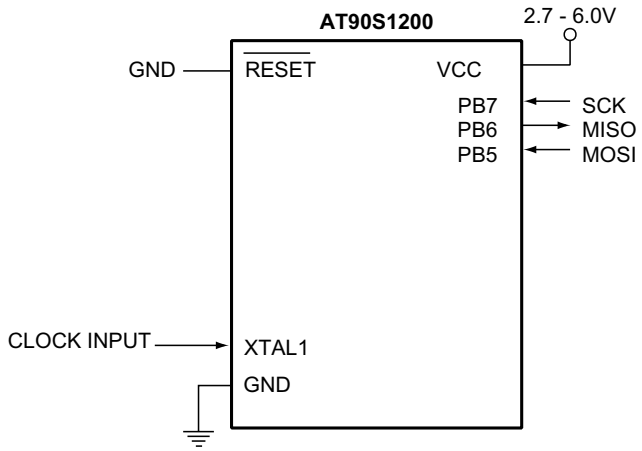
A: Load Command “Write Flash”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “0001 0000”. This is the command for Write Flash.

Serial Downloading

Both the program and data memory arrays can be programmed using the SPI bus while $\overline{\text{RESET}}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output) (see Figure 34). After $\overline{\text{RESET}}$ is set low, the Programming Enable instruction needs to be executed first before program/erase instructions can be executed.

Figure 34. Serial Programming and Verify



Note: If the device is clocked by the Internal Oscillator, it is no need to connect a clock source to the XTAL1 pin

For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the Program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $01FF for Flash program memory and $000 to $03F for EEPROM data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The minimum low and high periods for the Serial Clock (SCK) input are defined as follows:

Low: > 1 XTAL1 clock cycle

High: > 4 XTAL1 clock cycles

Serial Programming Algorithm

When writing serial data to the AT90S1200, data is clocked on the rising edge of SCK.

When reading data from the AT90S1200, data is clocked on the falling edge of SCK. See Figure 35 and Table 20 for timing details.

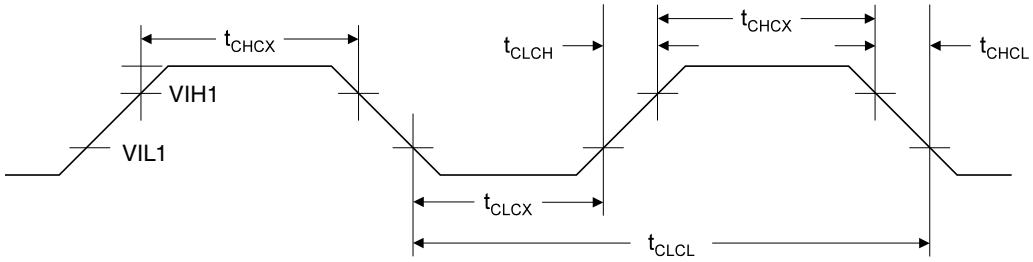
To program and verify the AT90S1200 in the Serial Programming mode, the following sequence is recommended (See 4-byte instruction formats in Table 17):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to “0”. If a crystal is not connected across pins XTAL1 and XTAL2 or the device is not running from the Internal RC Oscillator, apply a clock signal to the XTAL1 pin. If the programmer can not guarantee that SCK is held low during power-up, $\overline{\text{RESET}}$ must be given a positive pulse after SCK has been set to “0”.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB5) pin.

External Clock Drive Waveforms

Figure 37. External Clock Drive



External Clock Drive

Table 23. External Clock Drive

Symbol	Parameter	V_{CC} = 2.7V to 4.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	4.0	0	12.0	MHz
t_{CLCL}	Clock Period	250.0		83.3		ns
t_{CHCX}	High Time	100.0		33.3		ns
t_{CLCX}	Low Time	100.0		33.3		ns
t_{CLCH}	Rise Time		1.6		0.5	µs
t_{CHCL}	Fall Time		1.6		0.5	µs

Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

The power consumption in Power-down mode is independent of clock selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L \bullet V_{CC} \bullet f$ where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

Figure 38. Active Supply Current vs. Frequency

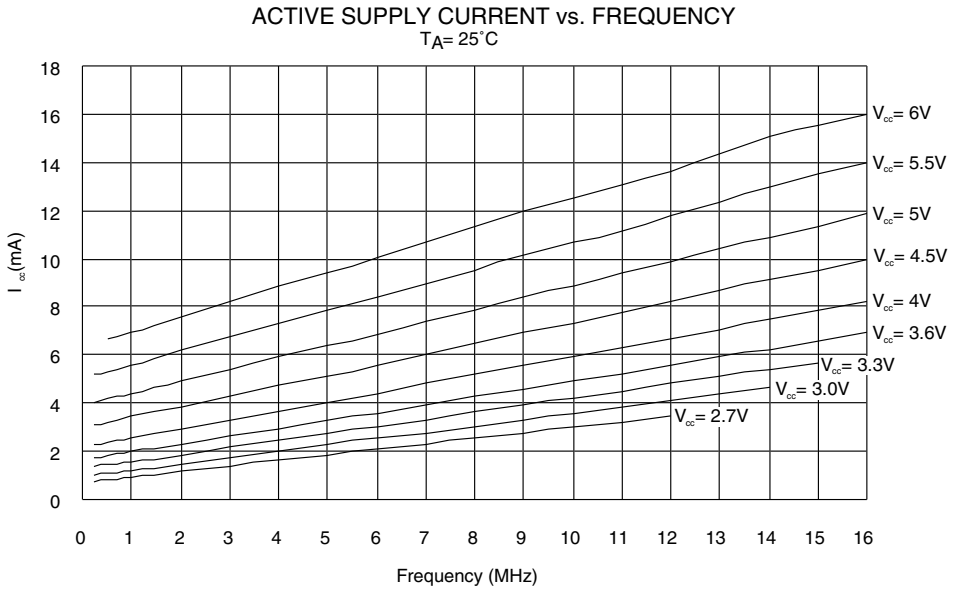


Figure 43. Idle Supply Current vs. V_{CC}, Device Clocked by Internal Oscillator

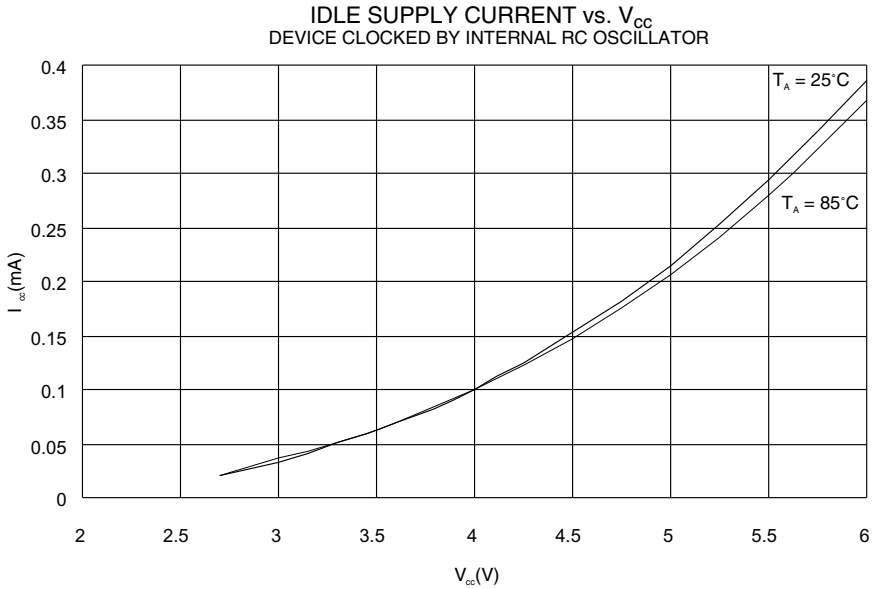


Figure 44. Power-down Supply Current vs. V_{CC}, Watchdog Timer Disabled

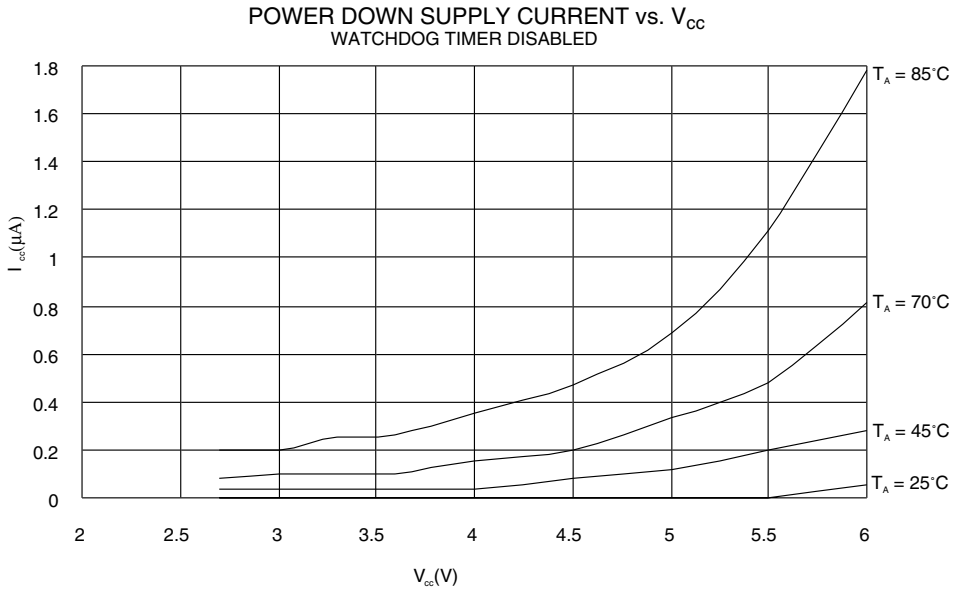


Figure 55. I/O Pin Sink Current vs. Output Voltage

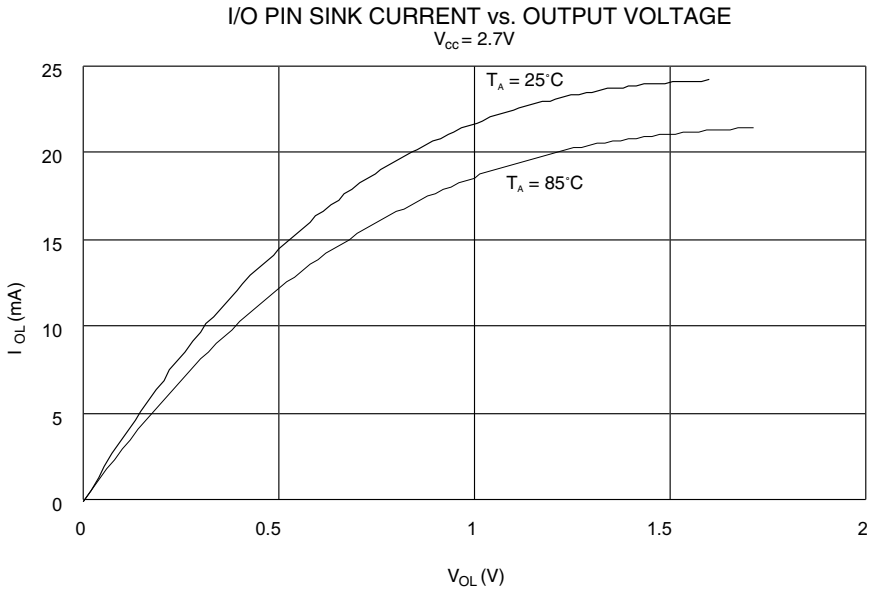
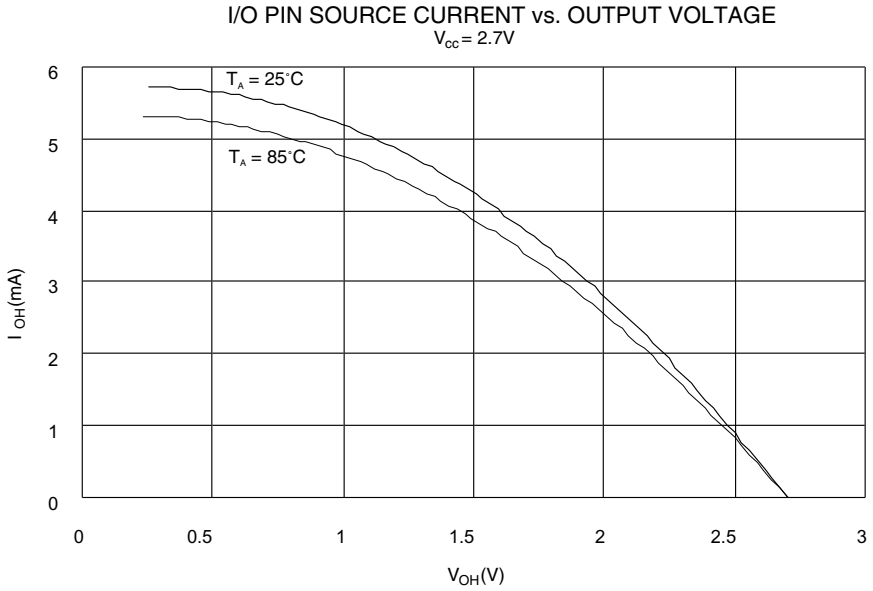
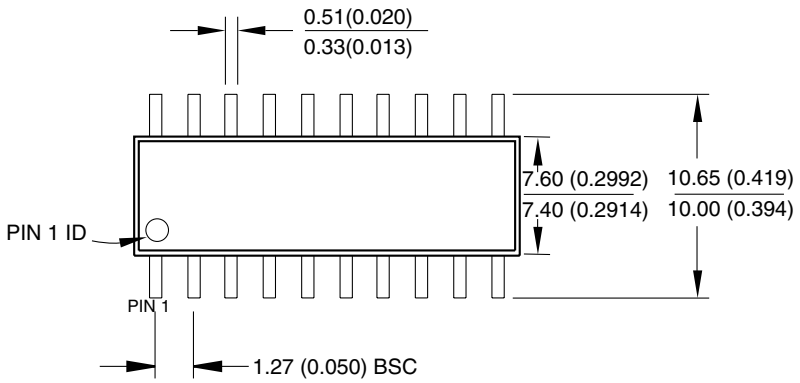


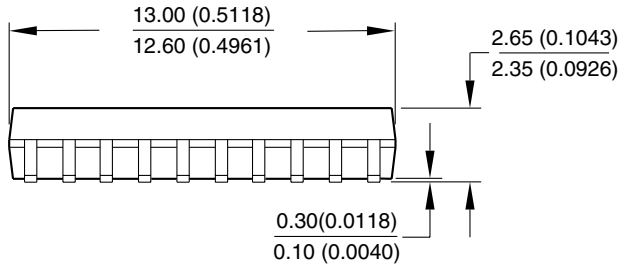
Figure 56. I/O Pin Source Current vs. Output Voltage

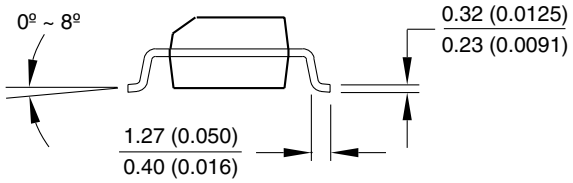


20S

20S, 20-lead, Plastic Gull Wing Small Outline (SOIC), 0.300" body.
Dimensions in Millineters and (Inches)*
JEDEC STANDARD MS-013







*Controlling dimension: Inches

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