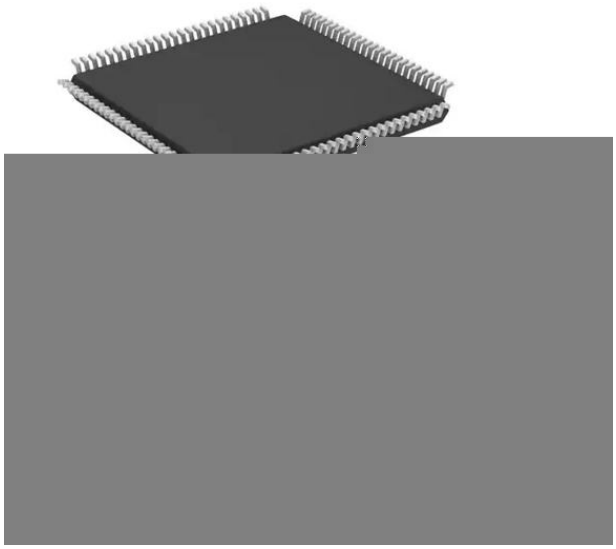


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56307cdfp-v0

Table 1.1 Outline of Specifications (5/5)

Classification	Module/Function	Description
10-bit A/D converter (ADb)		x1 unit (1 unit × 8 channels) x10-bit resolution xConversion time: 1.0 µs per channel (in operation with PCLK at 50 MHz) xOperating mode Scan mode (single scan mode or continuous scan mode) External amplifier connection mode xSample-and-hold function xThree ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		x2 channels x10-bit resolution xOutput voltage: 0 V to VREFH
Temperature sensor		x1 channel xPrecision: ± 1 ºC xThe voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		xCRC code generation for arbitrary amounts of data in 8-bit units xSelect any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. xGeneration of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, Vbatt = 2.3 to 3.6 V
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Package		177-pin TFLGA (PTLG0177KA-A) (in planning) 176-pin LFBGA (PLBG0176GA-A) (in planning) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) (in planning) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100KA-A) (in planning) 100-pin LQFP (PLQP0100KB-A) 80-pin LQFP (PLQP0080KB-A) (in planning)
On-chip debugging system		xE1 emulator (JTAG and FINE interfaces) xE20 emulator (JTAG interface)

Note 1. Please contact us if you are using a G version.

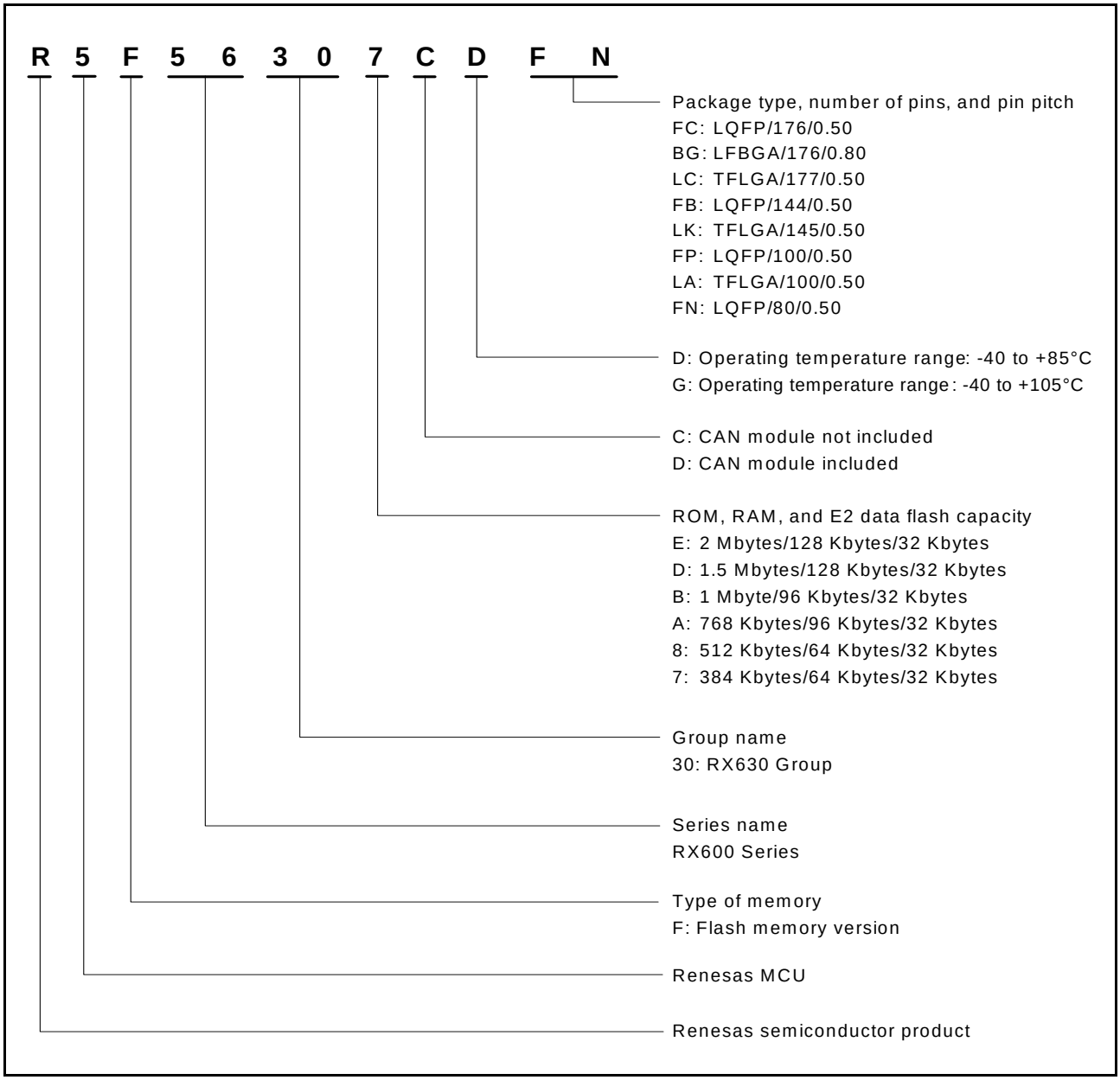


Figure 1.1 How to Read the Product Part Number

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	x Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	x Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	x Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	x Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
I^2C bus interface	SCL0[FM+], SCL1 to SCL3	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1 to SDA3	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain
USB power pins	VCC_USB	Input	Power supply pin. When the USB is not to be used, connect it to the VCC pin.
	VSS_USB	Input	Ground pin. When the USB is not to be used, connect it to the VSS pin.
USB 2.0 function module	USB0_DP	I/O	Inputs or outputs D+ data for the USB bus
	USB0_DM	I/O	Inputs or outputs D- data for the USB bus
	USB0_DPUPE	Output	Pull-up pin
	USB0_VBUS	Input	Input pin for detection of connection and disconnection of the USB cable
CAN module	CRX0 to CRX2	Input	Input pins
	CTX0 to CTX2	Output	Output pins
Serial peripheral interface	RSPCKA, RSPCKB RSPCKC	I/O	Clock input/output pins
	MOSIA, MOSIB, MOSIC	I/O	Inputs or outputs data output from the master
	MISOA, MISOB, MISOC	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0, SSLC0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3 SSLC1 to SSLC3	Output	Output pins for slave selection
IEBus controller	IERXD	Input	Input pin for data reception
	IETXD	Output	Output pin for data transmission
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pin

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

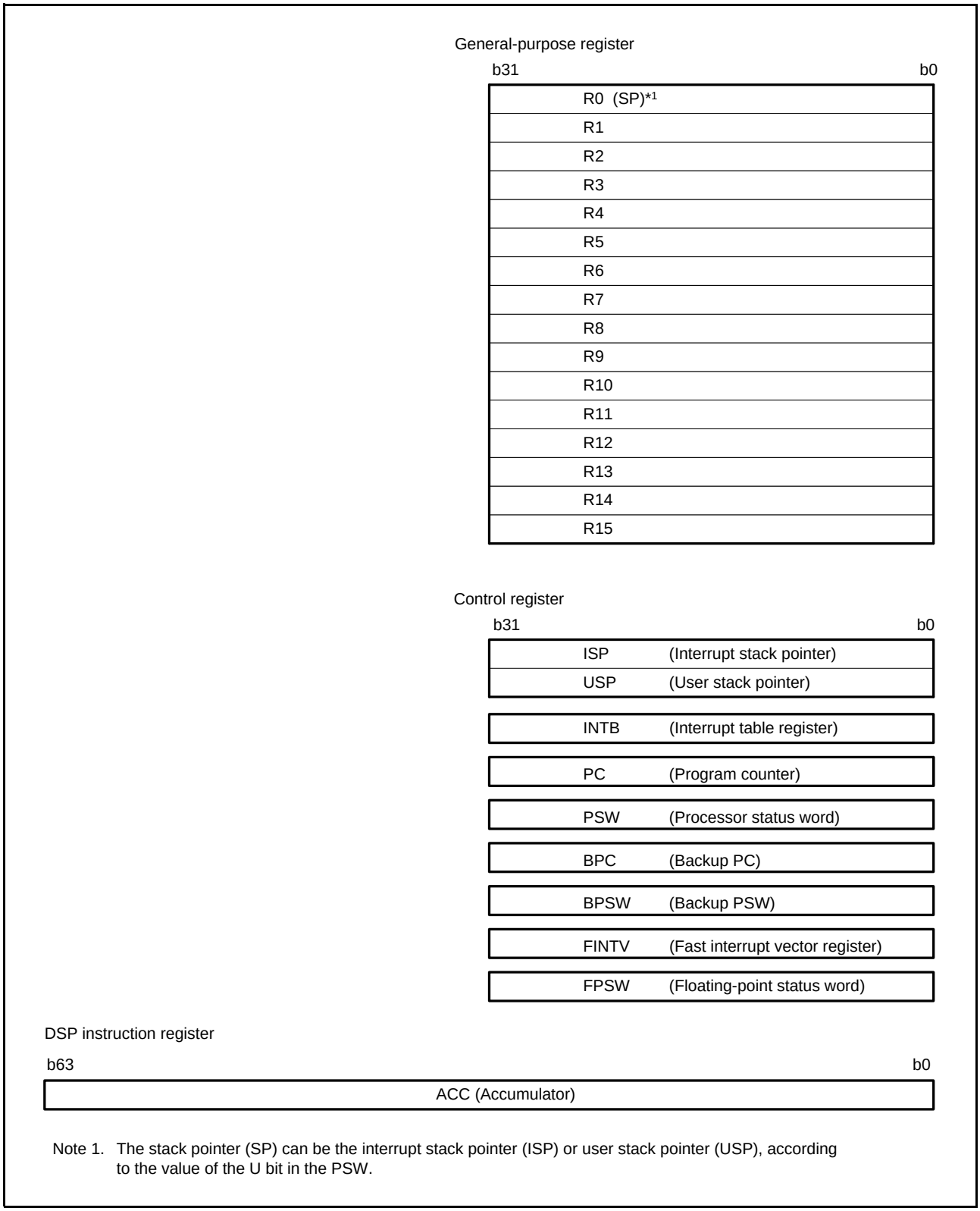
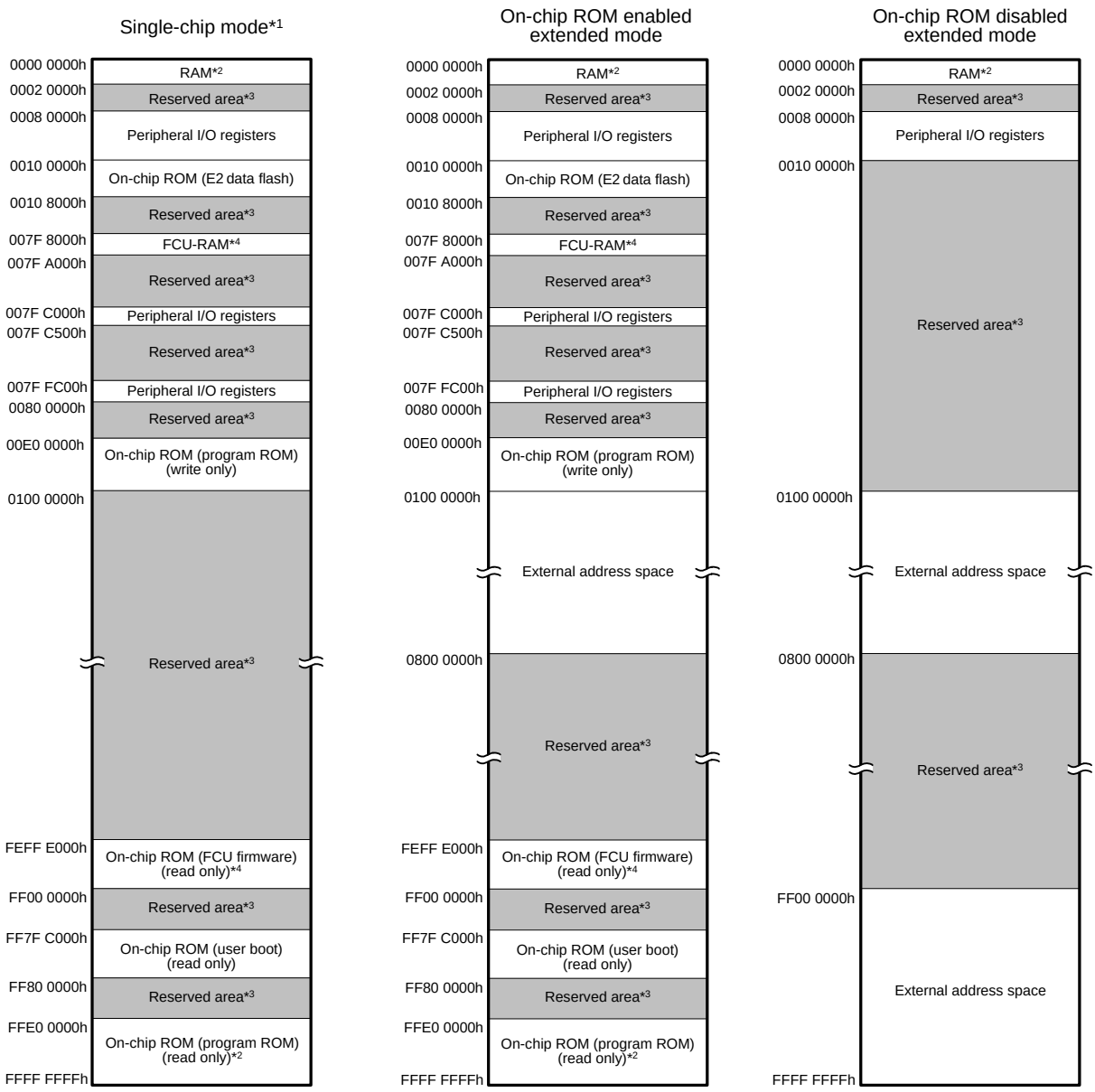


Figure 2.1 Register Set of the CPU



Note 1. The address space in boot mode and user boot mode/USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
2 M	FFE0 0000h to FFFF FFFFh	128 K	0000 0000h to 0001 FFFFh
1.5 M	FFE8 0000h to FFFF FFFFh		
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		

Note:See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
Note 4. For details on the FCU, see section 43, Flash Memory in the User's manual: Hardware.

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to eight CS areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) in on-chip ROM disabled extended mode.

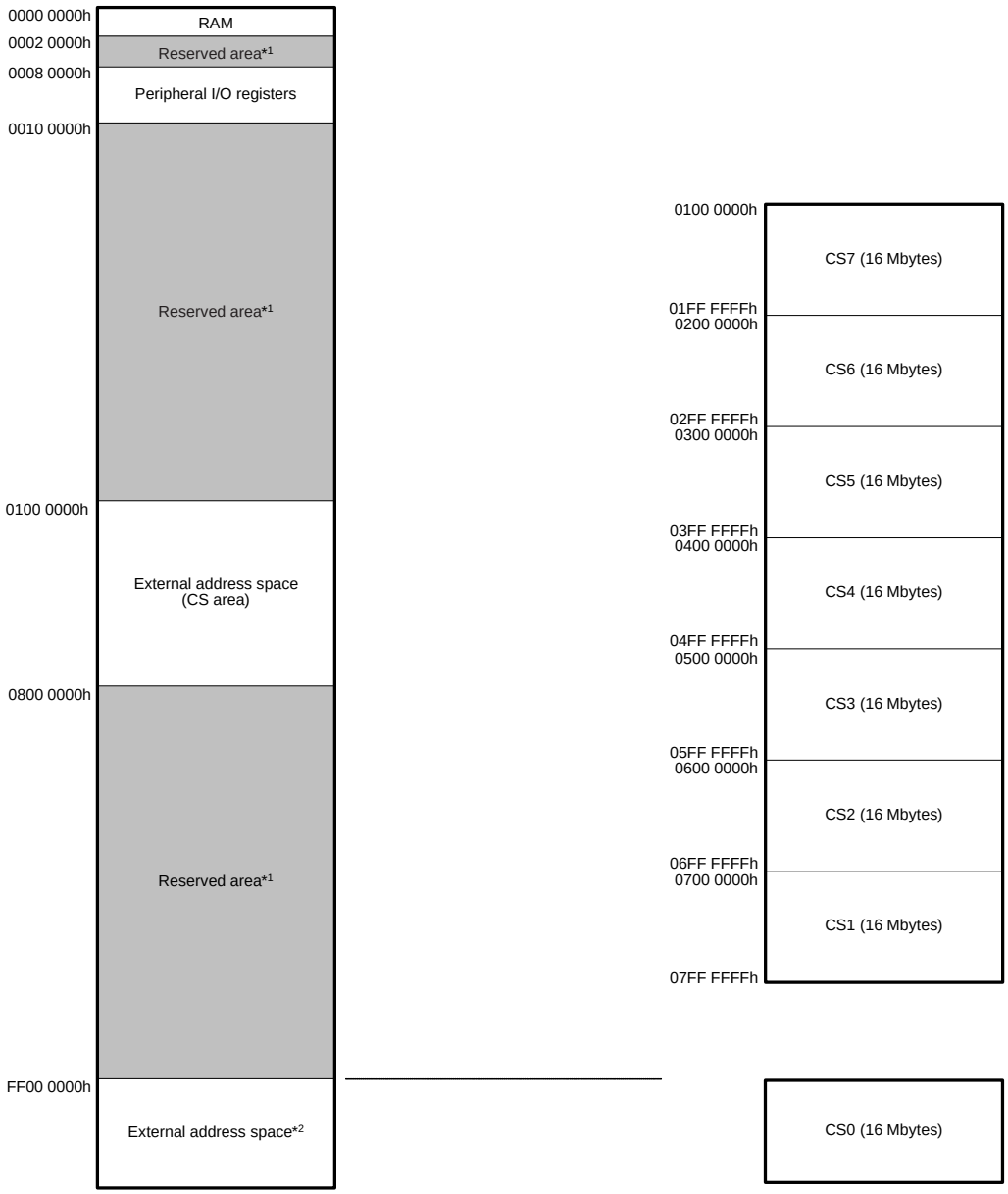


Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)