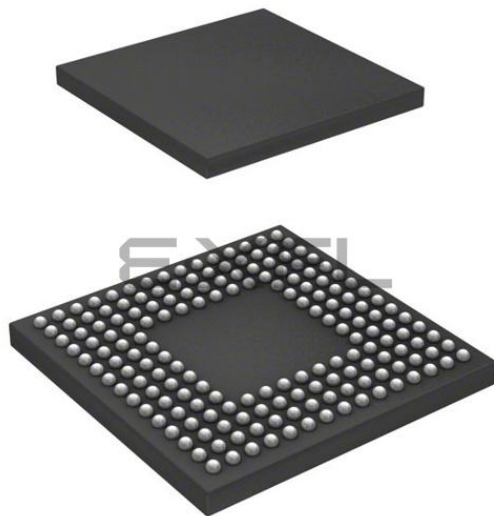




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	148
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630addbg-u0

Table 1.2 Comparison of Functions for Different Packages

Functions		RX630 Group			
Package		177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins	80 Pins
External bus	External bus width	32 bits	16 bits		Not supported
DMA	DMA controller	Ch. 0 to 3			
	Data transfer controller	Supported			
Timers	16-bit timer pulse unit	Ch. 0 to 11		Ch. 0 to 5	
	Multi-function timer pulse unit 2	Ch. 0 to 5			
	Port output enable 2	Supported			
	Programmable pulse generator	Ch. 0 and 1			
	8-bit timers	Ch. 0 to 3			
	Compare match timer	Ch. 0 to 3			
	Realtime clock	Supported			
	Watchdog timer	Supported			
	Independent watchdog timer	Supported			
Communication function	USB 2.0 function module	Ch. 0			
	Serial communications interfaces (SClc)	Ch. 0 to 11		Ch. 0 to 3, 5, 6, 8, 9	Ch. 1, 5, 6, 8, 9
	Serial communications interfaces (SCld)	Ch. 12			
	I ² C bus interfaces	Ch. 0 to 3		Ch. 0, 2	
	IEBus	Supported			
	Serial peripheral interfaces	Ch. 0 to 2		Ch. 0, 1	
	CAN module	For 1 M or less: Ch. 0, 1 For 1.5 M or more: Ch. 0 to 2		For 512 K or less: Ch. 1 For 768 K or more: Ch. 0, 1	Ch. 1
12-bit A/D converter		AN000 to 020		AN000 to 013	AN000 to 010
10-bit A/D converter		AN0 to 7			AN0 to 3
D/A converter		Ch. 0, 1		Ch. 1	
Temperature sensor		Supported			
CRC calculator		Supported			
Unique ID		Available (only for the G version)			

Table 1.3 List of Products (2/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX630 (D version)	R5F5630DDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDLK	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630EDDLK	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
RX630 (G version) *2	R5F5630BDGFB	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F5630ADGFB	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F5630BDGFP	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F5630ADGFP	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F56308DGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F56307DGFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F56308DGFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100MHz	-40 to +105°C
	R5F56307DGFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100MHz	-40 to +105°C

Note 1. The sub-clock oscillator, real-time clock, and boundary scan have different specifications. For details, see section 11.2.8, Sub-Clock Oscillator Wait Control Register (SOSCWTCR), section 28.2.19, RTC Control Register 3 (RCR3), and section 44.2.4, Boundary Scan Register (JTBSR) in the User's manual: Hardware.

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 41.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 41.3, Using the Temperature Sensor, and section 43.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

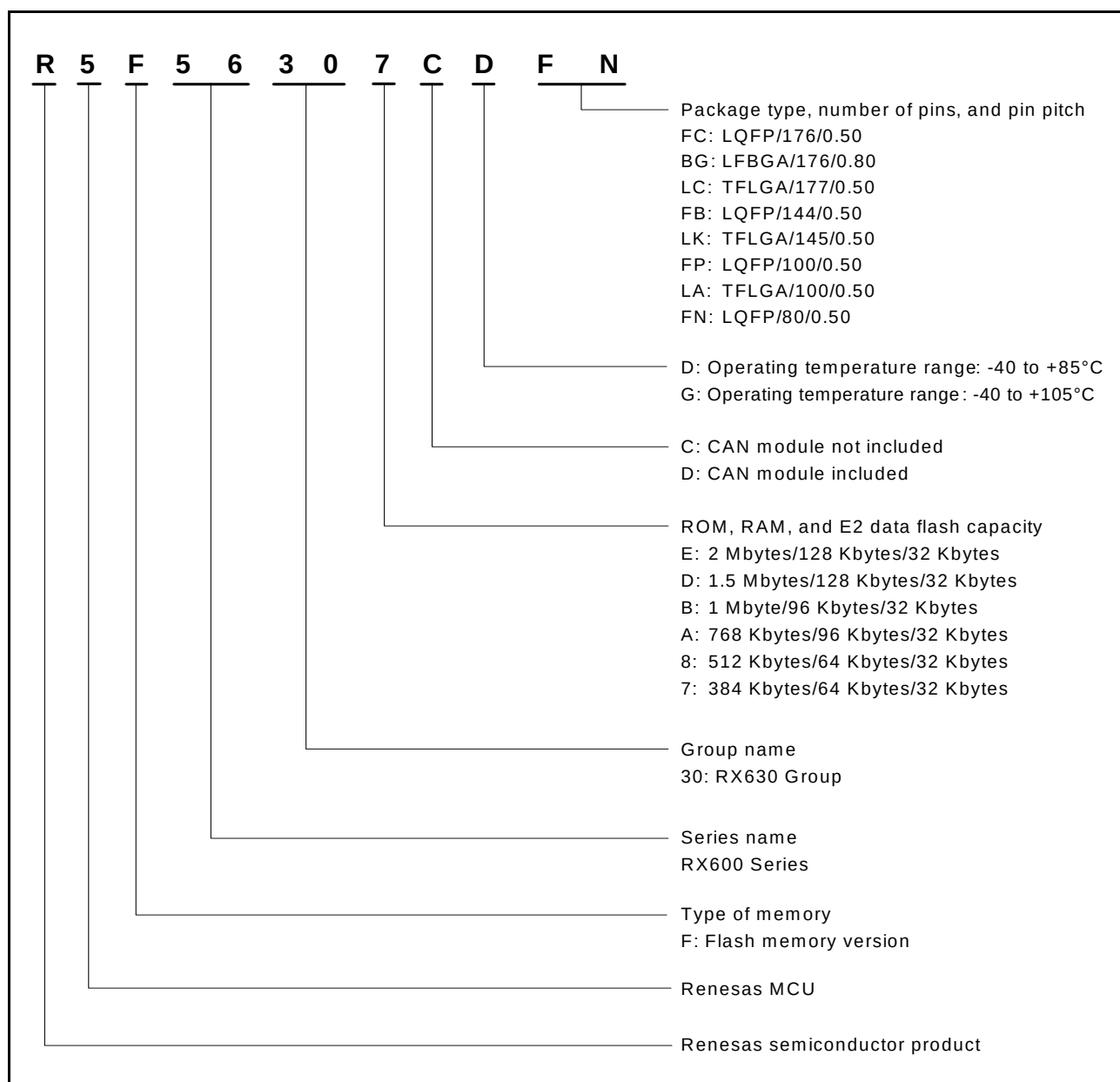


Figure 1.1 How to Read the Product Part Number

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
P7	VSS_USB						
P8		PL3					
P9		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
P10		P83		MTIOC4C	CTS10#/RTS10#/SS10#		
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
P13		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
P14		P75	CS5#	PO20	SCK11		
P15		PL1					
R1		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
R2		P20		MTIOC1A/TIOCB3/ TMR10/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS	IRQ6	ADTRG0#
R4		P85					
R5		P11		MTIC5V/TMC13	SCK2	IRQ1	
R6					USB0_DM		
R7					USB0_DP		
R8		PL4					
R9		P84					
R10	VSS						
R11	VCC						
R12		P80		MTIOC3B/PO26	SCK10		
R13		P76	CS6#	PO22	RXD11/SMISO11/SSCL11		
R14		P74	CS4#	PO19	CTS11#/RTS11#/SS11#		
R15		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3	IRQ12	

Note 1. The 176-pin LFBGA does not include the E5 pin.

Note 2. Enabled only for the ROM capacity: 2 MB/1.5 MB

Note 3. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (4/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCId, SCId, RSPI, RiIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
119	TRSYNC#	PG4	D28				
120		P67	CS7#		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
127		PK5			TXD4/SMOSI4/SSDA4		
128		P70			SCK4		
129		PK4			RXD4/SMISO4/SSCL4		
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOC0D/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
136		P64	CS4#				
137		P63	CS3#				
138		P62	CS2#				
139		P61	CS1#		CTS9#/RTS9#/SS9#		
140		PK3			RXD9/SMISO9/SSCL9		
141		P60	CS0#		SCK9		
142		PK2			TXD9/SMOSI9/SSDA9		
143		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
144		PG1	D25				
145		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
146		PG0	D24				
147		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
148		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
149		P97	A23/D23				
150		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011

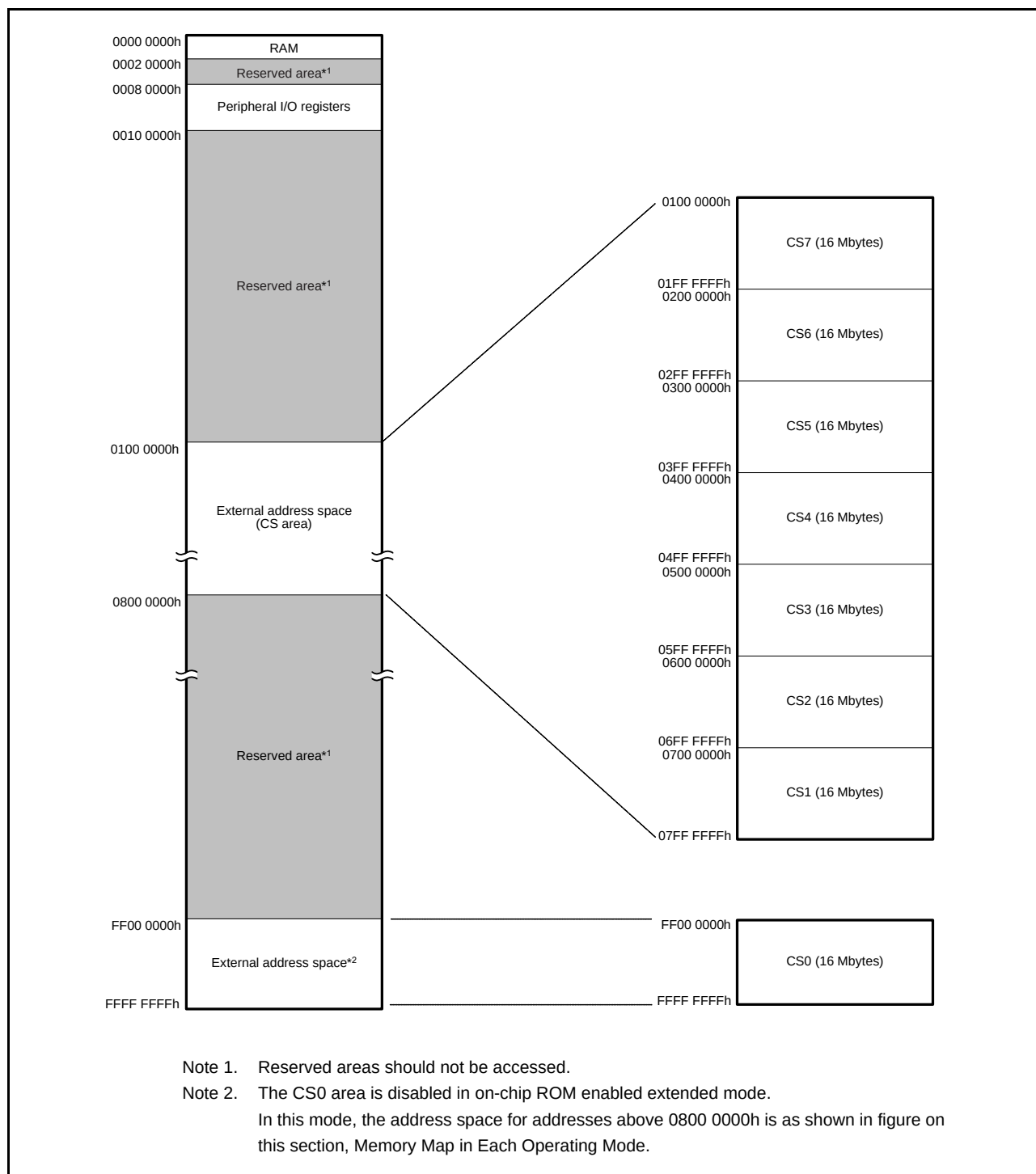
Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10		PK3			RXD9/SMISO9/SSCL9		
A11		P62	CS2#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10		PK2			TXD9/SMOSI9/SSDA9		
B11		P61	CS1#		CTS9#/RTS9#/SS9#		
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C1	VREFL						
C2		P02		TMCI1	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12		P70			SCK4		
C13		PK4			RXD4/SMISO4/SSCL4		
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019

3.2 External Address Space

The external address space is divided into up to eight CS areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral busses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

Table 4.1 List of I/O Registers (Address Order) (9/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 719Ah	ICU	DTC activation enable register 154	DTCER154	8	8	2 ICLK		ICUb
0008 719Bh	ICU	DTC activation enable register 155	DTCER155	8	8	2 ICLK		
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8	2 ICLK		
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2 ICLK		
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8	2 ICLK		
0008 719Fh	ICU	DTC activation enable register 159	DTCER159	8	8	2 ICLK		
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8	2 ICLK		
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8	2 ICLK		
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2 ICLK		
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2 ICLK		
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2 ICLK		
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2 ICLK		
0008 71AAh	ICU	DTC activation enable register 170	DTCER170	8	8	2 ICLK		
0008 71ABh	ICU	DTC activation enable register 171	DTCER171	8	8	2 ICLK		
0008 71ADh	ICU	DTC activation enable register 173	DTCER173	8	8	2 ICLK		
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK		
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK		
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK		
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK		
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK		
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK		
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK		
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK		
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK		
0008 71BFh	ICU	DTC activation enable register 191	DTCER191	8	8	2 ICLK		
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK		
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK		
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK		
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK		
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK		
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK		
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK		
0008 71D6h	ICU	DTC activation enable register 214	DTCER214	8	8	2 ICLK		
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK		
0008 71D9h	ICU	DTC activation enable register 217	DTCER217	8	8	2 ICLK		
0008 71DAh	ICU	DTC activation enable register 218	DTCER218	8	8	2 ICLK		
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK		
0008 71DDh	ICU	DTC activation enable register 221	DTCER221	8	8	2 ICLK		
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK		
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK		
0008 71E2h	ICU	DTC activation enable register 226	DTCER226	8	8	2 ICLK		
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK		
0008 71E5h	ICU	DTC activation enable register 229	DTCER229	8	8	2 ICLK		
0008 71E6h	ICU	DTC activation enable register 230	DTCER230	8	8	2 ICLK		
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK		
0008 71E9h	ICU	DTC activation enable register 233	DTCER233	8	8	2 ICLK		
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK		
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK		
0008 71EEh	ICU	DTC activation enable register 238	DTCER238	8	8	2 ICLK		
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (13/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK		ICUb
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK		
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK		
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK		
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK		
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK		
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK		
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK		
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK		
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK		
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK		
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK		
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK		
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	8	8	2 ICLK		
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	8	8	2 ICLK		
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK		
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK		
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK		
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK		
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK		
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8	2 ICLK		
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTa
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C0h	DA	D/A data register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa
0008 80C2h	DA	D/A data register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	
0008 80C4h	DA	D/A control register	DACR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C5h	DA	DADRm format select register	DADPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C6h	DA	D/A A/D synchronous start control register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8100h	TPUA	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa

Table 4.1 List of I/O Registers (Address Order) (20/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 83C3h	RSPI2	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 83C4h	RSPI2	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83C8h	RSPI2	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C9h	RSPI2	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CAh	RSPI2	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CBh	RSPI2	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CCh	RSPI2	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83CDh	RSPI2	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CEh	RSPI2	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CFh	RSPI2	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83D0h	RSPI2	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83D2h	RSPI2	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83D4h	RSPI2	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83D6h	RSPI2	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83D8h	RSPI2	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83DAh	RSPI2	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83DCh	RSPI2	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83DEh	RSPI2	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK	
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK	
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK	
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (23/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	S12ADa
0008 9034h	S12AD	A/D data register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	
0008 9036h	S12AD	A/D data register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	
0008 9038h	S12AD	A/D data register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	
0008 903Ah	S12AD	A/D data register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	
0008 903Ch	S12AD	A/D data register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	
0008 903Eh	S12AD	A/D data register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	
0008 9040h	S12AD	A/D data register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	
0008 9042h	S12AD	A/D data register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	
0008 9044h	S12AD	A/D data register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	
0008 9046h	S12AD	A/D data register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	
0008 9048h	S12AD	A/D data register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	
0008 9060h	S12AD	A/D sampling state register 01	ADSSTR01	16	16	2, 3 PCLKB	2 ICLK	
0008 9070h	S12AD	A/D sampling state register 23	ADSSTR23	16	16	2, 3 PCLKB	2 ICLK	
0008 9800h	AD	A/D data register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK	ADb
0008 9802h	AD	A/D data register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK	
0008 9804h	AD	A/D data register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK	
0008 9806h	AD	A/D data register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK	
0008 9808h	AD	A/D data register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK	
0008 980Ah	AD	A/D data register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK	
0008 980Ch	AD	A/D data register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK	
0008 980Eh	AD	A/D data register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK	
0008 9810h	AD	A/D control/status register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 9811h	AD	A/D control register	ADCR	8	8	2, 3 PCLKB	2 ICLK	
0008 9812h	AD	A/D control register 2	ADCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 9813h	AD	A/D sampling state register	ADSSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 981Fh	AD	A/D self-diagnostic register	ADDIAGR	8	8	2, 3 PCLKB	2 ICLK	
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCId, SCId
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A009h	SCI0	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ah	SCI0	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Bh	SCI0	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ch	SCI0	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (37/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 2848h	CAN2	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ah	CAN2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Bh	CAN2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ch	CAN2	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 284Dh	CAN2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Eh	CAN2	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Fh	CAN2	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 2850h	CAN2	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2851h	CAN2	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2852h	CAN2	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2853h	CAN2	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 2854h	CAN2	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2856h	CAN2	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2858h	CAN2	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0036h	USB0	BRDY interrupt status register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0038h	USB0	NRDY interrupt status register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	

Table 4.1 List of I/O Registers (Address Order) (42/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*9	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*9	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*9	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*9	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*9	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*9	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*9	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*9	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*9	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*9	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*9	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*9	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*9	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*9	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*9	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*9	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*9	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*9	TSCDRH	8	8	1 ICLK	1 ICLK	

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRH address is 000881EDh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FDh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.

Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 26.4 lists register allocation for 16-bit access in the User's manual: Hardware.

Note 6. The CAN2 module is not provided in products less than 1 Mbyte of ROM.

Note 7. The CAN0 module is not provided in products less than 512 Kbytes of ROM.

Note 8. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 9. These registers are only present in the G version.

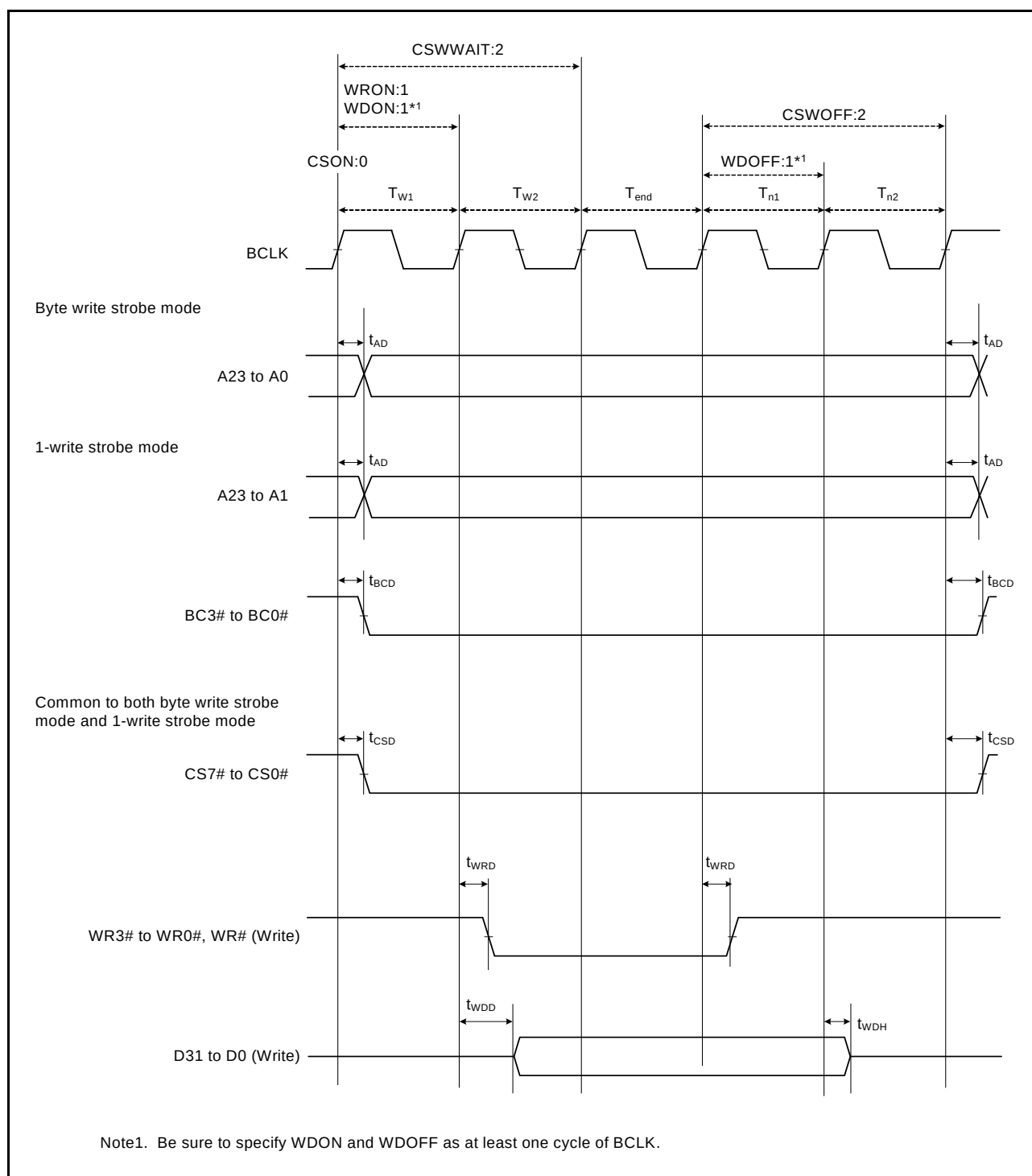


Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

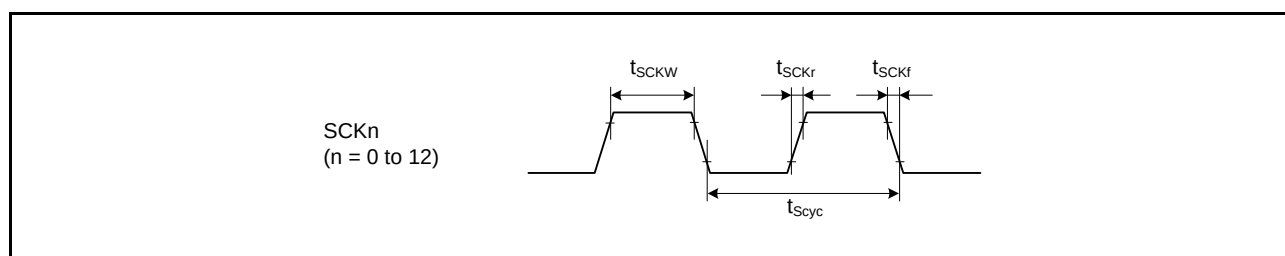


Figure 5.29 SCK Clock Input Timing

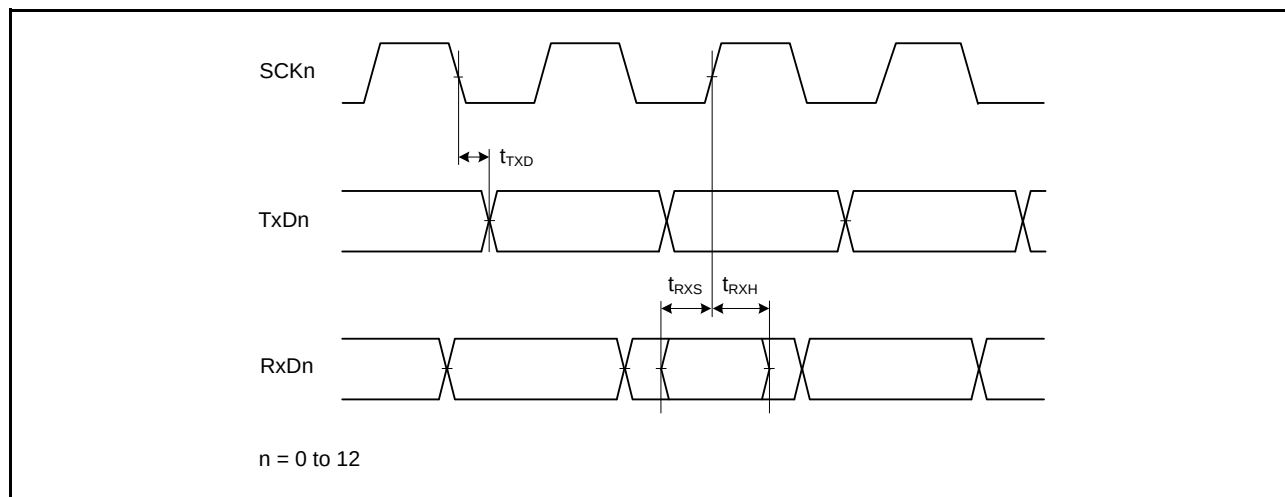


Figure 5.30 SCI Input/Output Timing: Clock Synchronous Mode

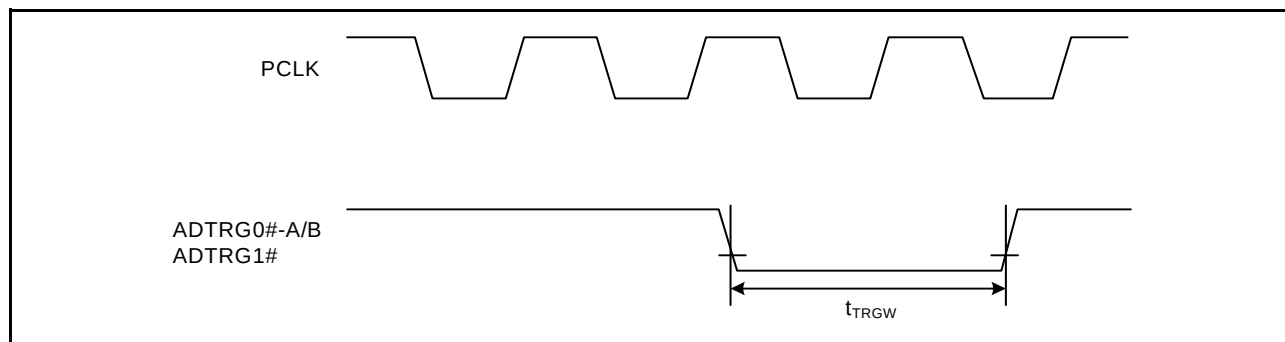


Figure 5.31 A/D Converter External Trigger Input Timing

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.30 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 Temperature range for the programming/erasure operation: $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30^{*2}	—	—	Year	$T_a = +85^{\circ}\text{C}$

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.31 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 Temperature range for the programming/erasure operation: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{PEC} \leq 100$ times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time $N_{PEC} > 100$ times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time $N_{PEC} \leq 100$ times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time $N_{PEC} > 100$ times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	μs

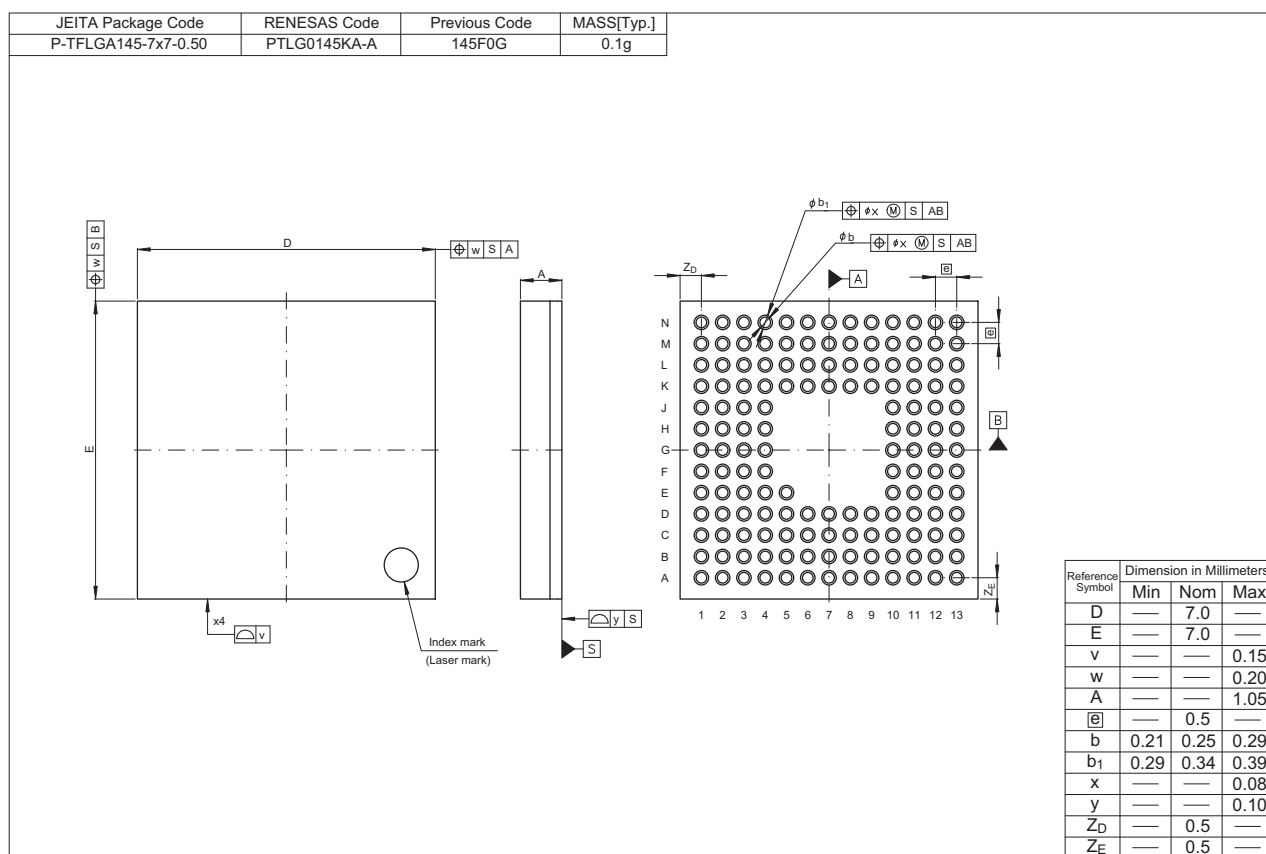


Figure D 145-Pin TFLGA (PTLG0145KA-A)

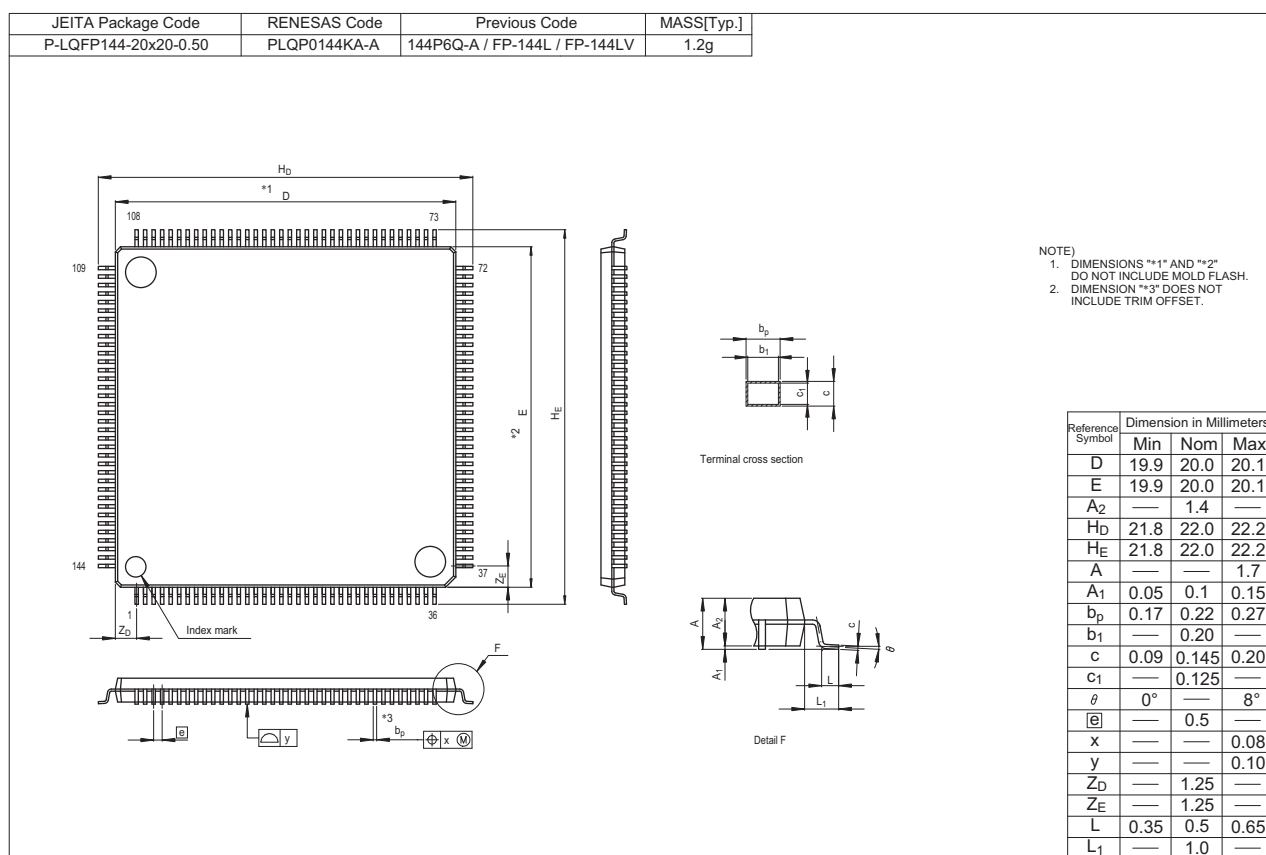


Figure E 144-Pin LQFP (PLQP0144KA-A)