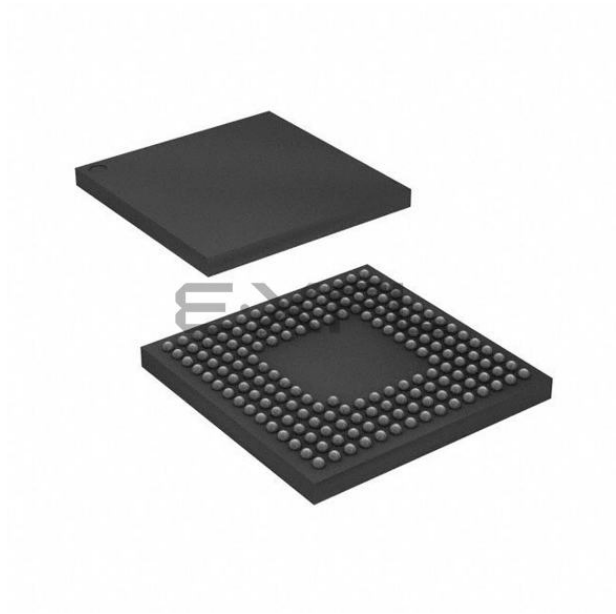
Renesas Electronics America Inc - R5F5630ADDLC#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	148
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630addlc-u0

Table 1.1 Outline of Specifications (2/5)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode • Battery backup function
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: 180 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, 16- or 32-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions
I/O ports	General I/O port pins	• 177-pin TFLGA (in planning), 176-pin LFBGA (in planning), 176-pin LQFP I/O pins: 148 Input pin: 1 Pull-up resistors: 148 Open-drain outputs: 148 5-V tolerance: 54 • 145-pin TFLGA (in planning), 144-pin LQFP I/O pins: 117 Input pin: 1 Pull-up resistors: 117 Open-drain outputs: 117 5-V tolerance: 53 • 100-pin TFLGA (in planning), 100-pin LQFP I/O pins: 78 Input pin: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 44 • 80-pin LQFP (in planning) I/O pins: 58 Input pin: 1 Pull-up resistors: 58 Open-drain outputs: 58 5-V tolerance: 34

Table 1.1 Outline of Specifications (5/5)

Classification	Module/Function	Description
10-bit A/D converter (ADb)		• 1 unit (1 unit × 8 channels) • 10-bit resolution • Conversion time: 1.0 µs per channel (in operation with PCLK at 50 MHz) • Operating mode Scan mode (single scan mode or continuous scan mode) External amplifier connection mode • Sample-and-hold function • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
Temperature sensor		• 1 channel • Precision: ± 1 ºC • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, Vbatt = 2.3 to 3.6 V
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Package		177-pin TFLGA (PTLG0177KA-A) (in planning) 176-pin LFBGA (PLBG0176GA-A) (in planning) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) (in planning) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100KA-A) (in planning) 100-pin LQFP (PLQP0100KB-A) 80-pin LQFP (PLQP0080KB-A) (in planning)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact us if you are using a G version.

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VSS	Input	Ground pin. Connect it to the system power supply (0 V)
	VBATT	Input	Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices
	XCOUT	Output	Input/output pins for the sub-clock oscillator circuit. Connect a crystal resonator between XCOUT and XCIN
	XCIN	Input	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on these pins must not be changed during operation
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid
	TRDATA0 to TRDATA3	Output	These pins output the trace information
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

1.5 Pin Assignments

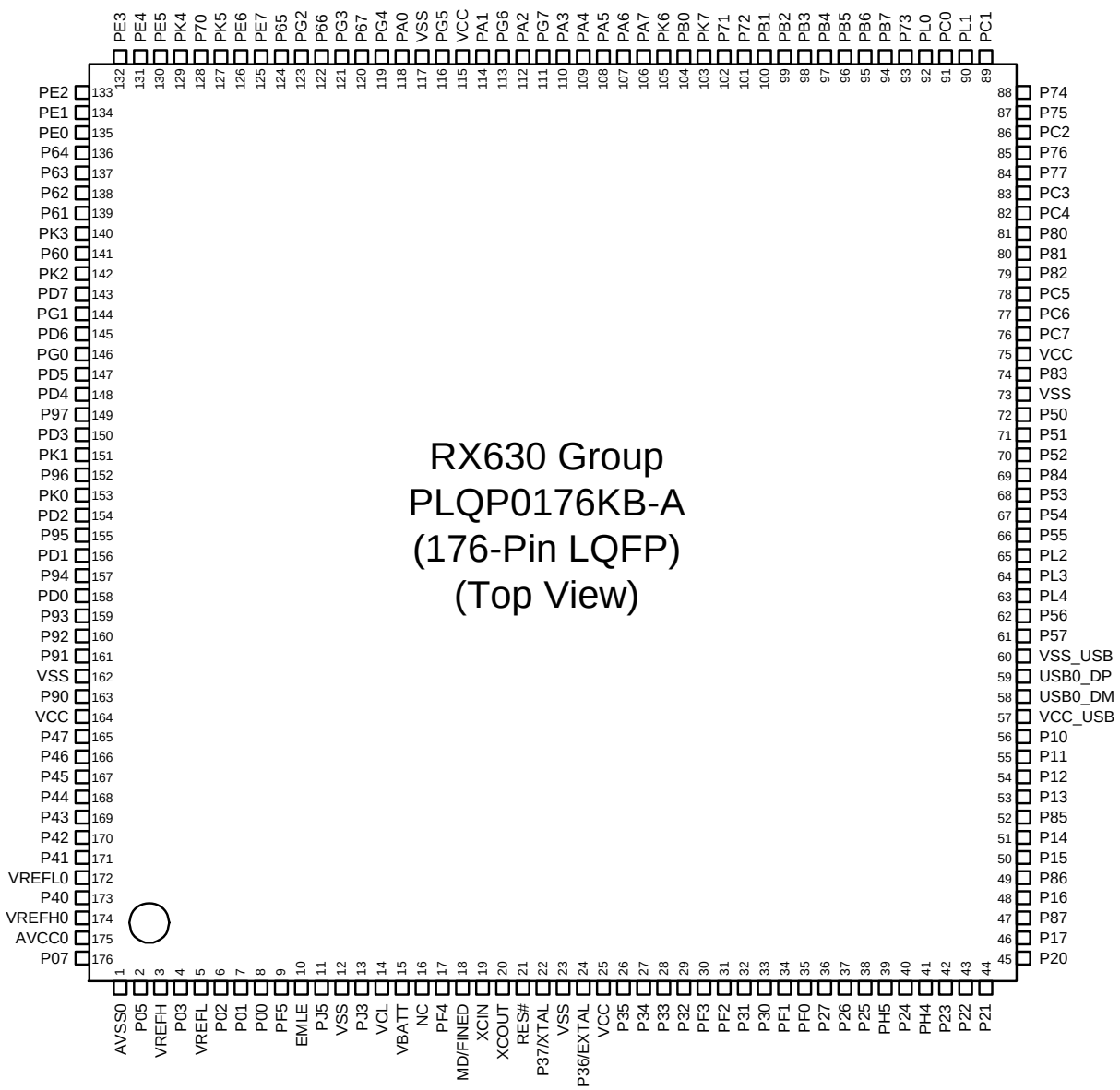
Figure 1.3 to Figure 1.10 show the pin assignments. Table 1.5 to Table 1.11 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	PL0	PL1	PC1	15
14	PE1	PE0	PK4	PE7	PG3	PA0	PA1	PA2	PA7	PK7	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	PK5	PG2	PG4	PG6	PA3	PK6	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	PK3	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	PK2	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	PK0	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	PK1								P53	PL2	PL3	PL4	8
7	VSS	P92	PD0	P95								P54	P55	VSS_ USB	USB0_ DP	7
6	VCC	P91	P90	P93								P56	P57	VCC_ USB	USB0_ DM	6
5	P46	P47	P45	P44	NC							P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	PH5	PH4	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX630 Group
PTLG0177KA-A
(177-Pin TFLGA)
(Upper perspective view)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (176-Pin LQFP).

Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C14		PK4			RXD4/SMISO4/SSCL4		
C15		P70			SCK4		
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8		PK1					
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#		CTS9#/RTS9#/SS9#		
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
D13		PK5			TXD4/SMOSI4/SSDA4		
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#		CRX2*2	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#		CTX2*2		
F13	TRSYNC#	PG4	D28				
F14		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
G15	VCC						

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (1/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	NC						
17	TRST#	PF4					
18	MD/FINED						
19	XCIN						
20	XCOUT						
21	RES#						
22	XTAL	P37					
23	VSS						
24	EXTAL	P36					
25	VCC						
26		P35				NMI	
27		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
28		P33		MTIOC0D/TIOCD0/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOUT/RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
30	TMS	PF3					
31	TDI	PF2			RXD1/SMISO1/SSCL1		
32		P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
33		P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
34	TCK/FINEC	PF1			SCK1		
35	TDO	PF0			TXD1/SMOSI1/SSDA1		
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
38		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
39		PH5					
40		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	MD/FINED						
17	XCIN						
18	XCOUT						
19	RES#						
20	XTAL	P37					
21	VSS						
22	EXTAL	P36					
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
26		P33		MTIOC0D/TIOCD0/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
27		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOUT/RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
29	TDI	P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
30	TCK/FINEC	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
32		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
33		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
34		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
35		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
36		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK		
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK		
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK		
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK		
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK		
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK		
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0024h	SYSTEM	System clock control register 2	SCKCR2	16	16	3 ICLK		
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16	3 ICLK		
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16	3 ICLK		
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8	3 ICLK		
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8	3 ICLK		
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8	3 ICLK		
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8	3 ICLK		
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8	3 ICLK		
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8	3 ICLK		
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8	3 ICLK		
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8	3 ICLK		
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8	3 ICLK		
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8	3 ICLK		
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8	3 ICLK		
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8	3 ICLK		
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8	3 ICLK		
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16	3 ICLK		
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit control register 1	LVD1CR1	8	8	3 ICLK		LVDA
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit status register	LVD1SR	8	8	3 ICLK		
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit control register 1	LVD2CR1	8	8	3 ICLK		
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit status register	LVD2SR	8	8	3 ICLK		
0008 03FEh	SYSTEM	Protect register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK		
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK		
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK		
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16	2 ICLK		
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK		DMACA
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (6/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		ICUb
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK		
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK		
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK		
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK		
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK		
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK		
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK		
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK		
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK		
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2 ICLK		
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2 ICLK		
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK		
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK		
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2 ICLK		
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2 ICLK		
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK		
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK		
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2 ICLK		
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK		
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK		
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK		
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK		
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK		
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK		
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK		
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK		
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK		
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK		
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK		
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK		
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK		
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK		
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK		
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK		
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2 ICLK		
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2 ICLK		
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK		
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK		
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK		
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2 ICLK		
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK		
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK		
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK		
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK		
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK		
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2 ICLK		
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (22/42)

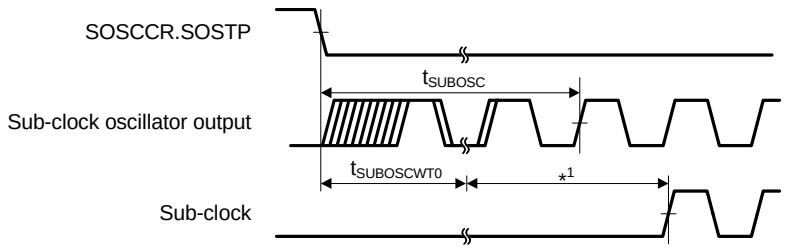
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK	
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK	
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK	
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK	
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK	
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK	
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK	
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK	
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK	
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK	
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE2a
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8908h	POE	Input level control/status register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK	
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	S12ADa
0008 9004h	S12AD	A/D channel select register 0	ADANS0	16	16	2, 3 PCLKB	2 ICLK	
0008 9006h	S12AD	A/D channel select register 1	ADANS1	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12AD	A/D-converted value addition mode select register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ah	S12AD	A/D-converted value addition mode select register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9012h	S12AD	A/D conversion extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (27/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A805h	IEB	IEBus slave address setting register 1	IESA1	8	8	3, 4 PCLKB	2, 3 ICLK	IEB
0008 A806h	IEB	IEBus slave address setting register 2	IESA2	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A807h	IEB	IEBus transmit message length register	IETBFL	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A809h	IEB	IEBus reception master address register 1	IEMA1	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A80Ah	IEB	IEBus reception master address register 2	IEMA2	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A80Bh	IEB	IEBus receive control field register	IERCTL	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A80Ch	IEB	IEBus receive message length register	IERBFL	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A80Eh	IEB	IEBus lock address register 1	IELA1	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A80Fh	IEB	IEBus lock address register 2	IELA2	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A810h	IEB	IEBus general flag register	IEFLG	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A811h	IEB	IEBus transmit status register	IETSR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A812h	IEB	IEBus transmit interrupt enable register	IEIET	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A814h	IEB	IEBus receive status register	IERSR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A815h	IEB	IEBus receive interrupt enable register	IEIER	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A818h	IEB	IEBus clock select register	IECKSR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A900h to 0008 A91Fh	IEB	IEBus transmit data buffer register 001 to 032	IETB001 to 032	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 AA00h to 0008 AA1Fh	IEB	IEBus receive data buffer register 001 to 032	IERB001 to 032	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 B300h	SCI12	Serial mode register	SMR12	8	8	3, 4 PCLKB	2, 3 ICLK	SCIc, SCId
0008 B301h	SCI12	Bit rate register	BRR12	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 B302h	SCI12	Serial control register	SCR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B303h	SCI12	Transmit data register	TDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B304h	SCI12	Serial status register	SSR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B305h	SCI12	Receive data register	RDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B306h	SCI12	Smart card mode register	SCMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B307h	SCI12	Serial extended mode register	SEMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B308h	SCI12	Noise filter setting register	SNFR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B309h	SCI12	I^2C mode register 1	SIMR112	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ah	SCI12	I^2C mode register 2	SIMR212	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Bh	SCI12	I^2C mode register 3	SIMR312	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ch	SCI12	I^2C status register	SIS12	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B320h	SCI12	Extended serial module enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK	
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK	
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B329h	SCI12	Control field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ah	SCI12	Control field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Bh	SCI12	Control field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (29/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C046h	PORT6	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C048h	PORT8	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C050h	PORTG	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C051h	PORTH	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C052h	PORTJ	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C053h	PORTK	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C054h	PORTL	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C070h	PORTG	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C073h	PORTK	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C074h	PORTL	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C080h	PORT0	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C081h	PORT0	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C088h	PORT4	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C089h	PORT4	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ah	PORT5	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Bh	PORT5	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ch	PORT6	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Dh	PORT6	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	



Note 1: This is the waiting period obtained by setting the SOCCWTCR.SSTS[4:0] bits.

Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.13 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t_{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

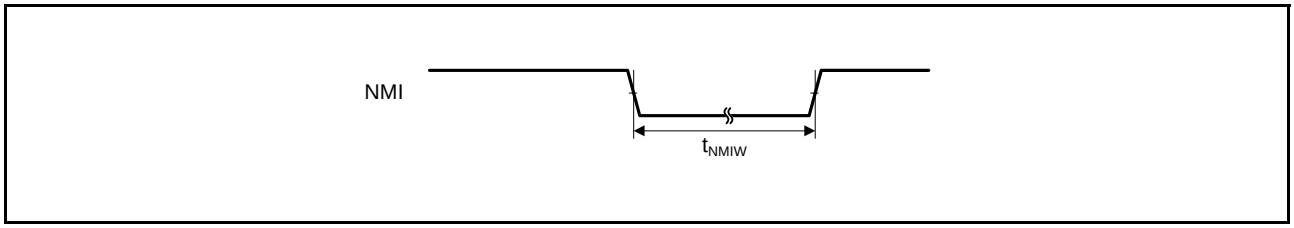


Figure 5.15 NMI Interrupt Input Timing

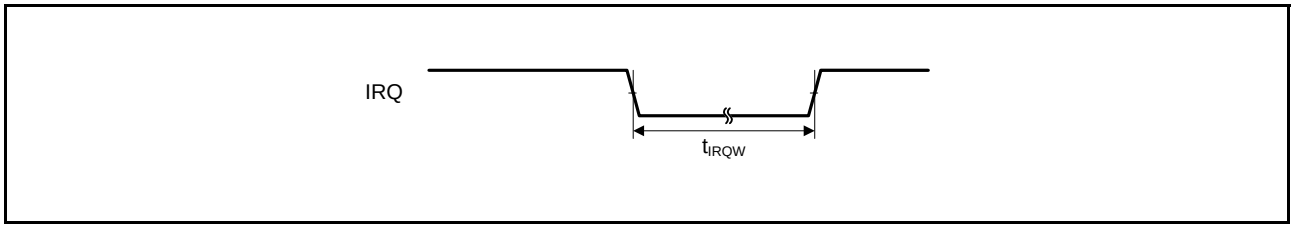


Figure 5.16 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.15 Bus Timing

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 100 MHz, BCLK = 8 to 50 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF
High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	20	ns	
CS# delay time	t_{CSD}	—	20	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	20	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.17 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V*1, VREFH0 = 3.0 V to AVCC0*1,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
PCLK = 8 to 50 MHz,
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master	VCC ≥ 3.0 V	t_{SU}	15	—	ns	C = 30pF, Figure 5.33 to Figure 5.36
			VCC < 3.0 V		20	—		
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master		t_H	0	—	ns	
		Slave			$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	18	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	C = 30pF, Figure 5.35 and Figure 5.36
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.
Note 2. t_{Pcyc}: PCLK cycle

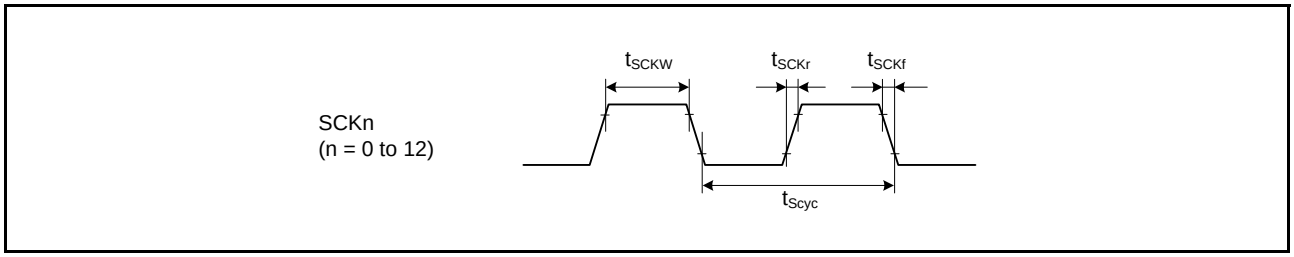


Figure 5.29 SCK Clock Input Timing

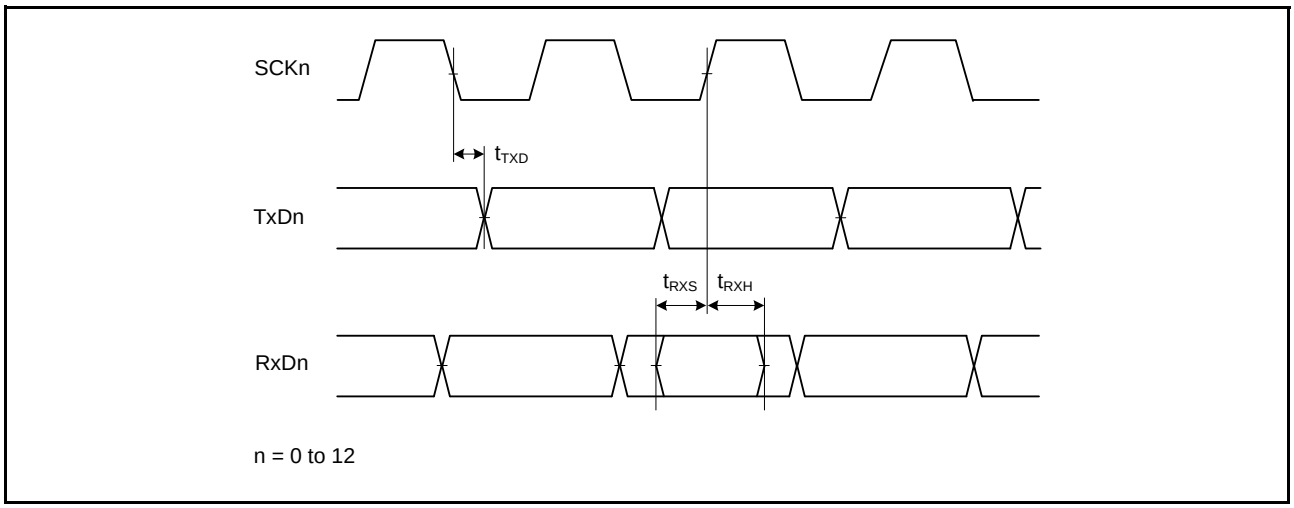


Figure 5.30 SCI Input/Output Timing: Clock Synchronous Mode

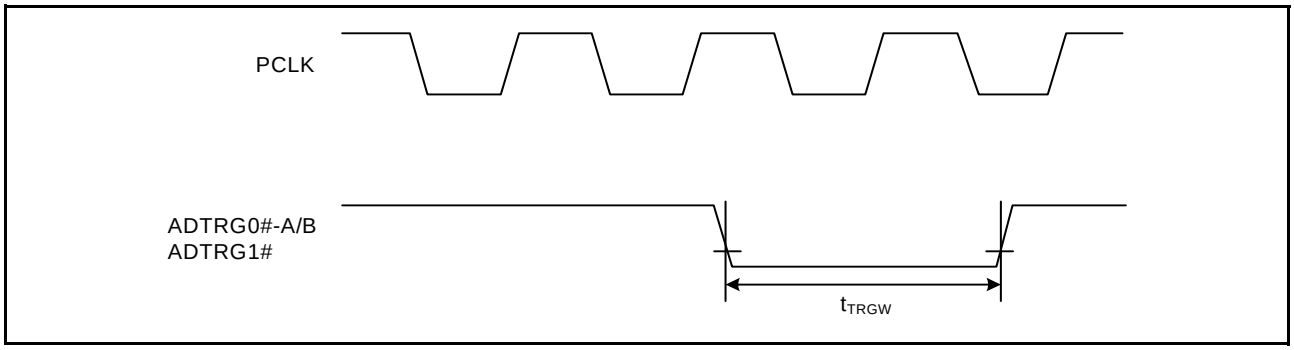


Figure 5.31 A/D Converter External Trigger Input Timing

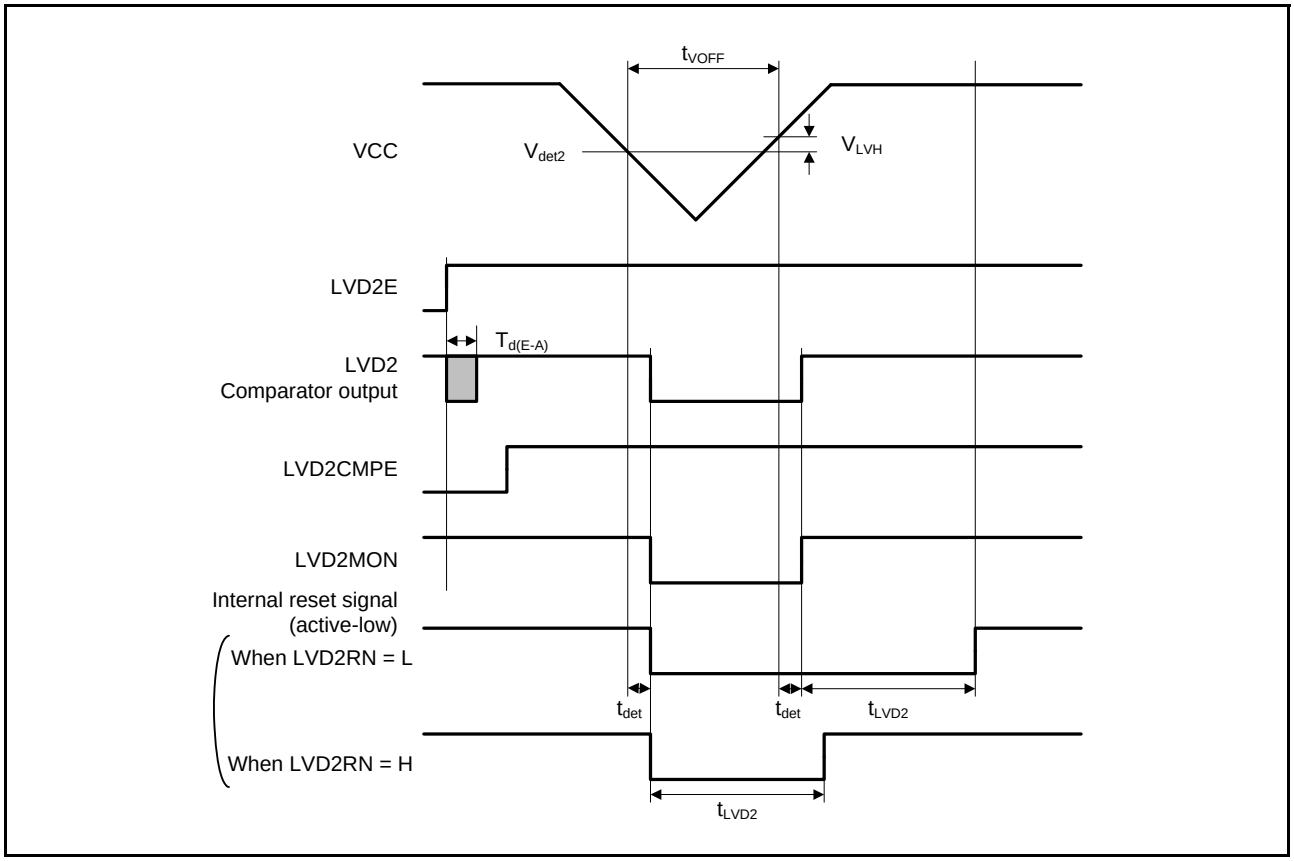
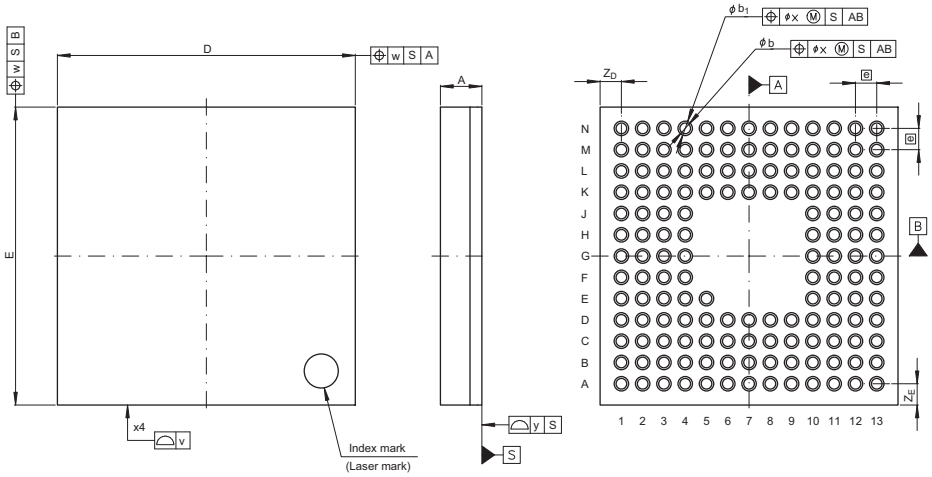


Figure 5.43 Voltage Detection Circuit Timing (V_{det2})

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 145-Pin TFLGA (PTLG0145KA-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.60	May 19. 2014	Features		
		1	Operating temp. range, changed Unique ID, added	
		1. Overview		
		All	Name of the on-chip emulator pin, changed: TRSYNC# → TRSYNC	
		2 to 6	Table 1.1 Outline of Specifications: Reset, real time clock, package, CPU, ROM, RAM, E2 DataFlash, clock generation circuit, temperature sensor, power supply voltage, changed. Low power consumption, deleted Operating temp. range changed, Unique ID and Note 1, added	
		7	Table 1.2 Comparison of Functions for Different Packages: Unique ID, added	
		8, 9	Table 1.3 List of Products: Group and Note 1 changed, Operating Temp. Range and G version added, Note 2 added	TN-RX*-A092A/E
		10	Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed	
		12, 15	Table 1.4 Pin Functions: VCC, VBATT and USB power pins, changed	
		43 to 45	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), changed (pinsTPU6 to TPU11, and RSPI2 have been deleted)	TN-RX*-A007A/E
		46 to 48	Table 1.10 List of Pins and Pin Functions (100-Pin LQFP), changed (pinsTPU6 to TPU11, and RSPI2 have been deleted)	TN-RX*-A007A/E
		3. Address Space		
		56	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		63, 76, 101	Table 4.1 List of I/O Registers (Address Order), changed, Note 9 added	TN-RX*-A048A/E
		5. Electrical Characteristics		
		All	Characteristics and timing conditions in the tables, changed	
		102	Table 5.1 Absolute Maximum Ratings: Operating temperature, changed	
		104	Table 5.3 DC Characteristics (2): Three-state leakage current (off state), Test conditions, changed; Input pull-up MOS current, changed	
		105	Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title, Analog power supply current, Reference power supply current, Note 7, and Note 8, changed RAM standby voltage, added	
		106	Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added	
		108 to 131	5.3 AC Characteristics, section structure changed	
		108	Table 5.7 Operation Frequency Value (High-Speed Operating Mode): Note, changed	
		109	Table 5.10 Reset Timing: changed, Note deleted	
		109	Figure 5.1 Reset Input Timing at Power-On, changed	
		109	Figure 5.2 Reset Input Timing, changed	
		110	Table 5.11 Clock Timing (Except for Sub-Clock Related): Item and Table, changed, Note, added	TN-RX*-A021A/E TN-RX*-A097A/E
		111	Table 5.12 Clock Timing (Sub-Clock Related): Sub-clock oscillation stabilization wait offset time, changed, Note, added	
		112	Figure 5.6 LOCO, IWDTCLK Oscillation Start Timing: Title and figure, changed	TN-RX*-A097A/E
		112	Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0), changed	
		112	Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit), changed	
		114	Figure 5.12 Sub-Clock Oscillation Start Timing, changed	
		115	Figure 5.14 Deep Software Standby Mode Cancellation Timing, changed	
		116	Table 5.15 Bus Timing, changed	
		118	Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized), changed	
		119	Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized), changed	