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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RX
Core Size	32-Bit
Speed	100MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630bcdfb-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630bcdfb-v0</a>

**Table 1.4 Pin Functions (2/5)**

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pin
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock
Port output enable 2	POE0# to POE3# POE8#	Input	Input pins for request signals to place the MTU large-current pins in the high impedance state

**Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)**

Pin Number	Power Supply Clock System Control	I/O Port	Bus	Timer  (MTU, TPU, TMR, PPG, RTC, POE)	Communications  (SCiC, SCiD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2	AVCC0						
A3	VREFL0						
A4		P42				IRQ10-DS	AN002
A5		P46				IRQ14-DS	AN006
A6	VCC						
A7	VSS						
A8		P94	A20/D20				
A9		PK0					
A10		P97	A23/D23				
A11		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A12		P60	CS0#		SCK9		
A13		P63	CS3#				
A14		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1		P05				IRQ13	DA1
B2		P07				IRQ15	ADTRG0#
B3		P40				IRQ8-DS	AN000
B4		P41				IRQ9-DS	AN001
B5		P47				IRQ15-DS	AN007
B6		P91	A17/D17		SCK7		AN015
B7		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
B8		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
B9		P96	A22/D22				
B10		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B11		PG1	D25				
B12		PK3			RXD9/SMISO9/SSCL9		
B13		P64	CS4#				
B14		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
C1	VREFL						
C2	VREFH						
C3	VREFH0						
C4		P43				IRQ11-DS	AN003
C5		P45				IRQ13-DS	AN005
C6		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
C7		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
C8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
C9		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C10		PG0	D24				
C11		PK2			TXD9/SMOSI9/SSDA9		
C12		P62	CS2#				

**Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)**

Pin Number	Power Supply Clock System Control	I/O Port	Bus	Timer  (MTU, TPU, TMR, PPG, RTC, POE)	Communications  (SCiC, SCiD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C14		PK4			RXD4/SMISO4/SSCL4		
C15		P70			SCK4		
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8		PK1					
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#		CTS9#/RTS9#/SS9#		
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
D13		PK5			TXD4/SMOSI4/SSDA4		
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#		CRX2*2	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#		CTX2*2		
F13	TRSYNC#	PG4	D28				
F14		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
G15	VCC						

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (2/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
41		PH4					
42		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
43		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
44		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
45		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	
46		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
47		P87		TIOCA2			
48		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS	IRQ6	ADTRG0#
49		P86		TIOCA0			
50		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
51		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
52		P85					
53		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
54		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
55		P11		MTIC5V/TMCI3	SCK2	IRQ1	
56		P10		MTIC5W/TMRI3		IRQ0	
57	VCC_USB						
58					USB0_DM		
59					USB0_DP		
60	VSS_USB						
61		P57	WAIT#/WR3#/ BC3#				
62		P56	WR2#/BC2#	MTIOC3C/TIOCA1			
63		PL4					
64		PL3					
65		PL2					
66		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
67		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1		
68	BCLK	P53*1					
69		P84					
70		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
71		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83		MTIOC4C	CTS10#/RTS10#/SS10#		
75	VCC						

**Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (3/5)**

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCId, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
76		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA		
79		P82		MTIOC4A/PO28	TXD10/SMOSI10/SSDA10		
80		P81		MTIOC3D/PO27	RXD10/SMISO10/ SSCL10		
81		P80		MTIOC3B/PO26	SCK10		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
83		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
84		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11		
85		P76	CS6#	PO22	RXD11/SMISO11/SSCL11		
86		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
87		P75	CS5#	PO20	SCK11		
88		P74	CS4#	PO19	CTS11#/RTS11#/SS11#		
89		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3	IRQ12	
90		PL1					
91		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3	IRQ14	
92		PL0					
93		P73	CS3#	PO16			
94		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
95		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
97		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6		
99		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#				
102		P71	CS1#				
103		PK7					
104		PB0	A8	MTIC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105		PK6					
106		PA7	A7	TIOCB2/PO23	MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
108		PA5	A5	TIOCB1/PO21	RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (3/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
72		P74	CS4#	PO19	CTS11#/RTS11#/SS11#		
73		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3	IRQ12	
74		PL1					
75		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3	IRQ14	
76		PL0					
77		P73	CS3#	PO16			
78		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
79		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
80		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
81		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
82		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6		
83		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		
84		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
85		P72	CS2#				
86		P71	CS1#				
87		PB0	A8	MTIC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
88		PA7	A7	TIOCB2/PO23	MISOA		
89		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
90		PA5	A5	TIOCB1/PO21	RSPCKA		
91	VCC						
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
95		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
97		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
98		P67	CS7#		CRX2*2	IRQ15	
99		P66	CS6#		CTX2*2		
100		P65	CS5#				
101		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
102		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
103		PK5			TXD4/SMOSI4/SSDA4		
104		P70			SCK4		
105		PK4			RXD4/SMISO4/SSCL4		
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2

**Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/3)**

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
33		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
40		P54	ALE	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1		
41	BCLK	P53*2					
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
49		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
51		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
54		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3/TCLKD/TMO0/ PO27/POE3#	SCK6		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#		
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
60	VCC						
61		PB0	A8	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
62	VSS						
63		PA7	A7	TIOCB2/PO23	MISOA		
64		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
65		PA5	A5	TIOCB1/PO21	RSPCKA		
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMR10/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	



**Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (3/3)**

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
68		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
69		PA1	A1	MTIOC0B/MTCLKC/ TIOC0B/PO17	SCK5/SSLA2	IRQ11	
70		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
71		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
72		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN3
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN2
75		PE3	D11[A11/D11]	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
76		PE2	D10[A10/D10]	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
77		PE1	D9[A9/D9]	MTIOC4C/PO18	TXD12/SMOS12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
78		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN7
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6	AN6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5	AN013
82		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
83		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
84		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
85		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
86		PD0	D0[A0/D0]			IRQ0	AN008
87		P47				IRQ15-DS	AN007
88		P46				IRQ14-DS	AN006
89		P45				IRQ13-DS	AN005
90		P44				IRQ12-DS	AN004
91		P43				IRQ11-DS	AN003
92		P42				IRQ10-DS	AN002
93		P41				IRQ9-DS	AN001
94	VREFL0						
95		P40				IRQ8-DS	AN000
96	VREFH0						
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						
100		P05				IRQ13	DA1

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (18/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8327h	RIIC1	I <sup>2</sup> C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8328h	RIIC1	I <sup>2</sup> C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8329h	RIIC1	I <sup>2</sup> C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNL	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8330h	RIIC1	I <sup>2</sup> C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8331h	RIIC1	I <sup>2</sup> C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8332h	RIIC1	I <sup>2</sup> C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8333h	RIIC1	I <sup>2</sup> C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8340h	RIIC2	I <sup>2</sup> C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8341h	RIIC2	I <sup>2</sup> C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8342h	RIIC2	I <sup>2</sup> C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8343h	RIIC2	I <sup>2</sup> C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8344h	RIIC2	I <sup>2</sup> C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8345h	RIIC2	I <sup>2</sup> C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8346h	RIIC2	I <sup>2</sup> C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8347h	RIIC2	I <sup>2</sup> C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8348h	RIIC2	I <sup>2</sup> C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8349h	RIIC2	I <sup>2</sup> C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ah	RIIC2	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Bh	RIIC2	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ch	RIIC2	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Dh	RIIC2	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Eh	RIIC2	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Fh	RIIC2	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8350h	RIIC2	I <sup>2</sup> C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8351h	RIIC2	I <sup>2</sup> C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8352h	RIIC2	I <sup>2</sup> C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8353h	RIIC2	I <sup>2</sup> C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8360h	RIIC3	I <sup>2</sup> C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8361h	RIIC3	I <sup>2</sup> C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8362h	RIIC3	I <sup>2</sup> C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8363h	RIIC3	I <sup>2</sup> C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8364h	RIIC3	I <sup>2</sup> C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8365h	RIIC3	I <sup>2</sup> C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8366h	RIIC3	I <sup>2</sup> C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8367h	RIIC3	I <sup>2</sup> C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8368h	RIIC3	I <sup>2</sup> C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8369h	RIIC3	I <sup>2</sup> C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (25/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCId, SCId
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A9h	SCI5	I <sup>2</sup> C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0AAh	SCI5	I <sup>2</sup> C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ABh	SCI5	I <sup>2</sup> C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ACh	SCI5	I <sup>2</sup> C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C9h	SCI6	I <sup>2</sup> C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CAh	SCI6	I <sup>2</sup> C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CBh	SCI6	I <sup>2</sup> C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CCh	SCI6	I <sup>2</sup> C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E9h	SCI7	I <sup>2</sup> C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EAh	SCI7	I <sup>2</sup> C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EBh	SCI7	I <sup>2</sup> C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ECh	SCI7	I <sup>2</sup> C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A109h	SCI8	I <sup>2</sup> C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ah	SCI8	I <sup>2</sup> C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (37/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 2848h	CAN2	Receive FIFO control register	RFCCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ah	CAN2	Transmit FIFO control register	TFCCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Bh	CAN2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ch	CAN2	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 284Dh	CAN2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Eh	CAN2	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Fh	CAN2	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 2850h	CAN2	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2851h	CAN2	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2852h	CAN2	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2853h	CAN2	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 2854h	CAN2	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2856h	CAN2	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2858h	CAN2	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0004h	USB0	System configuration status register 0	SYSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0036h	USB0	BRDY interrupt status register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0038h	USB0	NRDY interrupt status register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	

**Table 5.6 Permissible Output Currents**

Conditions:  $V_{CC} = AVCC0 = VREFH = VCC\_USB = 2.7$  to  $3.6$  V,  $VREFH0 = 2.7$  V to  $AVCC0$ ,  
 $VSS = AVSS0 = VREFL/VREFLO = VSS\_USB = 0$  V,  $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	$I_{OL}$	—	—	2.0	mA
	All output pins*2	High drive	$I_{OL}$			3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	$I_{OL}$	—	—	4.0	mA
	All output pins*2	High drive	$I_{OL}$			7.6	mA
Permissible output low current (total)	Total of all output pins		$\Sigma I_{OL}$	—	—	80	mA
Permissible output high current (average value per pin)	All output pins (except for USB_DPUPE pin)*1	Normal drive	$-I_{OH}$	—	—	-2.0	mA
	USB_DPUPE pin*2	High drive	$-I_{OH}$	—	—	-3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	$-I_{OH}$	—	—	-4.0	mA
	All output pins*2	High drive	$-I_{OH}$	—	—	-7.6	mA
Permissible output high current (total)	Total of all output pins		$\Sigma -I_{OH}$	—	—	-80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

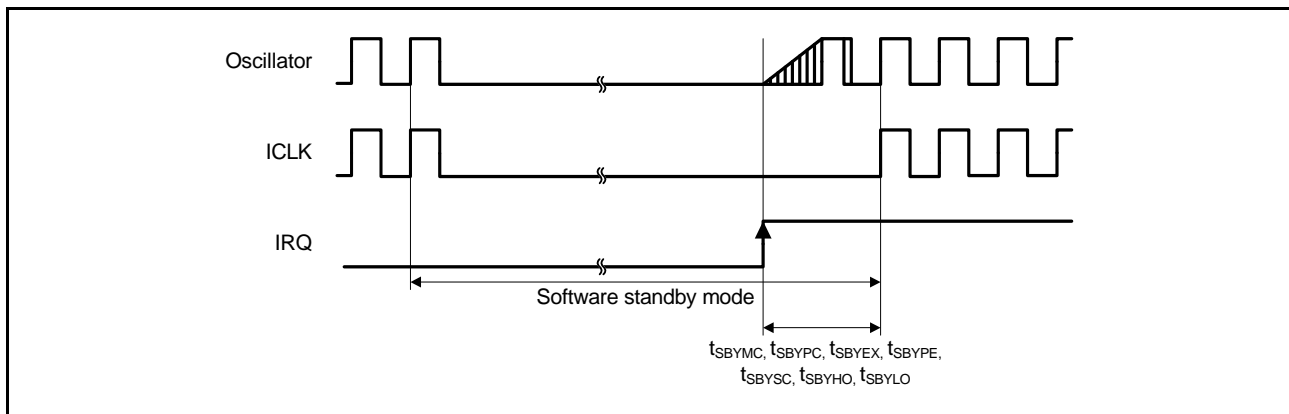


Figure 5.13 Software Standby Mode Cancellation Timing

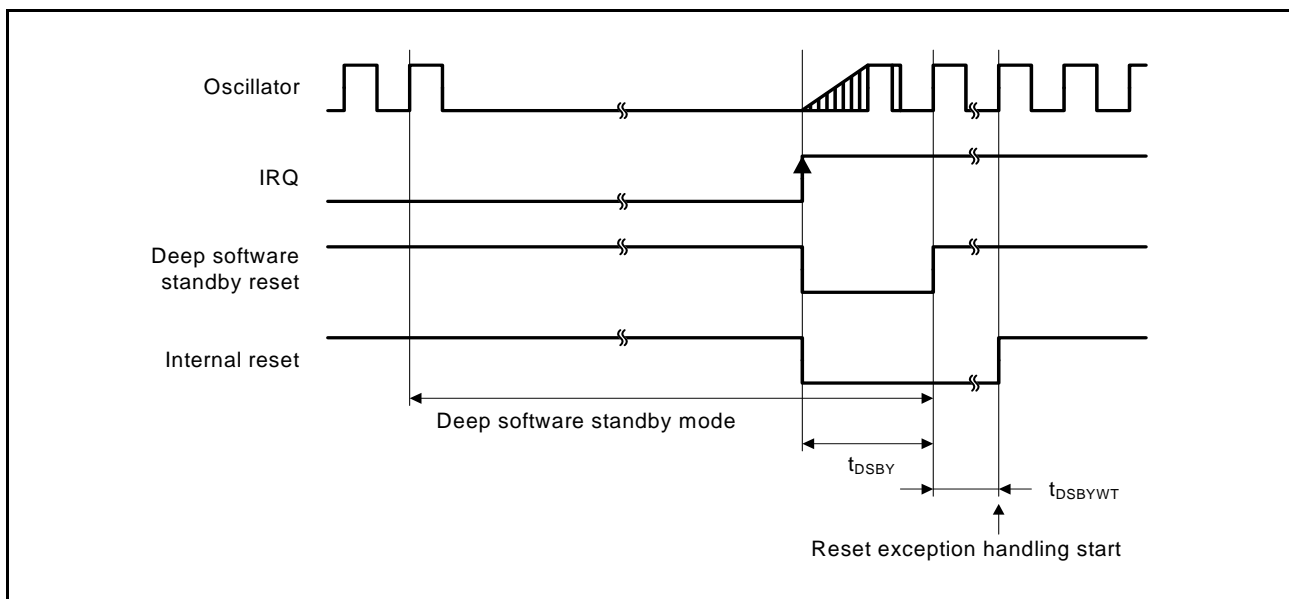


Figure 5.14 Deep Software Standby Mode Cancellation Timing

### 5.3.4 Control Signal Timing

Table 5.14 Control Signal Timing

Conditions:  $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $V_{REFH0} = 2.7$  V to  $AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS\_USB} = 0$  V,  $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	$t_{NMIW}$	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15
		$t_c (PCLK) \times 2$	—	—		$t_c (PCLK) \times 2 > 200$ ns Figure 5.15
IRQ pulse width	$t_{IRQW}$	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16
		$t_c (PCLK) \times 2$	—	—		$t_c (PCLK) \times 2 > 200$ ns Figure 5.16

**Table 5.20 Timing of On-Chip Peripheral Modules (5)**

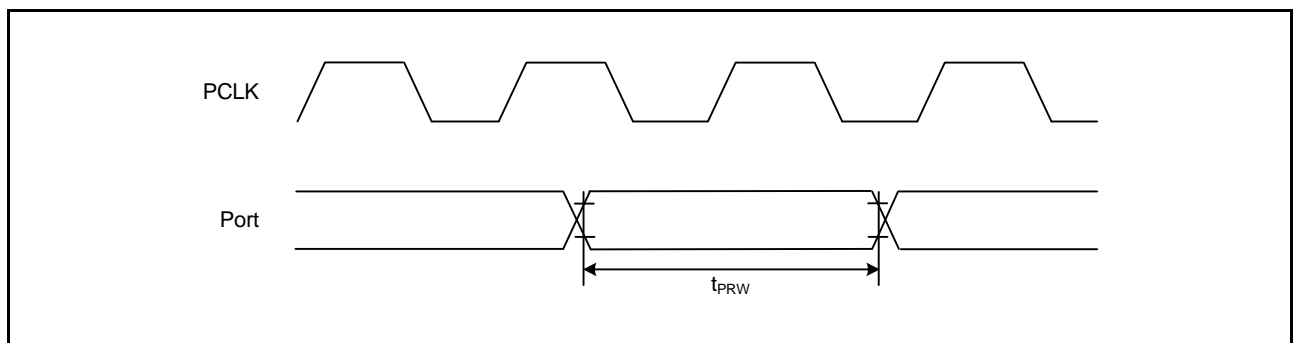
Conditions: VCC = AVCC0 = VREFH = VCC\_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0  
 VSS = AVSS0 = VREFL/VREFLO = VSS\_USB = 0 V  
 PCLK = 8 to 50 MHz  
 T<sub>a</sub> = T<sub>opr</sub>  
 High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*, *2	Max.*	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t <sub>SCL</sub>	6(12) × t <sub>IICcyc</sub> + 240	—	ns	Figure 5.37
	SCL input high pulse width	t <sub>SCLH</sub>	3(6) × t <sub>IICcyc</sub> + 120	—	ns	
	SCL input low pulse width	t <sub>SCLL</sub>	3(6) × t <sub>IICcyc</sub> + 120	—	ns	
	SCL, SDA input rise time	t <sub>Sr</sub>	—	120	ns	
	SCL, SDA input fall time	t <sub>Sf</sub>	—	120	ns	
	SCL, SDA input spike pulse removal time	t <sub>SP</sub>	0	1(4) × t <sub>IICcyc</sub>	ns	
	SDA input bus free time	t <sub>BUF</sub>	3(6) × t <sub>IICcyc</sub> + 120	—	ns	
	Start condition input hold time	t <sub>STAH</sub>	t <sub>IICcyc</sub> + 120	—	ns	
	Restart condition input setup time	t <sub>STAS</sub>	120	—	ns	
	Stop condition input setup time	t <sub>STOS</sub>	120	—	ns	
	Data input setup time	t <sub>SDAS</sub>	t <sub>IICcyc</sub> + 120	—	ns	
	Data input hold time	t <sub>SDAH</sub>	0	—	ns	
	SCL, SDA capacitive load	C <sub>b</sub>	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t <sub>Sr</sub>	—	1000	ns	
	SDA input fall time	t <sub>Sf</sub>	—	300	ns	
	SDA input spike pulse removal time	t <sub>SP</sub>	0	4 × t <sub>IICcyc</sub>	ns	
	Data input setup time	t <sub>SDAS</sub>	250	—	ns	
	Data input hold time	t <sub>SDAH</sub>	0	—	ns	
	SCL, SDA capacitive load	C <sub>b</sub>	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t <sub>Sr</sub>	20 + 0.1C <sub>b</sub>	300	ns	
	SCL, SDA input fall time	t <sub>Sf</sub>	20 + 0.1C <sub>b</sub>	300	ns	
	SCL, SDA input spike pulse removal time	t <sub>SP</sub>	0	4 × t <sub>IICcyc</sub>	ns	
	Data input setup time	t <sub>SDAS</sub>	100	—	ns	
	Data input hold time	t <sub>SDAH</sub>	0	—	ns	
	SCL, SDA capacitive load	C <sub>b</sub>	—	400	pF	

Note: t<sub>IICcyc</sub>: RIIC internal reference clock (IICφ) Cycle, t<sub>Pcyc</sub>: PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C<sub>b</sub> indicates the total capacity of the bus line.



**Figure 5.24 I/O Port Input Timing**

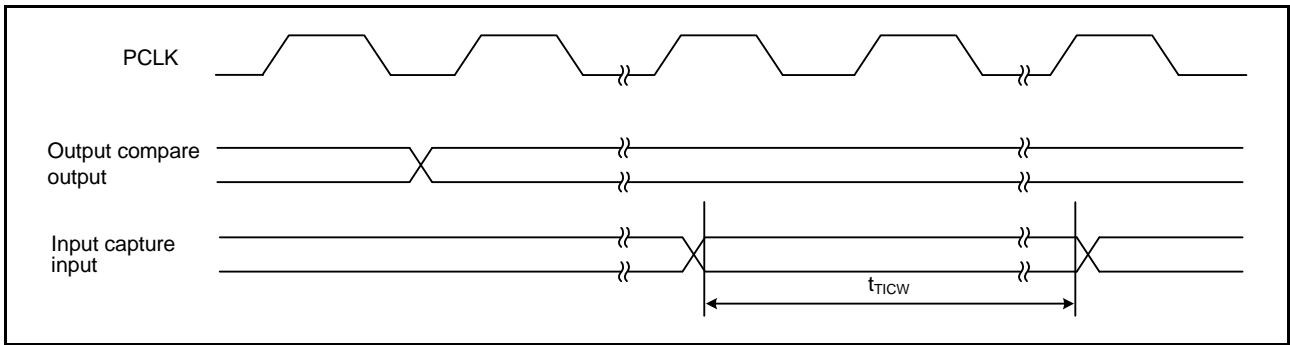


Figure 5.25 MTU Input/Output Timing

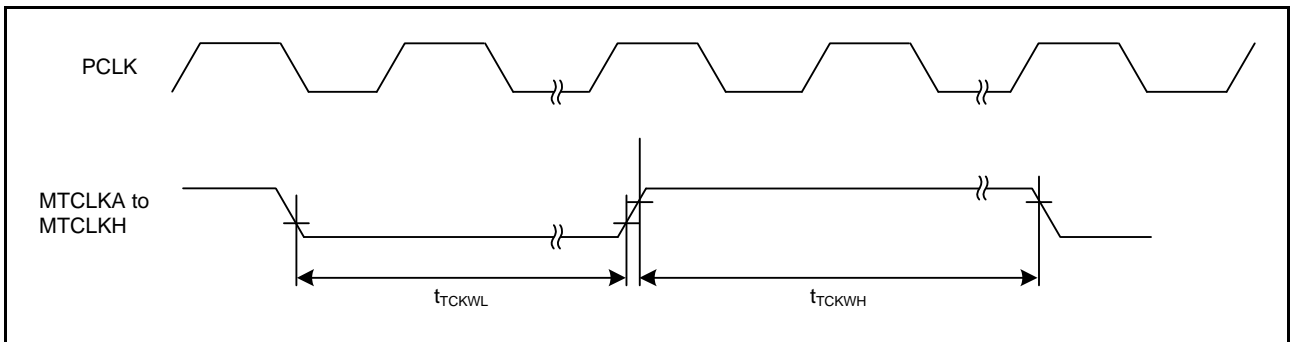


Figure 5.26 MTU Clock Input Timing

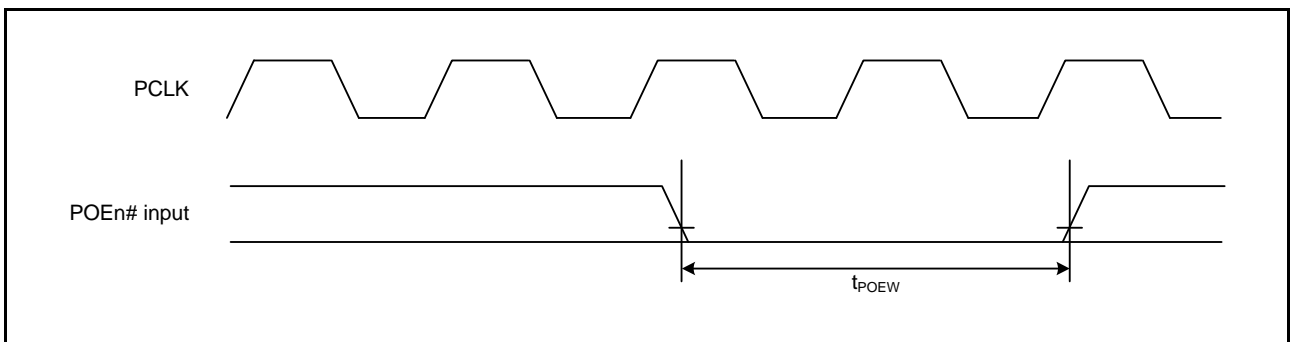


Figure 5.27 POE# Input Timing

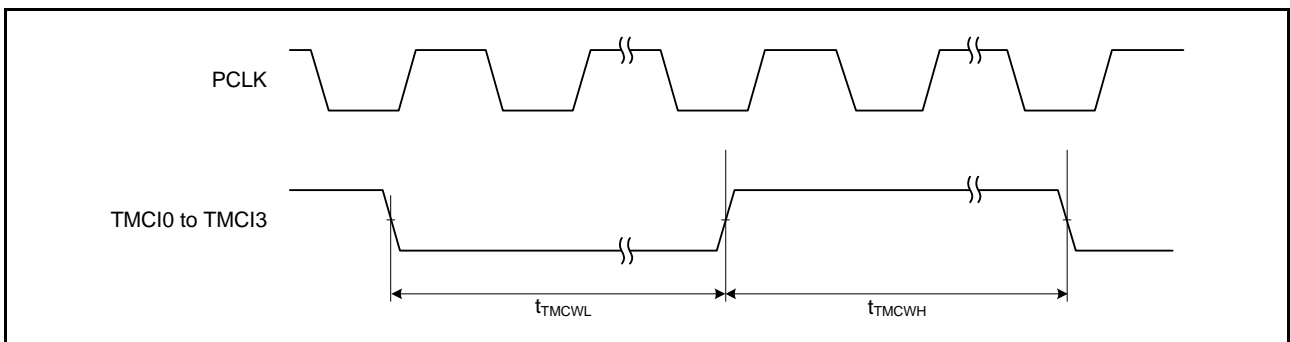


Figure 5.28 8-Bit Timer Clock Input Timing



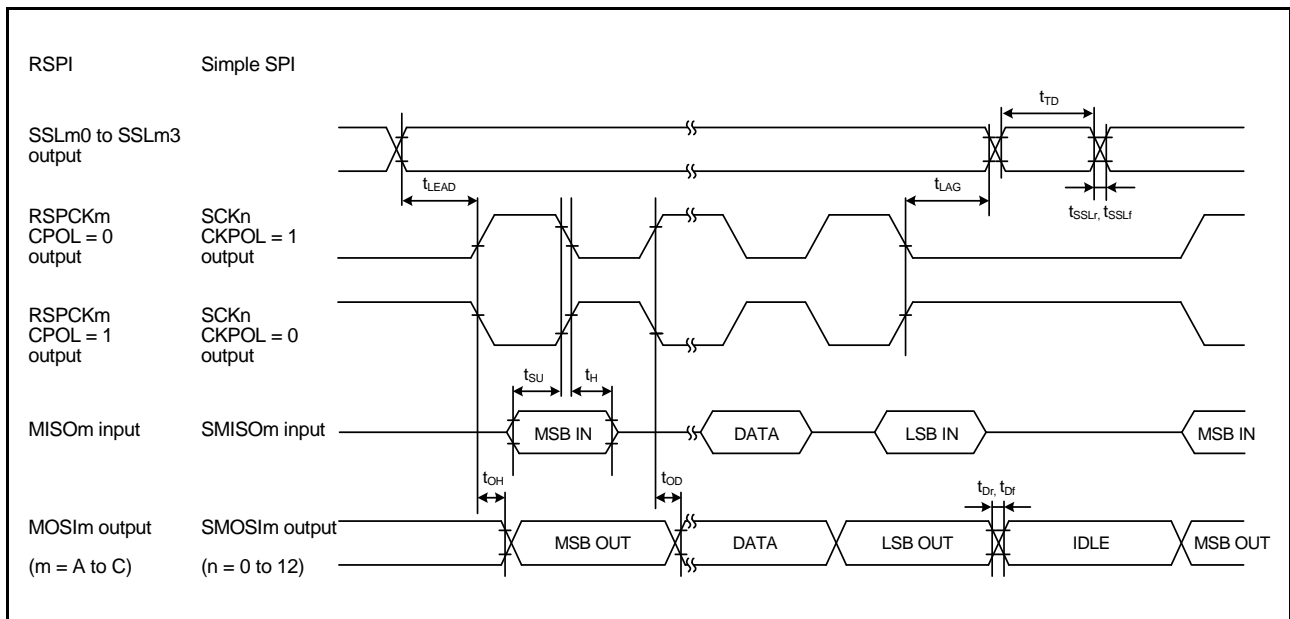


Figure 5.34 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

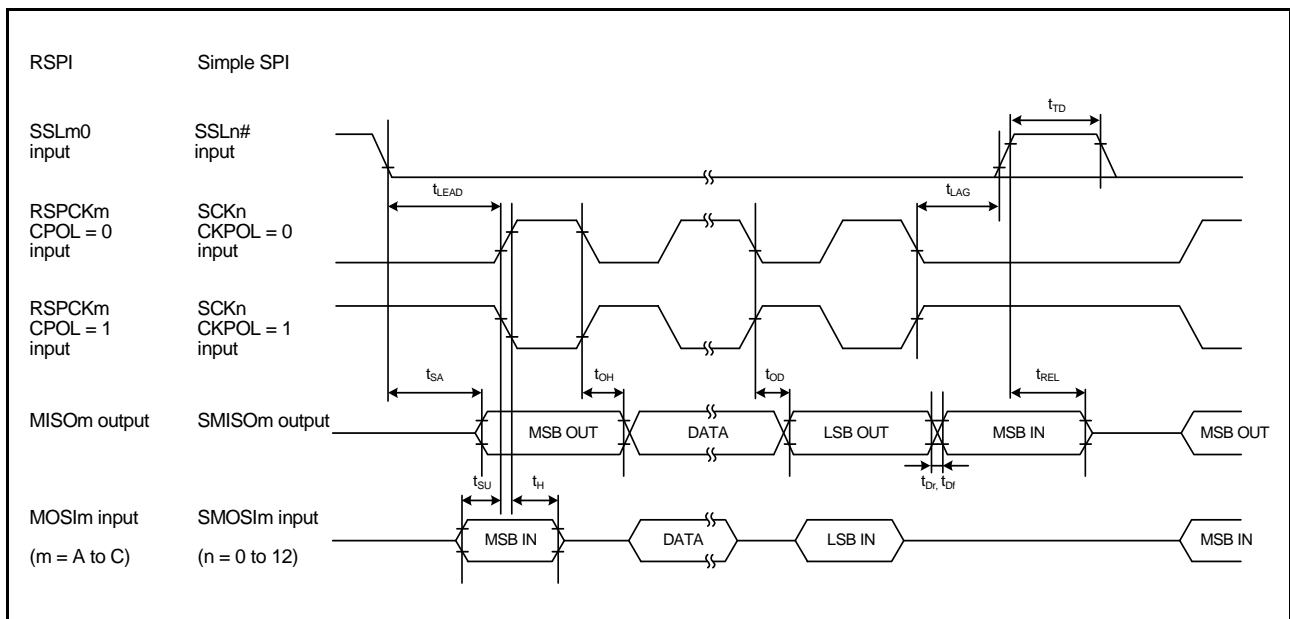


Figure 5.35 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

5.12 E<sup>2</sup> Flash Characteristics**Table 5.32 E<sup>2</sup> Flash Characteristics (1)**

Conditions: VCC = AVCC0 = VREFH = VCC\_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0  
 VSS = AVSS0 = VREFL/VREFL0 = VSS\_USB = 0 V  
 Temperature range for the programming/erasure operation: T<sub>a</sub> = T<sub>opr</sub>

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N <sub>DPEC</sub>	100000	—	—	Times	
Data hold time	t <sub>DDRP</sub>	30*2	—	—	Year	T <sub>a</sub> = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

**Table 5.33 E<sup>2</sup> Flash Characteristics (2)**

Conditions: VCC = AVCC0 = VREFH = VCC\_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0  
 VSS = AVSS0 = VREFL/VREFL0 = VSS\_USB = 0 V  
 Temperature range for the programming/erasure operation: T<sub>a</sub> = T<sub>opr</sub>

Item	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time N <sub>DPEC</sub> ≤ 100 times	2 bytes	t <sub>DP2</sub>	—	0.7	6	—	0.25	2	ms
Programming time N <sub>DPEC</sub> > 100 times	2 bytes	t <sub>DP2</sub>	—	0.7	6	—	0.25	2	ms
Erasure time N <sub>DPEC</sub> ≤ 100 times	32 bytes	t <sub>DE32</sub>	—	4	40	—	2	20	ms
Erasure time N <sub>DPEC</sub> > 100 times	32 bytes	t <sub>DE32</sub>	—	7	40	—	4	20	ms
Blank check time	2 bytes	t <sub>DBC2</sub>	—	—	100	—	—	30	μs
Suspend delay time during programming		t <sub>DSPD</sub>	—	—	250	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t <sub>DSESD1</sub>	—	—	250	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t <sub>DSESD2</sub>	—	—	500	—	—	300	μs
Suspend delay time during erasure (in erasure priority mode)		t <sub>DSEED</sub>	—	—	500	—	—	300	μs

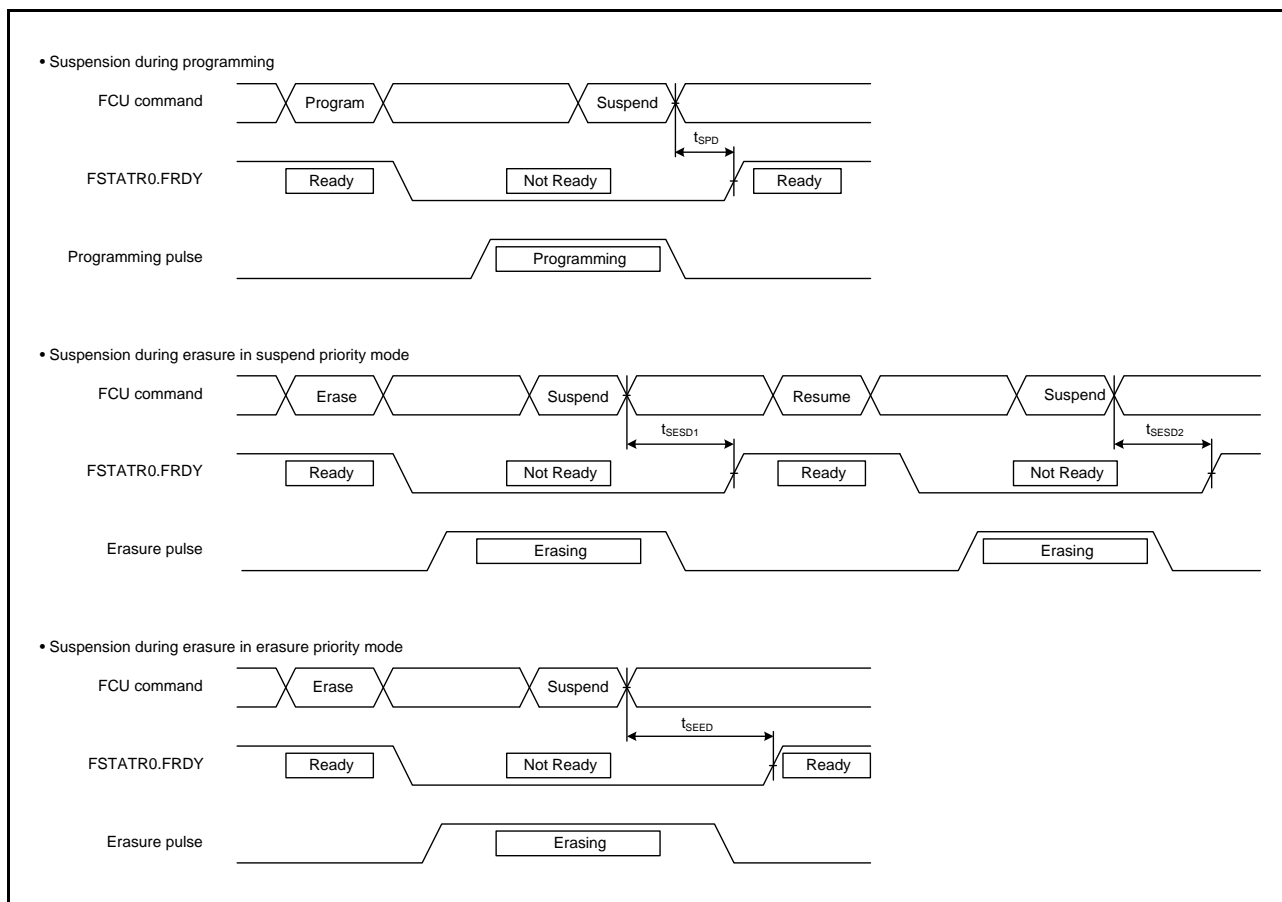


Figure 5.46 Flash Memory Program/Erase Suspend Timing

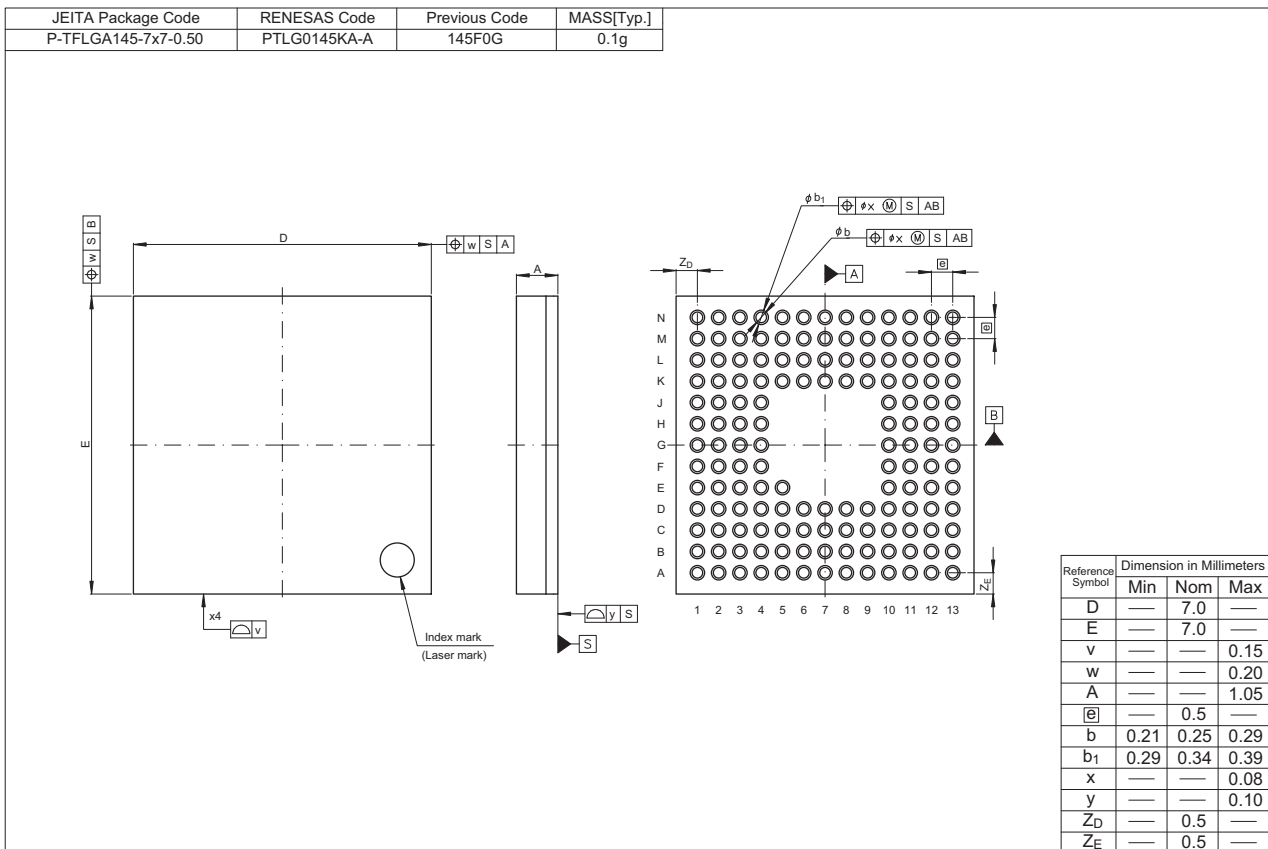


Figure D 145-Pin TFLGA (PTLG0145KA-A)

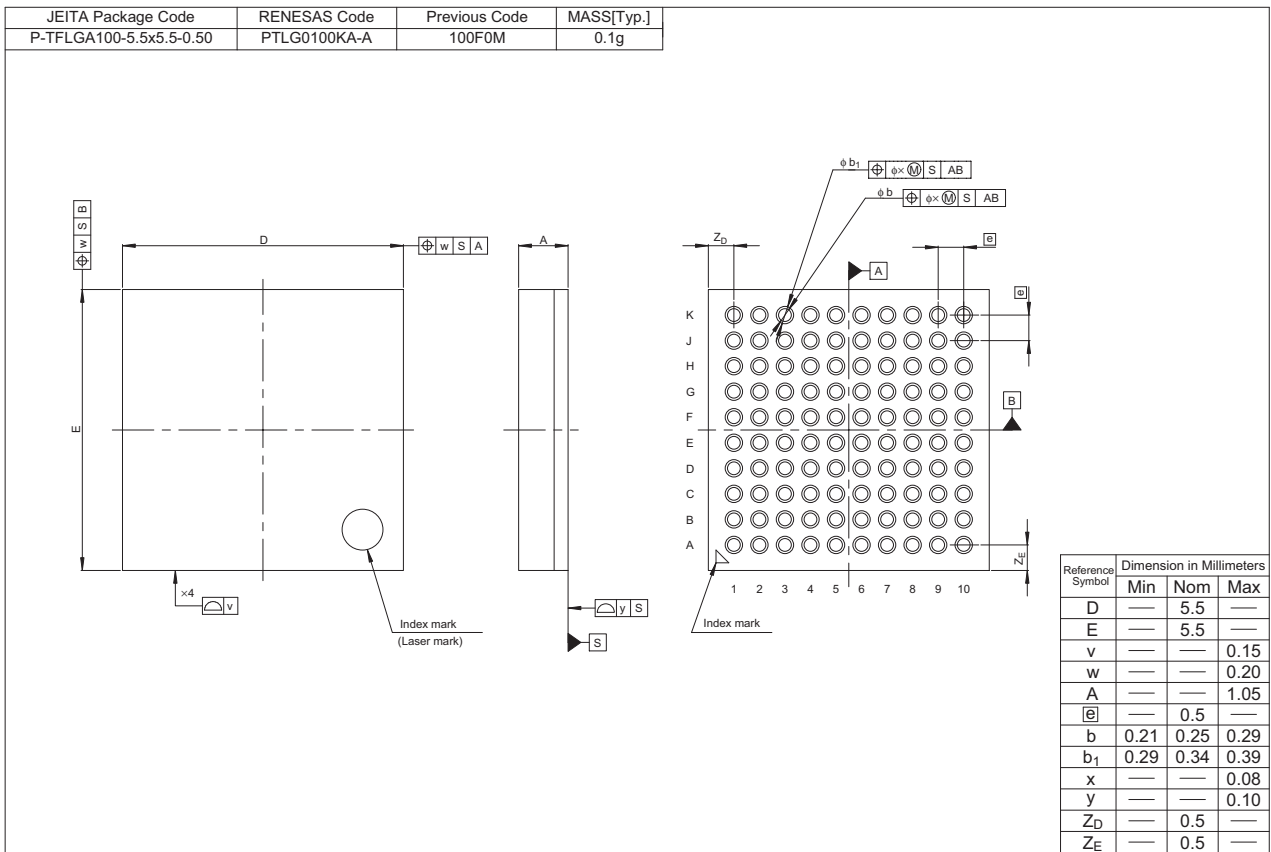


Figure F 100-Pin TFLGA (PTLG0100KA-A)