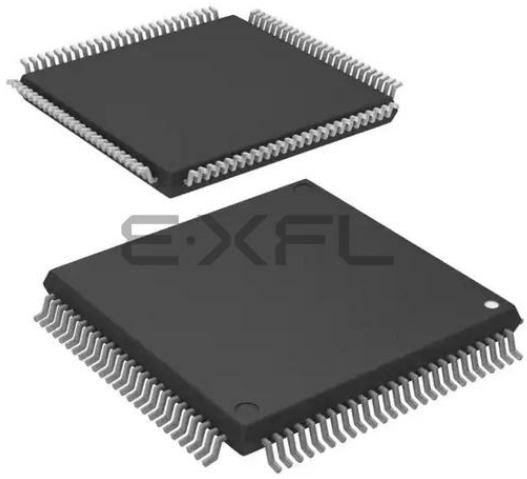
Renesas Electronics America Inc - R5F5630BDDFP#V0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630bddfp-v0

Table 1.1 Outline of Specifications (3/5)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 2 units • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Time bases for the 6 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines • Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • Digital filter • Signals from the input capture pins are input via a digital filter • PPG output trigger can be generated • Clock frequency measuring function
	Frequency measurement function (MCK)	The MTU or unit 0 TPU module can be used to monitor the main clock, sub-clock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies.
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Realtime clock (RTCa)	• Clock sources: Main clock, sub-clock • Clock and calendar functions Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTA)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator for the IWDT • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256

1.2 List of Products

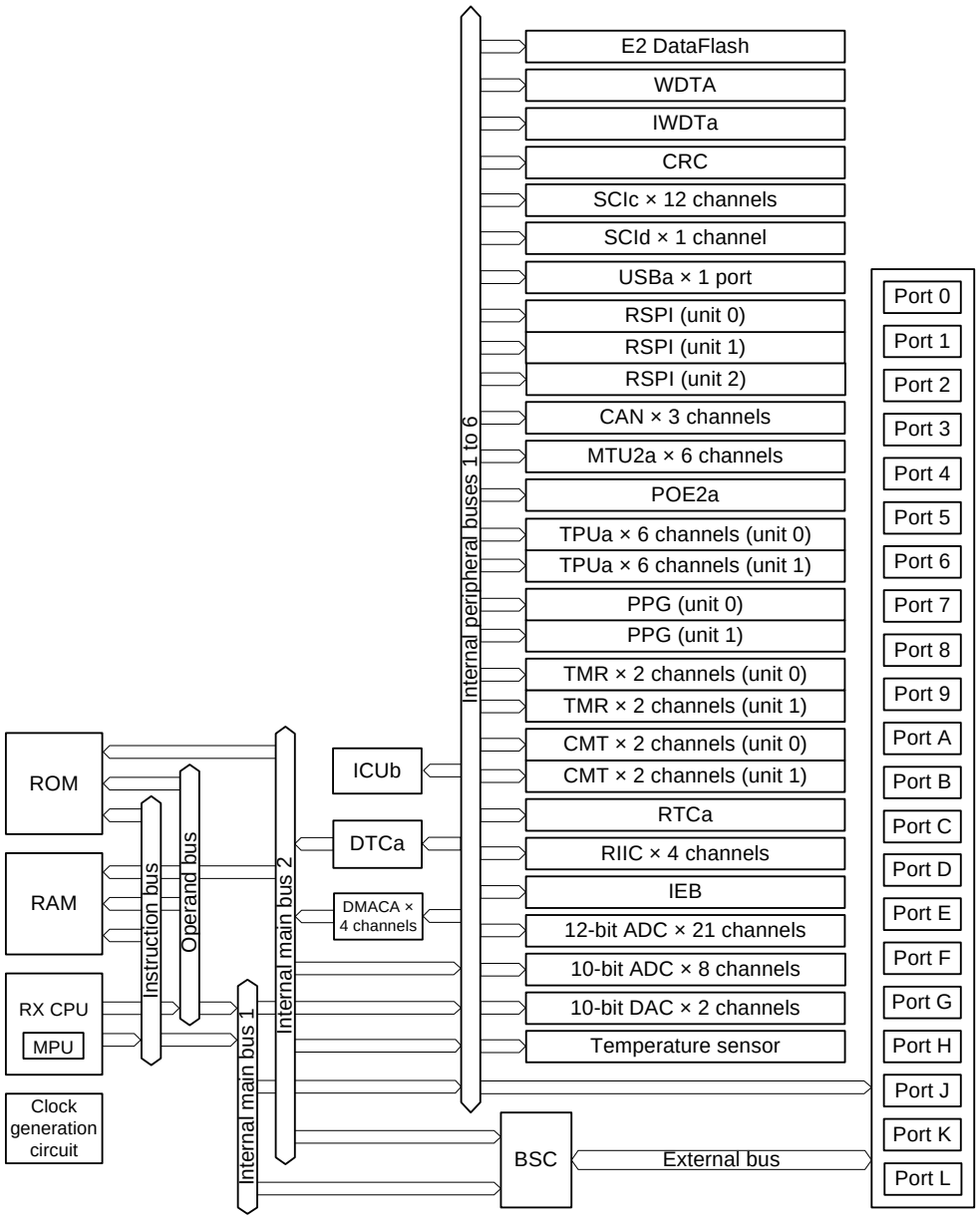
Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX630 (D version)	R5F56307CDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFP[*1]	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFP[*1]	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFB[*1]	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFB[*1]	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLK[*1]	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLK[*1]	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFP[*1]	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFP[*1]	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFB[*1]	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFB[*1]	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLK[*1]	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK[*1]	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLC	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLC	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb:	Interrupt controller	CAN:	CAN module
DTCa:	Data transfer controller	MTU2a:	Multi-function timer pulse unit 2
DMACA:	DMA controller	POE2a:	Port output enable 2
BSC:	Bus controller	TPUa:	16-bit timer pulse unit
WDTA:	Watchdog timer	PPG:	Programmable pulse generator
IWDTa:	Independent watchdog timer	TMR:	8-bit timer
CRC:	CRC (cyclic redundancy check) calculator	CMT:	Compare match timer
SCIc, SCId:	Serial communications interface	RTCa:	Realtime clock
USBa:	USB 2.0 function module	RIIC:	I^2C bus interface
RSPI:	Serial peripheral interface	IEB:	IEBus controller
MPU:	Memory protection unit		

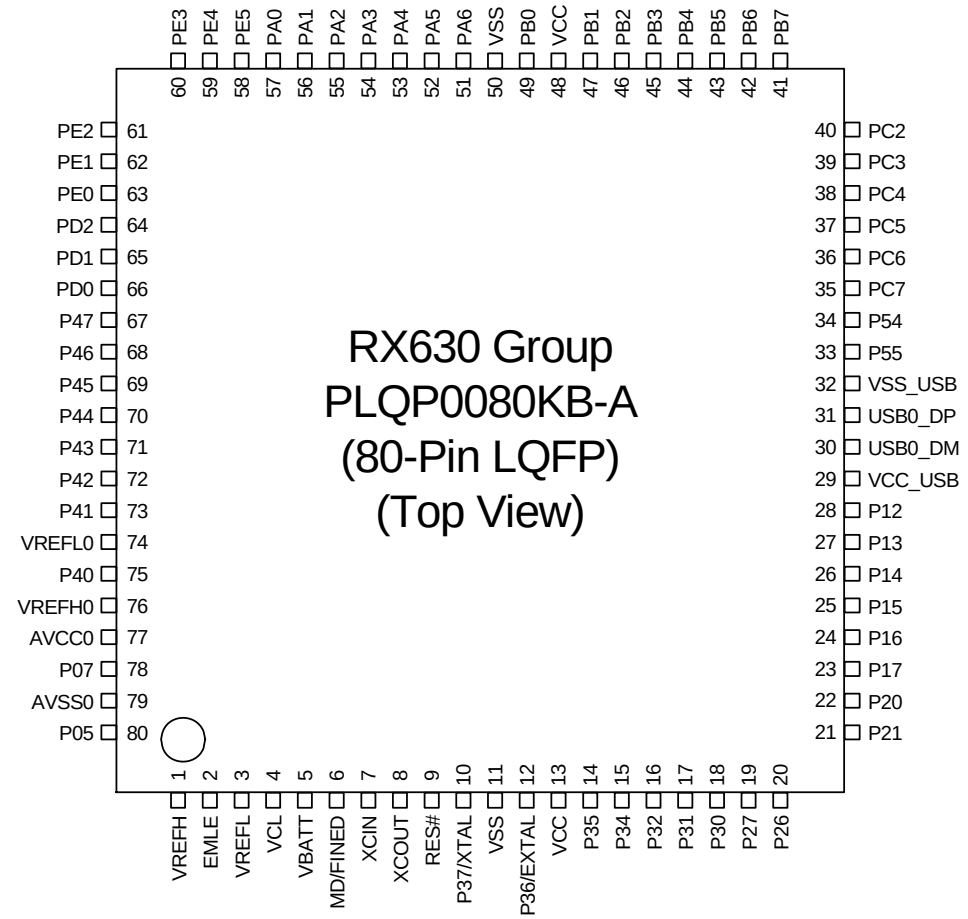
Figure 1.2 Block Diagram

RX630 Group
PTLG0100KA-A (100-Pin TFLGA)
(Top View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD	RES#	P35	P30	P16	P17	P20	3
2	VREFH	AVSS0	VREFL	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pins and Pin Functions (80-Pin LQFP).

Figure 1.10 Pin Assignment (80-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2	AVCC0						
A3	VREFL0						
A4		P42				IRQ10-DS	AN002
A5		P46				IRQ14-DS	AN006
A6	VCC						
A7	VSS						
A8		P94	A20/D20				
A9		PK0					
A10		P97	A23/D23				
A11		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A12		P60	CS0#		SCK9		
A13		P63	CS3#				
A14		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1		P05				IRQ13	DA1
B2		P07				IRQ15	ADTRG0#
B3		P40				IRQ8-DS	AN000
B4		P41				IRQ9-DS	AN001
B5		P47				IRQ15-DS	AN007
B6		P91	A17/D17		SCK7		AN015
B7		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
B8		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
B9		P96	A22/D22				
B10		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B11		PG1	D25				
B12		PK3			RXD9/SMISO9/SSCL9		
B13		P64	CS4#				
B14		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
C1	VREFL						
C2	VREFH						
C3	VREFH0						
C4		P43				IRQ11-DS	AN003
C5		P45				IRQ13-DS	AN005
C6		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
C7		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
C8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
C9		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C10		PG0	D24				
C11		PK2			TXD9/SMOSI9/SSDA9		
C12		P62	CS2#				

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (2/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
41		PH4					
42		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
43		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
44		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
45		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	
46		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
47		P87		TIOCA2			
48		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS	IRQ6	ADTRG0#
49		P86		TIOCA0			
50		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
51		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
52		P85					
53		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
54		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
55		P11		MTIC5V/TMCI3	SCK2	IRQ1	
56		P10		MTIC5W/TMRI3		IRQ0	
57	VCC_USB						
58					USB0_DM		
59					USB0_DP		
60	VSS_USB						
61		P57	WAIT#/WR3#/ BC3#				
62		P56	WR2#/BC2#	MTIOC3C/TIOCA1			
63		PL4					
64		PL3					
65		PL2					
66		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
67		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1		
68	BCLK	P53*1					
69		P84					
70		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
71		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83		MTIOC4C	CTS10#/RTS10#/SS10#		
75	VCC						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (2/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
D5	VCC						
D6		P93	A19		CTS7#/RTS7#/SS7#		AN017
D7		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D8		P60	CS0#		SCK9		
D9		P64	CS4#				
D10		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D11		PK5			TXD4/SMOSI4/SSDA4		
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
D13		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
E1	VSS						
E2	VCL						
E3		PJ5					
E4	EMLE						
E5		P44				IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
E11		P66	CS6#		CTX2*1		
E12		P65	CS5#				
E13		P67	CS7#		CRX2*1	IRQ15	
F1	XCIN						
F2	XCOUT						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	VBATT						
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
F11	VSS						
F12		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
F13		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
G1	XTAL	P37					
G2	RES#						
G3	MD/FINED						
G4	BSCANP						
G10		PA5	A5	TIOCB1/PO21	RSPCKA		
G11		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
G12	VCC						
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
H1	EXTAL	P36					
H2	VCC						
H3	VSS						
H4		P35				NMI	
H10		P72	CS2#				
H11		P71	CS1#				
H12		PB0	A8	MTIC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

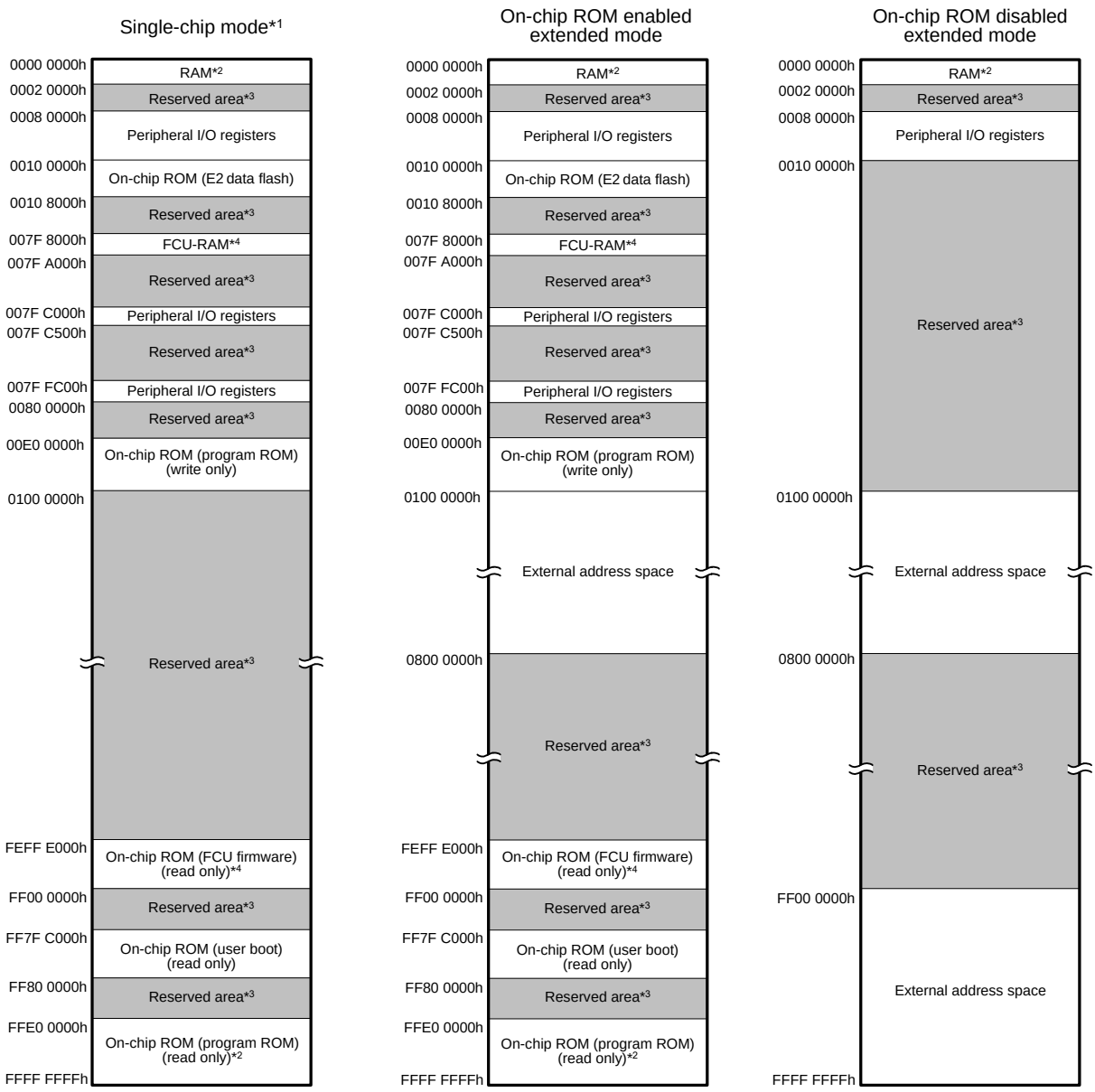
The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).



Note 1. The address space in boot mode and user boot mode/USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
2 M	FFE0 0000h to FFFF FFFFh	128 K	0000 0000h to 0001 FFFFh
1.5 M	FFE8 0000h to FFFF FFFFh		
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		

Note:See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
Note 4. For details on the FCU, see section 43, Flash Memory in the User's manual: Hardware.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (8/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2 ICLK		ICUb
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK		
0008 712Ah	ICU	DTC activation enable register 042	DTCER042	8	8	2 ICLK		
0008 712Bh	ICU	DTC activation enable register 043	DTCER043	8	8	2 ICLK		
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK		
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK		
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK		
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK		
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK		
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK		
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK		
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK		
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK		
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK		
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2 ICLK		
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2 ICLK		
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2 ICLK		
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2 ICLK		
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2 ICLK		
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2 ICLK		
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2 ICLK		
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2 ICLK		
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK		
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK		
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK		
0008 717Fh	ICU	DTC activation enable register 127	DTCER127	8	8	2 ICLK		
0008 7180h	ICU	DTC activation enable register 128	DTCER128	8	8	2 ICLK		
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK		
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK		
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK		
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK		
0008 7185h	ICU	DTC activation enable register 133	DTCER133	8	8	2 ICLK		
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK		
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK		
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK		
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK		
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK		
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK		
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK		
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK		
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK		
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK		
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK		
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK		
0008 7194h	ICU	DTC activation enable register 148	DTCER148	8	8	2 ICLK		
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK		
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK		
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK		
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK		
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (10/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 71F1h	ICU	DTC activation enable register 241	DTCER241	8	8	2 ICLK		ICUb
0008 71F2h	ICU	DTC activation enable register 242	DTCER242	8	8	2 ICLK		
0008 71F4h	ICU	DTC activation enable register 244	DTCER244	8	8	2 ICLK		
0008 71F5h	ICU	DTC activation enable register 245	DTCER245	8	8	2 ICLK		
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK		
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK		
0008 71FAh	ICU	DTC activation enable register 250	DTCER250	8	8	2 ICLK		
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK		
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK		
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK		
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK		
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK		
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2 ICLK		
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK		
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK		
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK		
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK		
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK		
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK		
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK		
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK		
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK		
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK		
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK		
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK		
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK		
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK		
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK		
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK		
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK		
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK		
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK		
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK		
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK		
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK		
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK		
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK		
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK		
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK		
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK		
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK		
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK		
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK		
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK		
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK		
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK		
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK		
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK		
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK		
0008 7323h	ICU	Interrupt source priority register 035	IPR035	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (17/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8209h	TMR1	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8215h	TMR3	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8217h	TMR3	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8219h	TMR3	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I²C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I²C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I²C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I²C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I²C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I²C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I²C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I²C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I²C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I²C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (39/42)

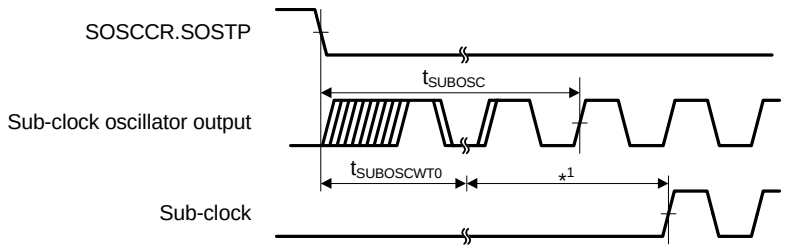
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0056h	USB0	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	USBa
000A 0058h	USB0	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 005Ah	USB0	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0060h	USB0	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0064h	USB0	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0068h	USB0	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 006Ch	USB0	Pipe maximum packet size register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 006Eh	USB0	Pipe cycle control register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0070h	USB0	Pipe 1 control register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	

Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	—	115	mA	ICLK = 100 MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 50 MHz
		Normal	Peripheral function: clock signal supplied*4		—	52	—		
			Peripheral function: clock signal stopped*4		—	40	—		
		Sleep mode			—	25	75		
		All-module-clock-stop mode (reference value)			—	20	45		
		Increased by BGO operation*5			—	15	—		
	Low-speed operating mode 1*6				—	4	—		ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—		ICLK = 32.768 kHz
	Software standby mode				—	0.2	6		
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	µA	
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power function enabled consumption function disabled		—	21	60		
			Power-on reset circuit and low-power function enabled consumption function enabled		—	6.2	28		
	Increased by RTC operation				—	3	—		
	RTC operation when VCC is off				—	1.7	—		V_{BATT} = 2.3 V
					—	3.3	—		V_{BATT} = 3.3 V
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I_{AVCC0}	—	2.3	3.2	mA	
	During 10-bit A/D conversion			I_{VREFH}*7	—	1.0	1.65	mA	
	During D/A conversion (per unit)				—	0.7	1.0	mA	
	Waiting for A/D, D/A conversion (all units)*8			—	—	25	35	µA	
	A/D, D/A converter in standby mode (all units)*8				—	0.1	5	µA	
Reference power supply current	During 12-bit A/D conversion			I_{VREFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA	
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0	µA	
RAM standby voltage				V_{RAM}	2.7	—	—	V	
VCC rising gradient				SrVCC	8.4	—	20000	µs/V	
VCC falling gradient*8				SfVCC	8.4	—	—	µs/V	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)
I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)
I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)
I_{CC} Max. = 0.48 × f + 12 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 7. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.
Note 8. The values are the sum of I_{AVCC0} and I_{VREFH}.



Note 1: This is the waiting period obtained by setting the SOCCWTCR.SSTS[4:0] bits.

Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.13 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t_{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V_{POR}	2.5	2.6	2.7	V	Figure 5.40
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0}	2.7	2.80	2.9		Figure 5.41
	Voltage detection circuit (LVD1)		V_{det1_A}	2.75	2.95	3.15		
	Voltage detection circuit (LVD2)		V_{det2_A}	2.75	2.95	3.15		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 5.40
	LVD0 reset time		t_{LVD0}	—	4.6	—		Figure 5.41
	LVD1 reset time		t_{LVD1}	—	0.9	—		Figure 5.42
	LVD2 reset time		t_{LVD2}	—	0.9	—		Figure 5.43
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 5.40 and Figure 5.41
Response delay time			t_{det}	—	—	200	µs	Figure 5.40 to Figure 5.43
LVD operation stabilization time (after LVD is enabled)			$Td_{(E-A)}$	—	—	3	µs	Figure 5.42 and Figure 5.43
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

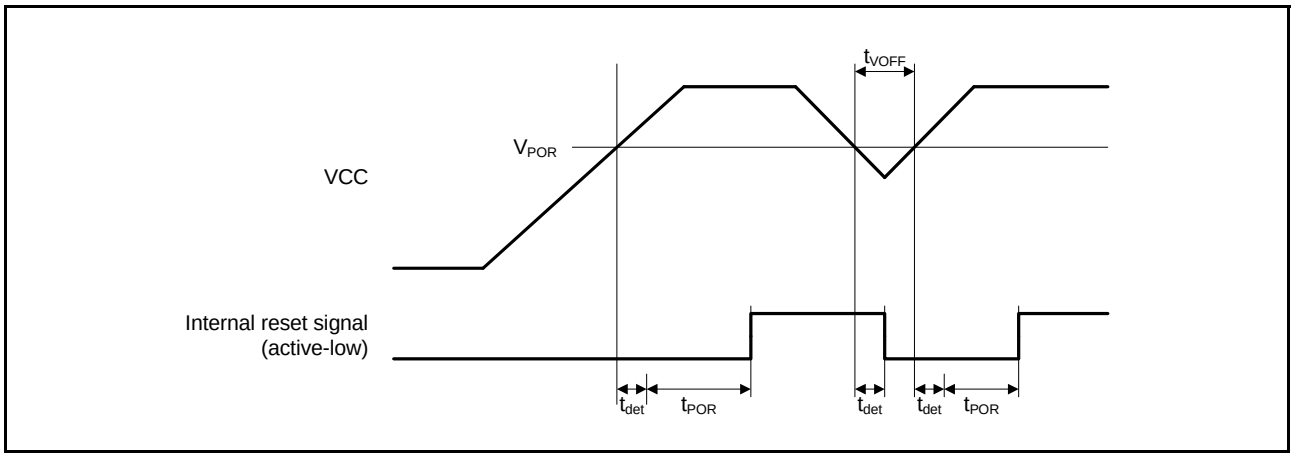


Figure 5.40 Power-on Reset Timing

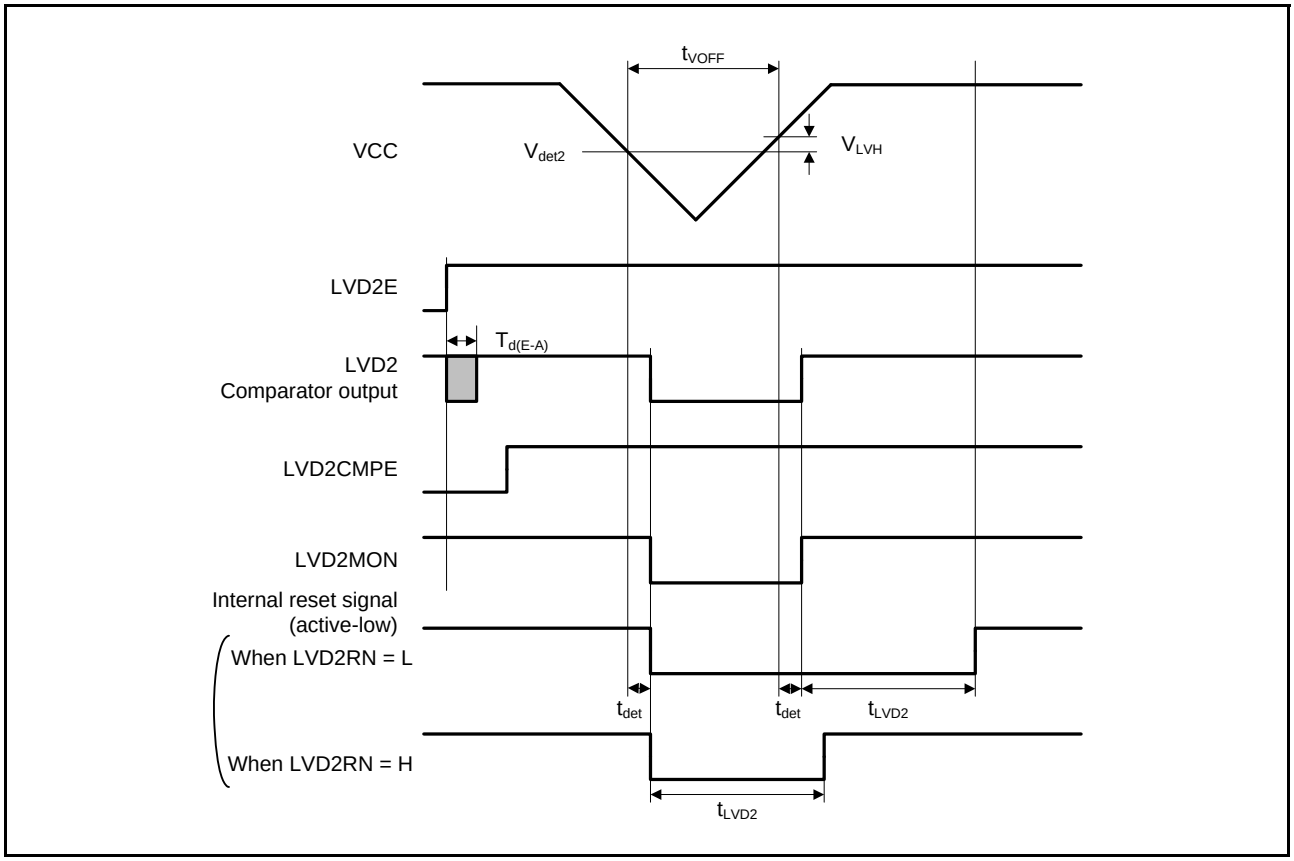


Figure 5.43 Voltage Detection Circuit Timing (V_{det2})

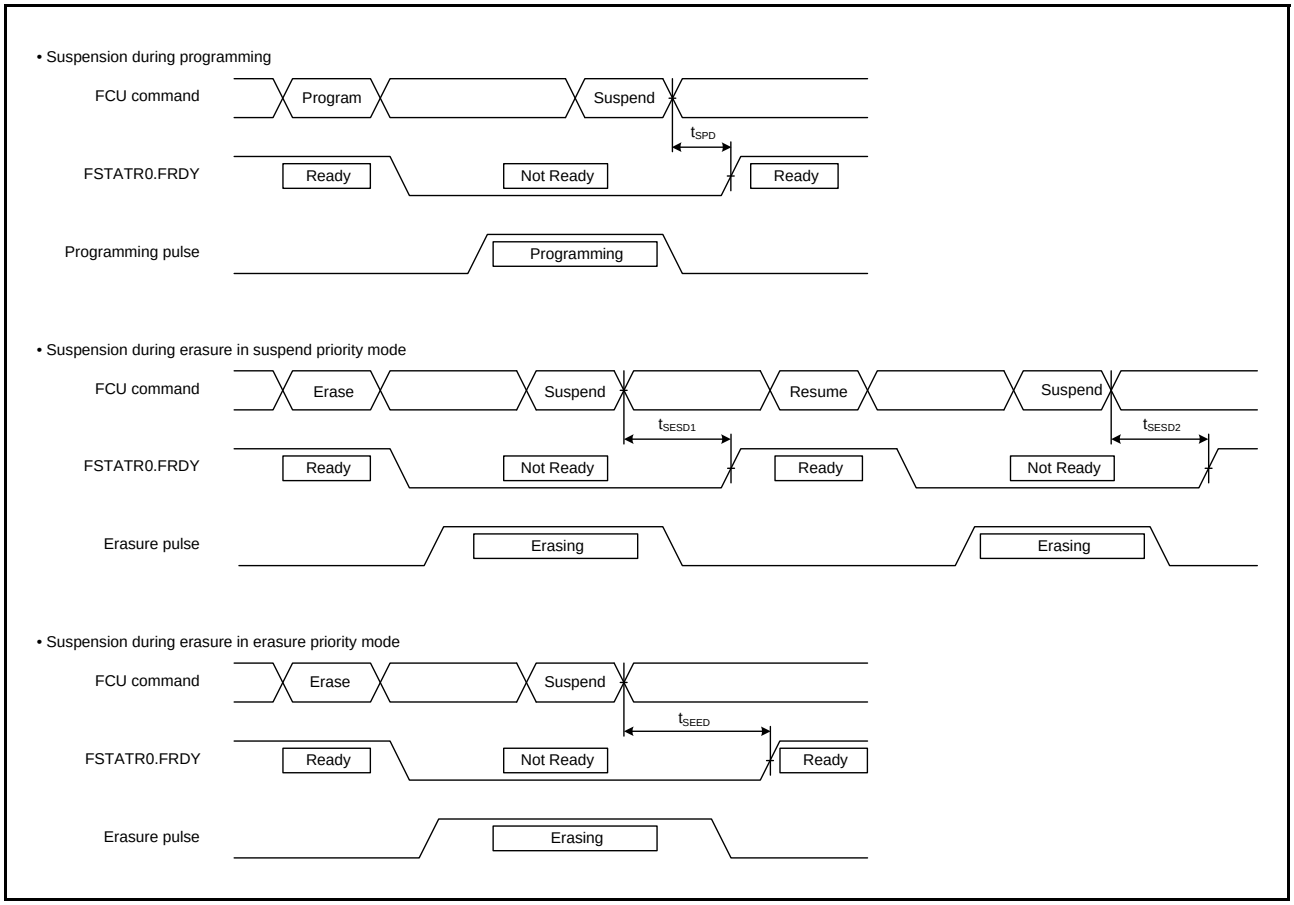
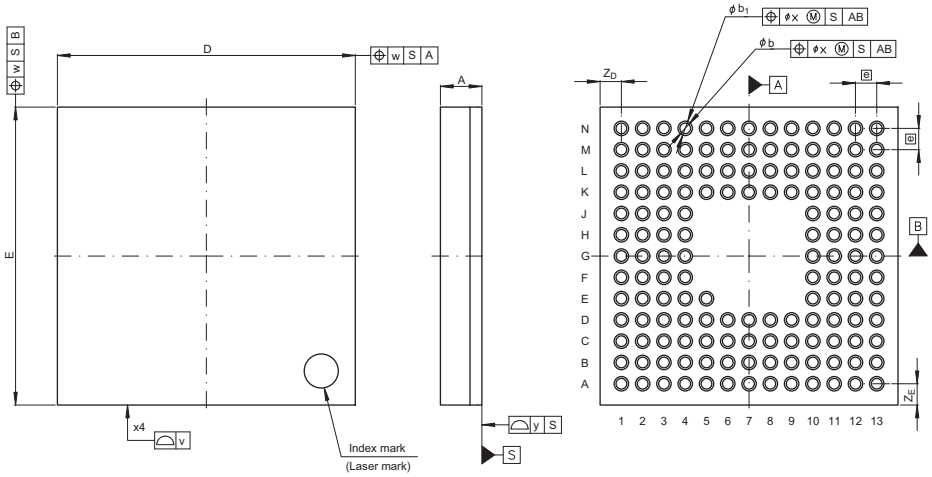


Figure 5.46 Flash Memory Program/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 145-Pin TFLGA (PTLG0145KA-A)