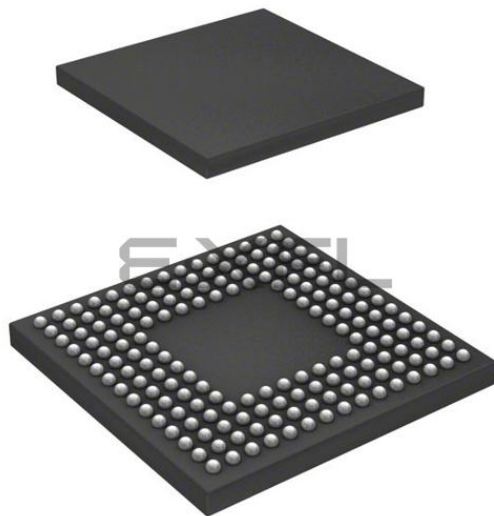




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	148
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630dcdbg-u0

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX630 (D version)	R5F56307CDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLC	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VSS	Input	Ground pin. Connect it to the system power supply (0 V)
	VBATT	Input	Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices
	XCOUT	Output	Input/output pins for the sub-clock oscillator circuit. Connect a crystal resonator between XCOUT and XCIN
	XCIN	Input	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on these pins must not be changed during operation
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid
	TRDATA0 to TRDATA3	Output	These pins output the trace information
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

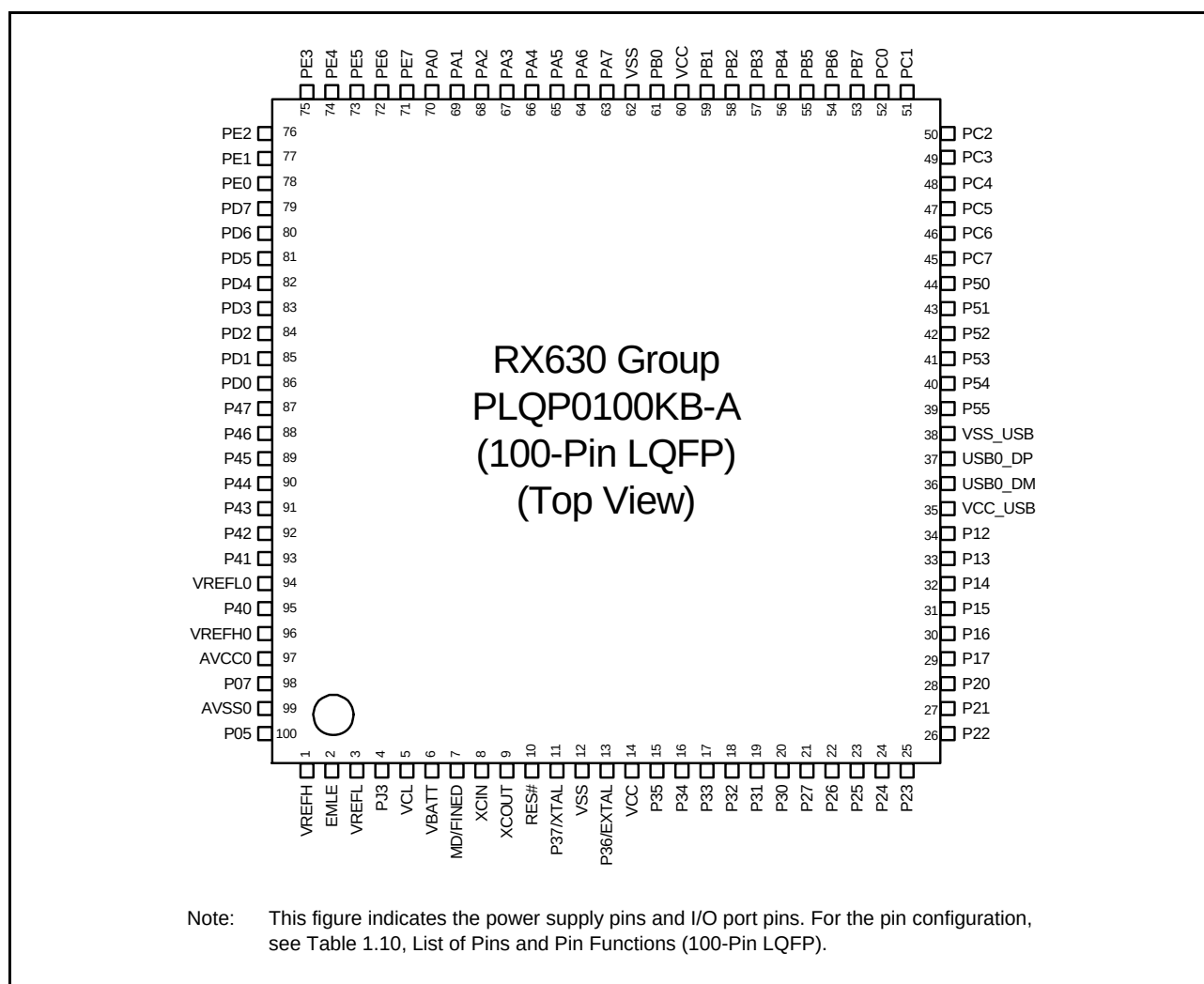


Figure 1.9 Pin Assignment (100-Pin LQFP)

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (1/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	NC						
17	TRST#	PF4					
18	MD/FINED						
19	XCIN						
20	XCOUT						
21	RES#						
22	XTAL	P37					
23	VSS						
24	EXTAL	P36					
25	VCC						
26		P35				NMI	
27		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
28		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOU/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
30	TMS	PF3					
31	TDI	PF2			RXD1/SMISO1/SSCL1		
32		P31		MTIOC4D/TMCI2/PO9/ RTIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
33		P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
34	TCK/FINEC	PF1			SCK1		
35	TDO	PF0			TXD1/SMOSI1/SSDA1		
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
38		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
39		PH5					
40		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
H4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
H5		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
H6		P54	ALE	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1		
H7		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMOSI8/SSCL8/ MOSIA	IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMOSI9/SSCL9		
H10		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
J1		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
J2		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0	IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
J4		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
J5	VSS_USB						
J6	VCC_USB						
J7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
J9		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1	IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2	IRQ12	
K1		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
K2		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0	IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
K5					USB0_DM		
K6					USB0_DP		
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA		
K9		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
K10		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.11 List of Pins and Pin Functions (80-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
37		PC5	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA		
38		PC4	MTIOC3D/MTCLKC/ TMCI1/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
39		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
40		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
41		PB7	MTIOC3B/TIOC5B/PO31	TXD9/SMOSI9/SSDA9		
42		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
43		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
44		PB4	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
45		PB3	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6		
46		PB2	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#		
47		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
48	VCC					
49		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
50	VSS					
51		PA6	MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
52		PA5	TIOCB1/PO21	RSPCKA		
53		PA4	MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
54		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
55		PA2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
56		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
57		PA0	MTIOC4A/TIOCA0/PO16	SSLA1		
58		PE5	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN3
59		PE4	MTIOC4D/MTIOC1A/PO28	SSLB0		AN2
60		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
61		PE2	MTIOC4A/PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN0
62		PE1	MTIOC4C/PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		ANEX1
63		PE0		SCK12/SSLB1		ANEX0
64		PD2	MTIOC4D		IRQ2	AN010
65		PD1	MTIOC4B		IRQ1	AN009
66		PD0			IRQ0	AN008
67		P47			IRQ15-DS	AN007
68		P46			IRQ14-DS	AN006
69		P45			IRQ13-DS	AN005
70		P44			IRQ12-DS	AN004
71		P43			IRQ11-DS	AN003
72		P42			IRQ10-DS	AN002

Table 1.11 List of Pins and Pin Functions (80-Pin LQFP) (3/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
73		P41			IRQ9-DS	AN001
74	VREFL0					
75		P40			IRQ8-DS	AN000
76	VREFH0					
77	AVCC0					
78		P07			IRQ15	ADTRG0#
79	AVSS0					
80		P05			IRQ13	DA1

Table 4.1 List of I/O Registers (Address Order) (6/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2	ICLK	ICUb
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2	ICLK	
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2	ICLK	
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2	ICLK	
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2	ICLK	
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2	ICLK	
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2	ICLK	
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2	ICLK	
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2	ICLK	
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2	ICLK	
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2	ICLK	
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2	ICLK	
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2	ICLK	
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2	ICLK	
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2	ICLK	
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2	ICLK	
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2	ICLK	
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2	ICLK	
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2	ICLK	
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2	ICLK	
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2	ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2	ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2	ICLK	
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2	ICLK	
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2	ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2	ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2	ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2	ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2	ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2	ICLK	
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2	ICLK	
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2	ICLK	
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2	ICLK	
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2	ICLK	
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2	ICLK	
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2	ICLK	
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2	ICLK	
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2	ICLK	
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2	ICLK	
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2	ICLK	
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2	ICLK	
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2	ICLK	
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2	ICLK	
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2	ICLK	
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2	ICLK	
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2	ICLK	
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2	ICLK	
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2	ICLK	
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2	ICLK	
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (19/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8370h	RIIC3	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I ² C bus receive data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83C0h	RSPI2	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C1h	RSPI2	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83C2h	RSPI2	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (33/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B0h	MPC	PE0 pin function control register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DAh	MPC	PK2 pin function control register	PK2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DBh	MPC	PK3 pin function control register	PK3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DCh	MPC	PK4 pin function control register	PK4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DDh	MPC	PK5 pin function control register	PK5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM

Table 4.1 List of I/O Registers (Address Order) (34/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C300h	ICU	Group 0 interrupt source register	GRP00	32	32	1, 2 PCLKB	2 ICLK	ICUb
0008 C304h	ICU	Group 1 interrupt source register	GRP01	32	32	1, 2 PCLKB	2 ICLK	
0008 C308h	ICU	Group 2 interrupt source register	GRP02	32	32	1, 2 PCLKB	2 ICLK	
0008 C30Ch	ICU	Group 3 interrupt source register	GRP03	32	32	1, 2 PCLKB	2 ICLK	
0008 C310h	ICU	Group 4 interrupt source register	GRP04	32	32	1, 2 PCLKB	2 ICLK	
0008 C314h	ICU	Group 5 interrupt source register	GRP05	32	32	1, 2 PCLKB	2 ICLK	
0008 C318h	ICU	Group 6 interrupt source register	GRP06	32	32	1, 2 PCLKB	2 ICLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1, 2 PCLKB	2 ICLK	
0008 C340h	ICU	Group 0 interrupt enable register	GEN00	32	32	1, 2 PCLKB	2 ICLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1, 2 PCLKB	2 ICLK	
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1, 2 PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1, 2 PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1, 2 PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1, 2 PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1, 2 PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1, 2 PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1, 2 PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1, 2 PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1, 2 PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1, 2 PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1, 2 PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1, 2 PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1, 2 PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1, 2 PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (35/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCa
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ah	RTC	Date capture register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK	Temperature Sensor
0008 C880h	SYSTEM	Counter-clock extension register 1	SCK1	8	8	2, 3 PCLKB	2 ICLK	MCK
0008 C890h	SYSTEM	Counter-clock extension register 2	SCK2	8	8	2, 3 PCLKB	2 ICLK	
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0842h	CAN0	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 0850h	CAN0	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (40/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 0072h	USB0	Pipe 2 control register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	USBa
000A 0074h	USB0	Pipe 3 control register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 0076h	USB0	Pipe 4 control register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 0078h	USB0	Pipe 5 control register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 007Ah	USB0	Pipe 6 control register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 007Ch	USB0	Pipe 7 control register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 007Eh	USB0	Pipe 8 control register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 0080h	USB0	Pipe 9 control register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 0090h	USB0	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	
000A 0092h	USB0	Pipe 1 transaction counter register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9/(\text{frequency ratio of ICLK/PCLKB})^8$	

Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	115	mA	ICLK = 100 MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 50 MHz	
		Normal	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	75			
		All-module-clock-stop mode (reference value)			—	20	45			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—	ICLK = 1 MHz ICLK = 32.768 kHz		
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA		
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power function enabled consumption function disabled		—	21	60			
			Power-on reset circuit and low-power function enabled consumption function enabled		—	6.2	28			
		Increased by RTC operation			—	3	—			
		RTC operation when VCC is off			—	1.7	—		V _{BATT} = 2.3 V	
					—	3.3	—	V _{BATT} = 3.3 V		
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA		
	During 10-bit A/D conversion			I _{VREFH} *7	—	1.0	1.65	mA		
	During D/A conversion (per unit)				—	0.7	1.0	mA		
	Waiting for A/D, D/A conversion (all units)*8			—	—	25	35	μA		
	A/D, D/A converter in standby mode (all units)*8				—	0.1	5	μA		
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7	mA		
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA		
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0	μA		
RAM standby voltage				V _{RAM}	2.7	—	—	V		
VCC rising gradient				SrVCC	8.4	—	20000	μs/V		
VCC falling gradient*8				SfVCC	8.4	—	—	μs/V		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.48 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 8. The values are the sum of I_{AVCC0} and I_{VREFH}.

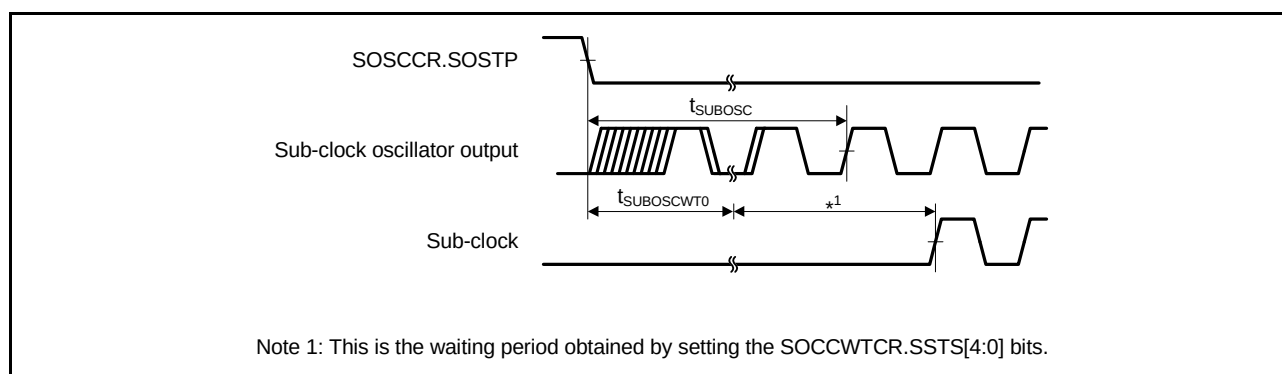


Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.13 Timing of Recovery from Low Power Consumption Modes

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t _{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t _{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t _{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t _{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t _{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t _{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDG-dedicated on-chip oscillator operating		t _{SBYLO}	—	—	800	μs	
Recovery time after cancellation of deep software standby mode			t _{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t _{DSBYWT}	45	—	46	t _{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

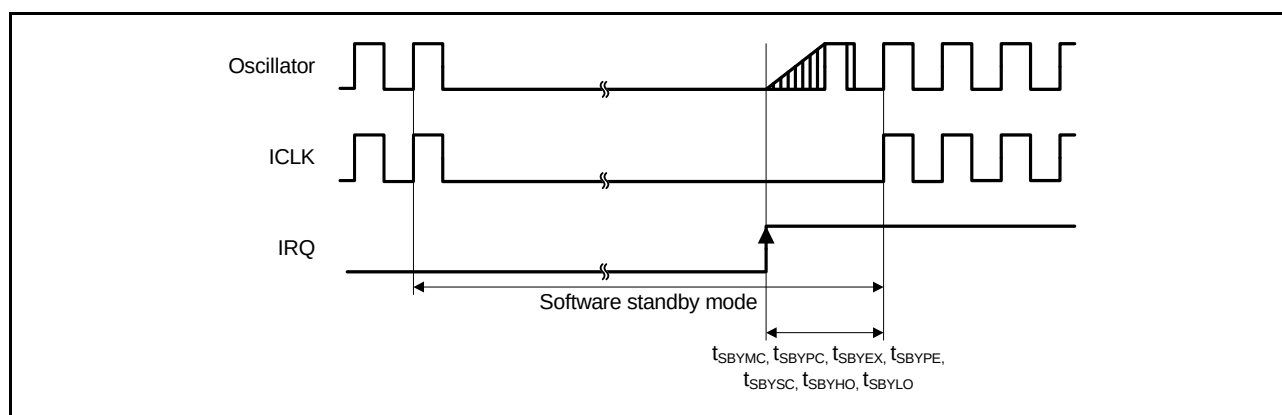


Figure 5.13 Software Standby Mode Cancellation Timing

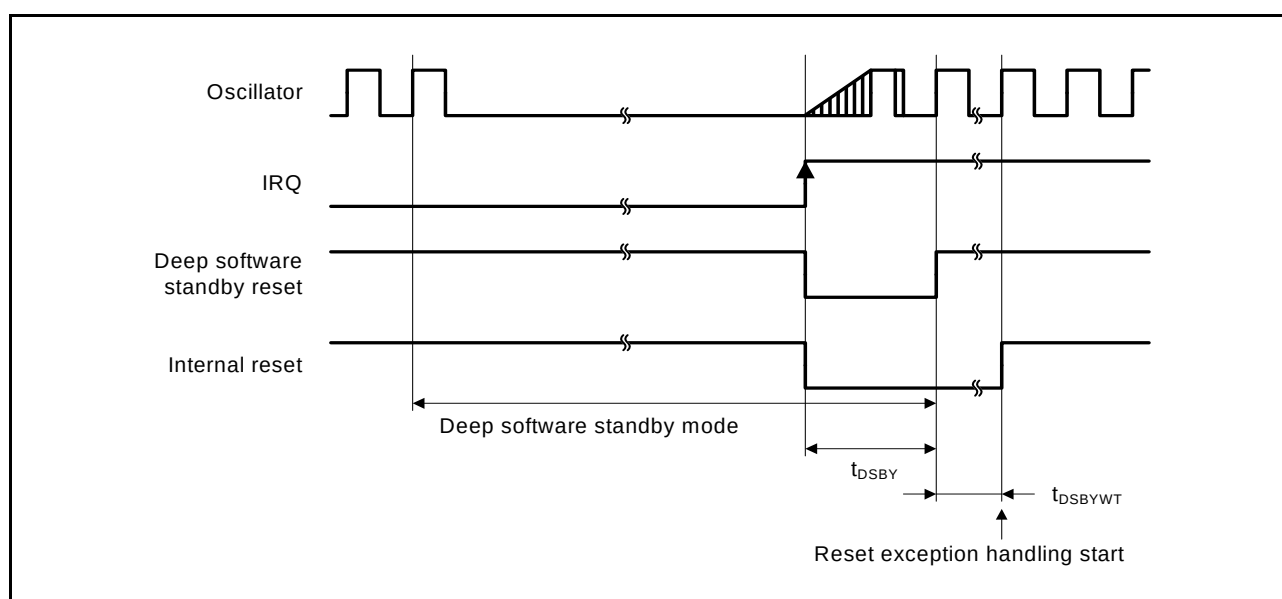


Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.14 Control Signal Timing

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.16

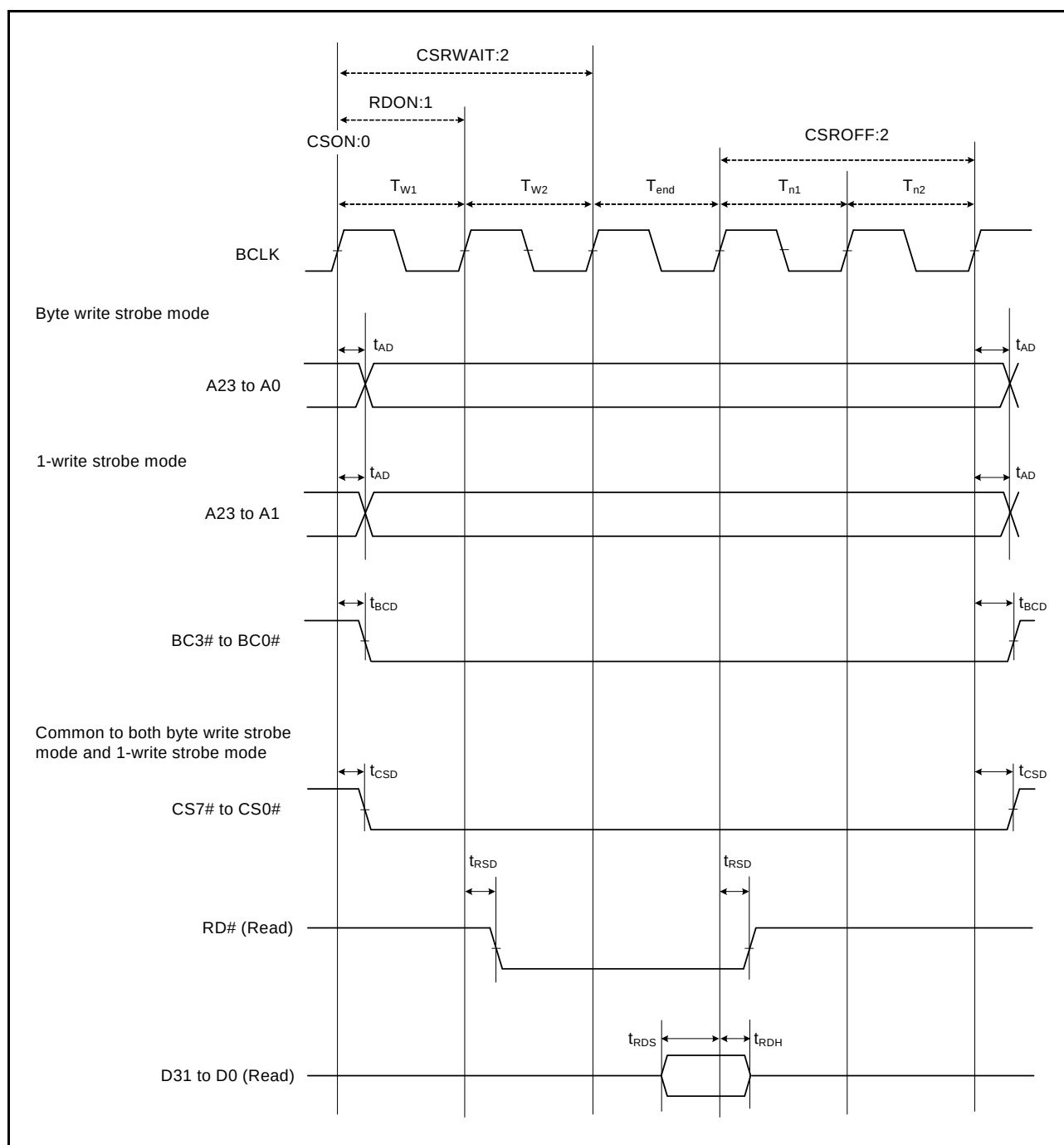


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.23 12-Bit A/D Conversion CharacteristicsConditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	AN0 to AN7	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.4)*2	—	—	μs	Sampling in 20 states
	Other channels	Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 3.0 V	2.0 (1.4)*2	—	—	μs	Sampling in 70 states
		Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 2.7 V	5.6 (5.0)*2	—	—	μs	Sampling in 250 states
Analog input capacitance			—	—	30	pF	
Offset error			—	±2.0	±7.5	LSB	
Full-scale error			—	±2.0	±7.5	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±2.5	±8.0	LSB	
DNL differential nonlinearity error			—	±2.0	±4.0	LSB	
INL integral nonlinearity error			—	±2.0	±4.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.24 A/D Internal Reference Voltage CharacteristicsConditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D Internal reference voltage	1.45	1.50	1.55	V	

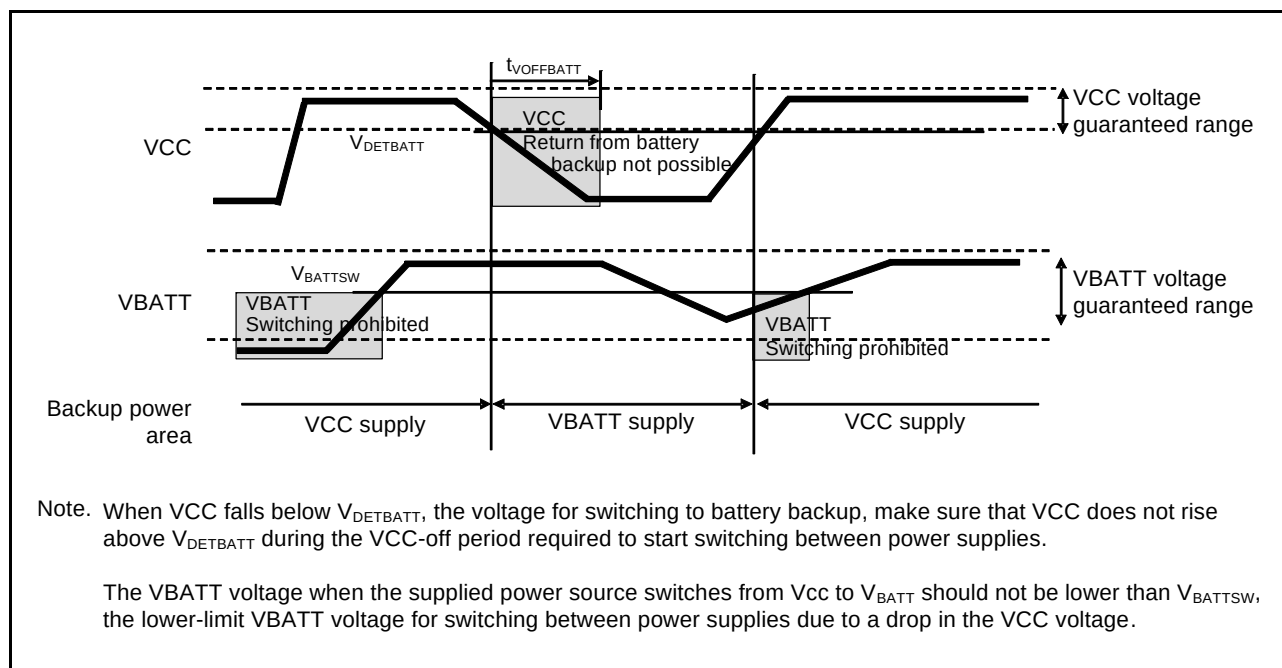
5.10 Battery Backup Function Characteristics

Table 5.29 Battery Backup Function Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$, $V_{BATT} = 2.3$ to 3.6 V
 $VSS = AVSS0 = VREFL/VREFO = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.45
Lower-limit VBATT voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	μs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

**Figure 5.45 Battery Backup Function Characteristics**

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