Renesas Electronics America Inc - R5F5630DCDFB#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630dcdfb-v0

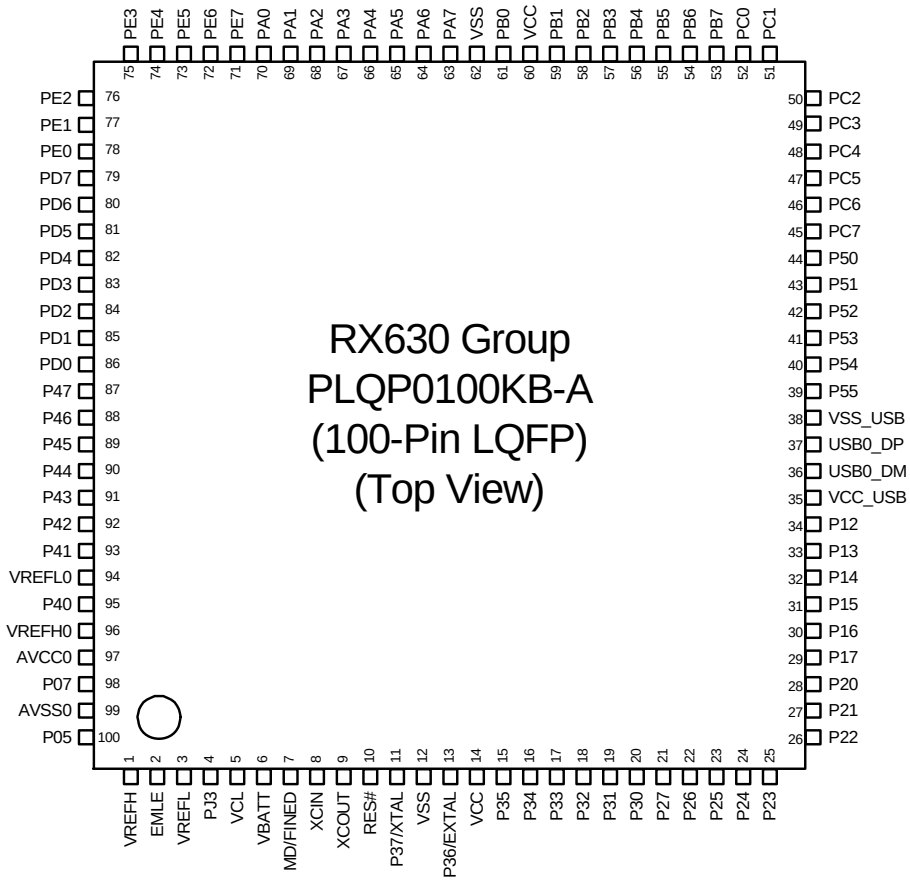
1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes • 100 MHz, no-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode)
	RAM	• Capacity: 64 Kbytes, 96 Kbytes, 128 Kbytes • 100 MHz, no-wait access
	E^2 data flash	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
MCU operating modes		Single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.9 Pin Assignment (100-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C14		PK4			RXD4/SMISO4/SSCL4		
C15		P70			SCK4		
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8		PK1					
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#		CTS9#/RTS9#/SS9#		
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
D13		PK5			TXD4/SMOSI4/SSDA4		
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#		CRX2*2	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#		CTX2*2		
F13	TRSYNC#	PG4	D28				
F14		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
G15	VCC						

Table 1.6 List of Pins and Pin Functions (176-Pin LQFP) (5/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
151		PK1					
152		P96	A22/D22				
153		PK0					
154		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
155		P95	A21/D21				
156		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/CLKG	MOSIC/CTX0	IRQ1	AN009
157		P94	A20/D20				
158		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
159		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
160		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
161		P91	A17/D17		SCK7		AN015
162	VSS						
163		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
164	VCC						
165		P47				IRQ15-DS	AN007
166		P46				IRQ14-DS	AN006
167		P45				IRQ13-DS	AN005
168		P44				IRQ12-DS	AN004
169		P43				IRQ11-DS	AN003
170		P42				IRQ10-DS	AN002
171		P41				IRQ9-DS	AN001
172	VREFL0						
173		P40				IRQ8-DS	AN000
174	VREFH0						
175	AVCC0						
176		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 MB/1.5 MB

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

Table 4.1 List of I/O Registers (Address Order) (2/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK		DMACA
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK		
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK		
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK		
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK		
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK		
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK		
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK		
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK		
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK		
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK		
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK		
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK		DTCa
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK		
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK		
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK		
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK		
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK		
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK		
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK		
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (7/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK		ICUb
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK		
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK		
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK		
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK		
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK		
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK		
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK		
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK		
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK		
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK		
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK		
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK		
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK		
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK		
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK		
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK		
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK		
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK		
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK		
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK		
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK		
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK		
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK		
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK		
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK		
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK		
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK		
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK		
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK		
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK		
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2 ICLK		
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2 ICLK		
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2 ICLK		
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2 ICLK		
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK		
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK		
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK		
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK		
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK		
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK		
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK		
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2 ICLK		
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK		
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK		
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK		
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK		
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK		
0008 7121h	ICU	DTC activation enable register 033	DTCER033	8	8	2 ICLK		
0008 7122h	ICU	DTC activation enable register 034	DTCER034	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (11/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2 ICLK		ICUb
0008 732Ah	ICU	Interrupt source priority register 042	IPR042	8	8	2 ICLK		
0008 732Dh	ICU	Interrupt source priority register 045	IPR045	8	8	2 ICLK		
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8	2 ICLK		
0008 7334h	ICU	Interrupt source priority register 052	IPR052	8	8	2 ICLK		
0008 7338h	ICU	Interrupt source priority register 056	IPR056	8	8	2 ICLK		
0008 733Eh	ICU	Interrupt source priority register 062	IPR062	8	8	2 ICLK		
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK		
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK		
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK		
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK		
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK		
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK		
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK		
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK		
0008 7348h	ICU	Interrupt source priority register 072	IPR072	8	8	2 ICLK		
0008 7349h	ICU	Interrupt source priority register 073	IPR073	8	8	2 ICLK		
0008 734Ah	ICU	Interrupt source priority register 074	IPR074	8	8	2 ICLK		
0008 734Bh	ICU	Interrupt source priority register 075	IPR075	8	8	2 ICLK		
0008 734Ch	ICU	Interrupt source priority register 076	IPR076	8	8	2 ICLK		
0008 734Dh	ICU	Interrupt source priority register 077	IPR077	8	8	2 ICLK		
0008 734Eh	ICU	Interrupt source priority register 078	IPR078	8	8	2 ICLK		
0008 734Fh	ICU	Interrupt source priority register 079	IPR079	8	8	2 ICLK		
0008 735Ah	ICU	Interrupt source priority register 090	IPR090	8	8	2 ICLK		
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK		
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK		
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8	2 ICLK		
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK		
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK		
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK		
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8	2 ICLK		
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8	2 ICLK		
0008 736Eh	ICU	Interrupt source priority register 110	IPR110	8	8	2 ICLK		
0008 736Fh	ICU	Interrupt source priority register 111	IPR111	8	8	2 ICLK		
0008 7370h	ICU	Interrupt source priority register 112	IPR112	8	8	2 ICLK		
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK		
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2 ICLK		
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2 ICLK		
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2 ICLK		
0008 7384h	ICU	Interrupt source priority register 132	IPR132	8	8	2 ICLK		
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK		
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK		
0008 738Ch	ICU	Interrupt source priority register 140	IPR140	8	8	2 ICLK		
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK		
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK		
0008 7394h	ICU	Interrupt source priority register 148	IPR148	8	8	2 ICLK		
0008 7396h	ICU	Interrupt source priority register 150	IPR150	8	8	2 ICLK		
0008 7398h	ICU	Interrupt source priority register 152	IPR152	8	8	2 ICLK		
0008 739Ch	ICU	Interrupt source priority register 156	IPR156	8	8	2 ICLK		
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (28/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C013h	PORTK	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C014h	PORTL	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C033h	PORTK	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C034h	PORTL	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.6	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC +0.3	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to +5.8	V
Reference power supply voltage		VREFH	–0.3 to VCC +0.3	V
Analog power supply voltage		AVCC*2	–0.3 to +4.6	V
Analog input voltage		V_{AN}	–0.3 to VCC +0.3	V
Operating temperature	D version	T_{opr}	–40 to +85	°C
	G version	T_{opr}	–40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20 to 25, 30 to 34, 50 to 52, 54 to 57, 67, 74 to 77, 80 to 82, A1 to A4, A6, B, and C are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI, WAIT#, TCK		VCC × 0.8	—	VCC + 0.3		
	XCIN*3		VCC × 0.8	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, WAIT#, TCK		–0.3	—	VCC × 0.2		
	XCIN*3		–0.3	—	VCC × 0.2		
	D0 to D31		–0.3	—	VCC × 0.3		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 12 to 17, 20 to 25, 30 to 34, 50 to 52, 54 to 57, 67, 74 to 77, 80 to 82, A1 to A4, A6, B, and C are 5 V tolerant.
Note 3. For P32, P31, P30, and XCIN, input as follows when the V_{BATT} power supply is selected.
VIH Min. = V_{BATT} × 0.8, VIH Max. = V_{BATT} + 0.3, VIL Min. = –0.3, VIL Max. = V_{BATT} × 0.2

5.3 AC Characteristics

Table 5.7 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLKB)		—*1	—	50	
	FlashIF clock (FCLK)		—*2	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	
	IEBUS clock (IECLK)		—	—	44.03	

Note 1. The PCLKB must run at a frequency of at least 24 MHz if the USB is in use.
Note 2. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

Table 5.8 Operation Frequency Value (Low-Speed Operating Mode 1)

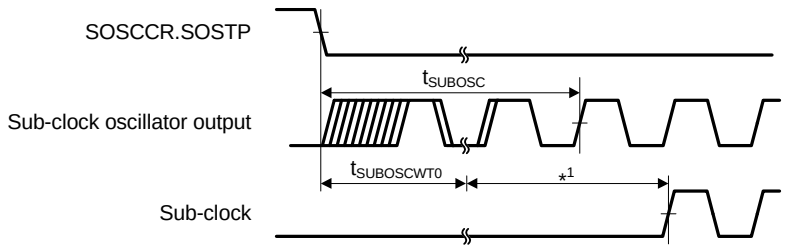
Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKB)		—	—	1	
	FlashIF clock (FCLK)		—	—	1	
	External bus clock (BCLK)		—	—	1	
	BCLK pin output		—	—	1	
	USB clock (UCLK)		—	—	1	
	IEBUS clock (IECLK)		—	—	1	

Table 5.9 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	32	—	143.75	kHz
	Peripheral module clock (PCLKB)		—	—	143.75	
	FlashIF clock (FCLK)		32	—	143.75	
	External bus clock (BCLK)		—	—	143.75	
	BCLK pin output		—	—	143.75	
	USB clock (UCLK)		—	—	143.75	
	IEBUS clock (IECLK)		—	—	143.75	



Note 1: This is the waiting period obtained by setting the SOCCWTCR.SSTS[4:0] bits.

Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.13 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t_{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

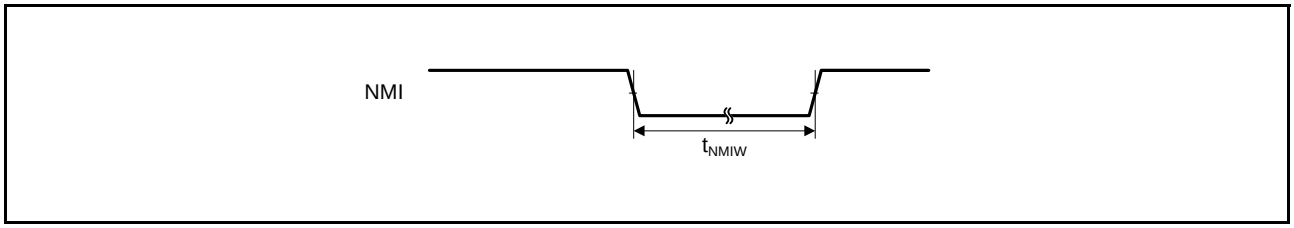


Figure 5.15 NMI Interrupt Input Timing

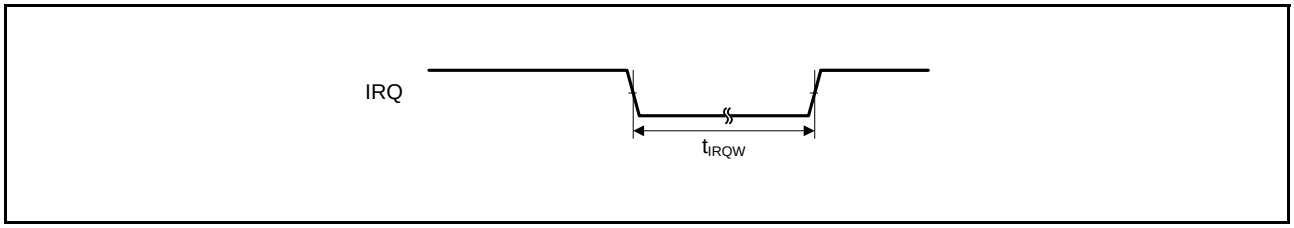


Figure 5.16 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.15 Bus Timing

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 100 MHz, BCLK = 8 to 50 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF
High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	20	ns	
CS# delay time	t_{CSD}	—	20	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	20	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.20 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*, *2	Max.*	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.37
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 120$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle, t_{Pcyc}: PCLK cycle
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

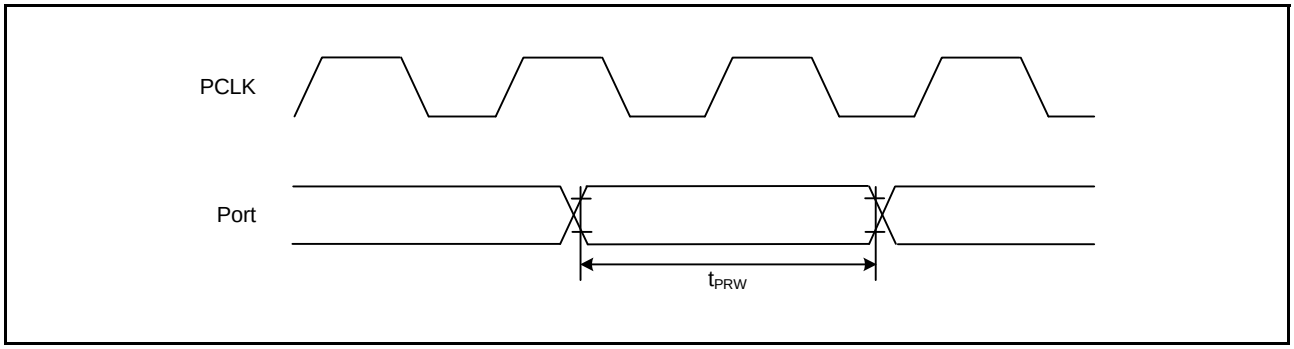


Figure 5.24 I/O Port Input Timing

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V_{POR}	2.5	2.6	2.7	V	Figure 5.40
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0}	2.7	2.80	2.9		Figure 5.41
	Voltage detection circuit (LVD1)		V_{det1_A}	2.75	2.95	3.15		
	Voltage detection circuit (LVD2)		V_{det2_A}	2.75	2.95	3.15		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 5.40
	LVD0 reset time		t_{LVD0}	—	4.6	—		Figure 5.41
	LVD1 reset time		t_{LVD1}	—	0.9	—		Figure 5.42
	LVD2 reset time		t_{LVD2}	—	0.9	—		Figure 5.43
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 5.40 and Figure 5.41
Response delay time			t_{det}	—	—	200	µs	Figure 5.40 to Figure 5.43
LVD operation stabilization time (after LVD is enabled)			$Td_{(E-A)}$	—	—	3	µs	Figure 5.42 and Figure 5.43
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

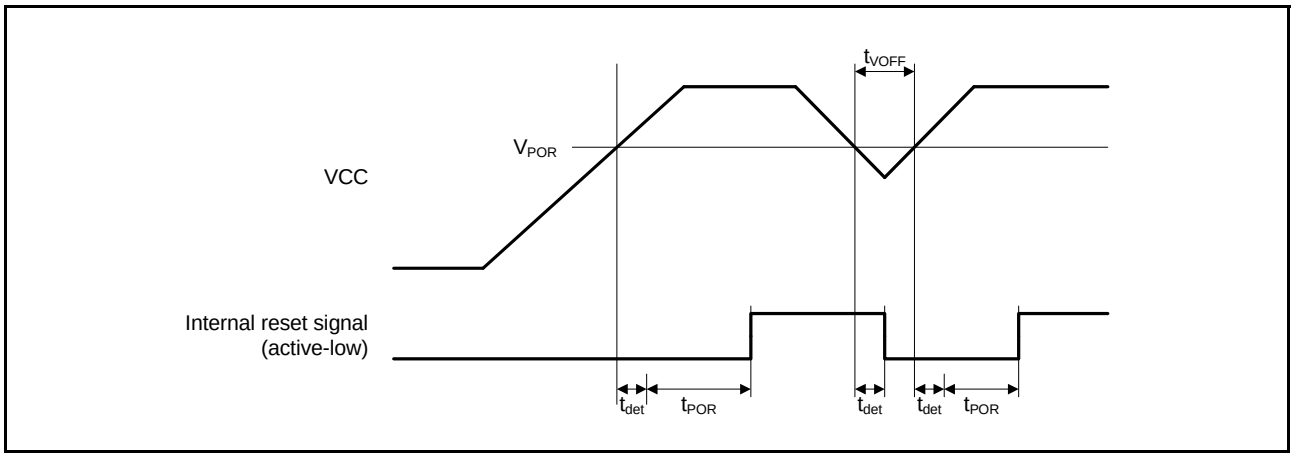


Figure 5.40 Power-on Reset Timing

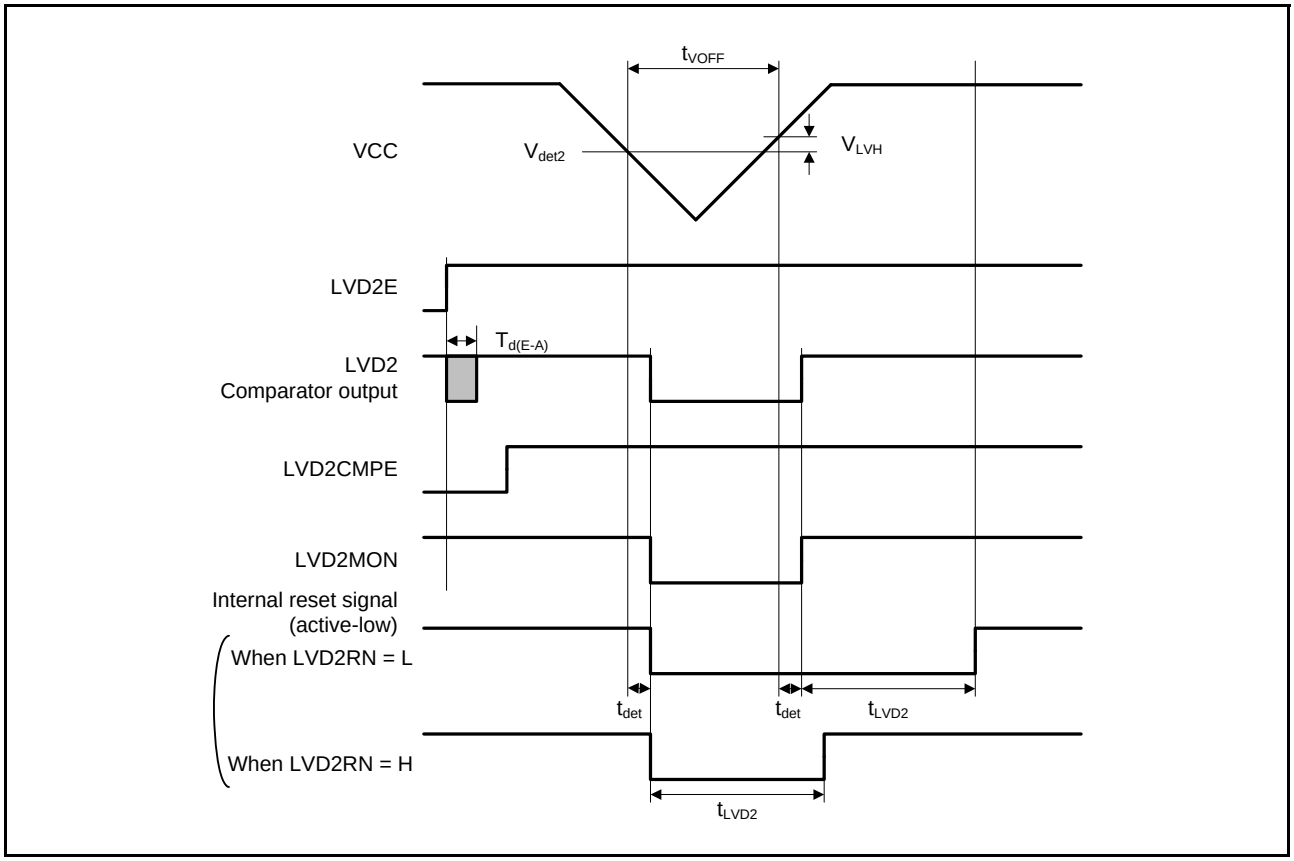


Figure 5.43 Voltage Detection Circuit Timing (V_{det2})

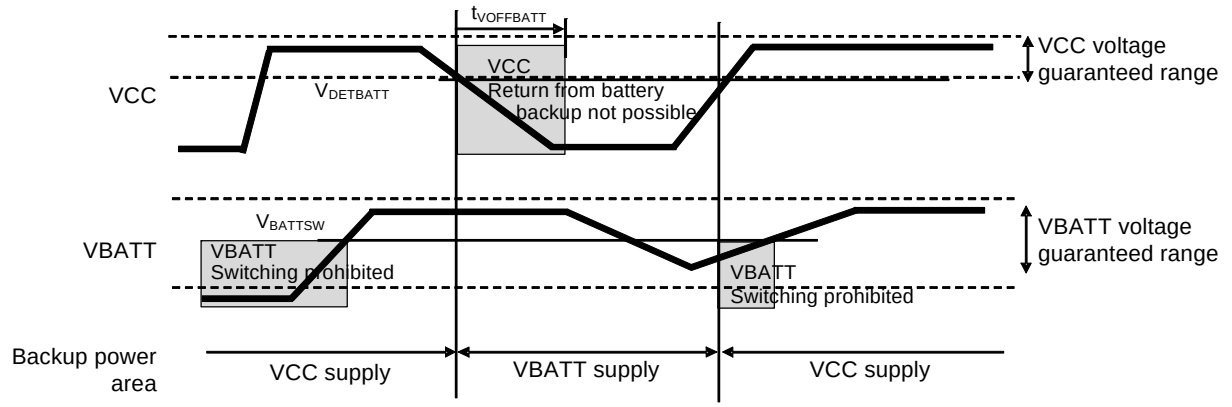
5.10 Battery Backup Function Characteristics

Table 5.29 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V_{BATT} = 2.3 to 3.6 V
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.45
Lower-limit VBATT voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

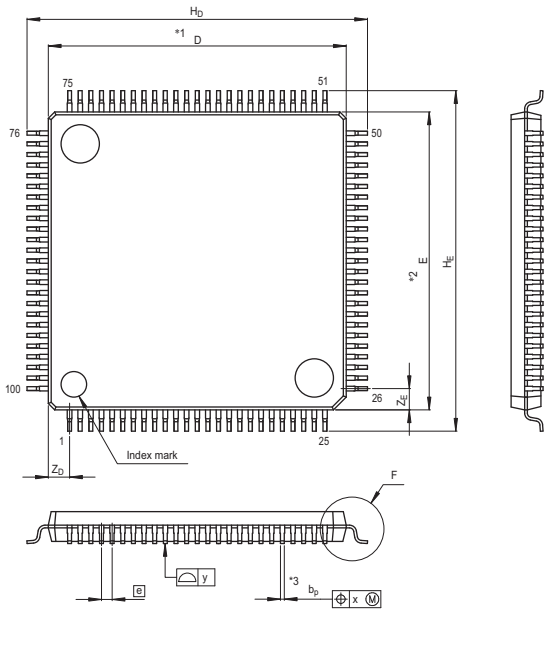


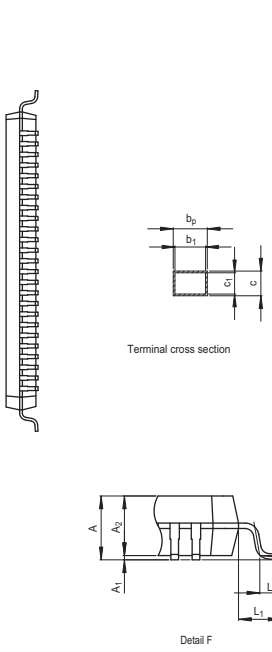
Note. When VCC falls below $V_{DETBATT}$, the voltage for switching to battery backup, make sure that VCC does not rise above $V_{DETBATT}$ during the VCC-off period required to start switching between power supplies.

The VBATT voltage when the supplied power source switches from Vcc to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 5.45 Battery Backup Function Characteristics

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure G 100-Pin LQFP (PLQP0100KB-A)

Rev.	Date	Description		Classification
		Page	Summary	
1.60	May 19. 2014	120	Figure 5.21 External Bus Timing/Page Read Cycle (Bus Clock Synchronized), changed	
		120	Figure 5.22 External Bus Timing/Page Write Cycle (Bus Clock Synchronized), changed	
		121	Figure 5.23 External Bus Timing/External Wait Control, changed	
		123	Table 5.17 Timing of On-Chip Peripheral Modules (2), changed	
		124	Table 5.18 Timing of On-Chip Peripheral Modules (3), changed	
		125	Table 5.19 Timing of On-Chip Peripheral Modules (4): min and max, changed, Note, added	TN-RX*-A014A/E
		126	Table 5.20 Timing of On-Chip Peripheral Modules (5): min and max, changed, Note, added	TN-RX*-A014A/E
		129	Figure 5.32 RSPI Clock Timing and Simple SPI Clock Timing, changed	
		129	Figure 5.33 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1), changed	
		130	Figure 5.34 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0), changed	
		130	Figure 5.35 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), changed	
		131	Figure 5.36 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), changed	
		131	Figure 5.37 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing, changed	
		132	Table 5.21 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics): Item, changed	
		133	Table 5.22 10-Bit A/D Conversion Characteristics: Note, changed	
		134	Table 5.23 12-Bit A/D Conversion Characteristics: Note, changed	
		139	Figure 5.44 Oscillation Stop Detection Timing, changed	
		140	Figure 5.45 Battery Backup Function Characteristics, changed	
		141	Table 5.30 ROM (Flash Memory for Code Storage) Characteristics (1), added	
		141	Table 5.31 ROM (Flash Memory for Code Storage) Characteristics (2): Table and title, changed	
		142	Table 5.32 E2 Flash Characteristics (1), added	
		142	Table 5.33 E2 Flash Characteristics (2): Table and title, changed	